

POST-CMOS PROCESSING FOR HIGH-ASPECT-RATIO INTEGRATED SILICON MICROSTRUCTURES

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ABSTRACT

We present a new fabrication sequence for integrated-silicon microstructures designed and manufactured in a conventional CMOS process. The sequence employs a post-CMOS deep silicon backside etch, which allows fabrication of high aspect ratio (25:1) and flat MEMS devices with integrated circuitry. A comb-drive actuator and a beam resonator were fabricated using this process sequence. Electrical isolation of single-crystal silicon was realized by using the undercut of the reactive ion etch (RIE) process. The fabricated devices were actuated electrostatically and flatness characterized using interferometric measurements.

INTRODUCTION

Micromachined devices fabricated by CMOS-compatible fabrication processes are attractive because of the possibility to integrate high-performance on-chip signal conditioning circuits and digital readouts, and expected multi-vendor accessibility and short design cycle times. Currently, most CMOS-compatible micromachining processes are polysilicon or poly-Ge surface micromachining processes that use silicon oxide as the sacrificial material and typically involve a wet etch for releasing micromechanical structures [1,2]. Even though vapor HF is often used, protection of integrated circuits and sticking problems during release are still major concerns [3]. Moreover, the relatively large parasitic capacitance in many integrated polysilicon processes degrades performance of capacitive sensor designs.

In prior work, post-CMOS surface micromachining processes use composite microstructures made from combinations of aluminum, silicon oxide, and silicon nitride thin films [4]. For these processes, the silicon substrate acts as the sacrificial material and is undercut for release (Fig. 1). The resultant multi-conductor microstructures provide wiring flexibility and low parasitic capacitance to the substrate. Both lateral and vertical CMOS accelerometers [5,6] with fully differential full bridge capacitive interface circuits have been fabricated by using this post-CMOS micromachining process. A tri-axial microstage has also been realized [7].

However, all of the microstructures discussed above are made of thin films, either homogeneous or multi-layer. Thin-film deposition processes generate residual stress and stress gradients which cause curling. This limits the maximum thickness and size of microstructures, which are critical dimensions for inertial sensors. Moreover, release holes and unwanted curvature of microstructures degrade their applications in optics.

Deep RIE (DRIE) technologies have advanced significantly in recent years. By alternating passivation and etching cycles, the Bosch advanced silicon etch (ASE) process [8] can typically achieve high aspect ratios of 20~30:1. For example, a bulk silicon comb-drive actuator with 100 μm deep comb fingers and 15 μm gap spacing has been fabricated by using the ASE process [9]. Because silicon etch rate of the ASE process is relatively high ($\sim 3\mu\text{m}/\text{min}$), it is feasible to release microstructures by through-wafer etching, instead of by undercutting the silicon substrate [10]. However, given a typical wafer thickness ($\sim 500\mu\text{m}$), a minimum gap spacing of 20 μm would be needed to retain anisotropy. Such a spacing is too large for either effective sensing or actuation.

Our solution is to combine the maskless post-CMOS micromachining process [4], ASE and backside etch. The backside etch is used to control the thickness of the final, released, microstructures, which allows optimization of design parameters and simplifies the packaging process. The new process sequence (Fig. 2) provides high-aspect-ratio and flat microstructures. *It incorporates all the advantages of CMOS composite microstructures with the excellent mechanical properties of single crystal silicon.*

In this paper, a new CMOS DRIE micromachining process will be described and contrasted with the previous post-CMOS surface micromachining process. Characterization results of two example devices fabricated using the new process flow will be presented and some process issues will be discussed.

CMOS MICROMACHINING PROCESSES

CMOS surface micromachining process

The previous post-CMOS micromachining process [4] consists of an anisotropic dielectric etch for defining the microstructures and an isotropic silicon etch for release. Fig. 1 shows the cross-sectional view after the process is completed. The etching masks are interconnect metals from preceding CMOS processing, so no post-CMOS photolithography is required. An aspect ratio as high as 4:1 can be achieved. The microstructures consist of up to three metal layers that are electrically isolated by dielectrics, which

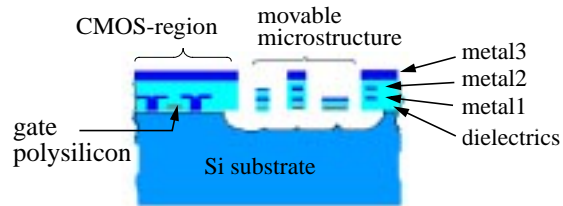


Figure 1. Cross-sectional view of the thin-film post-CMOS micromachining processing.

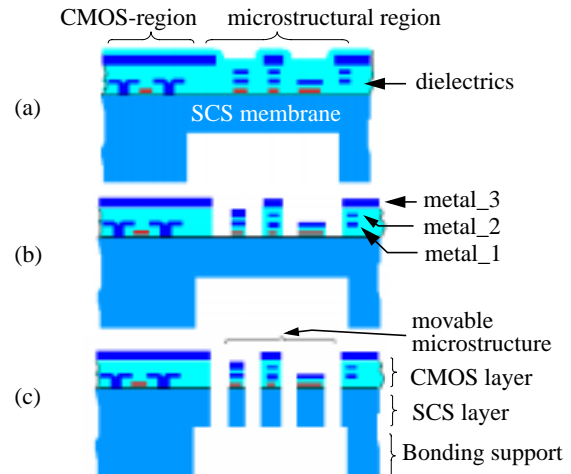


Figure 2. The process-flow for the modified CMOS micromachining. (a) CMOS-chip with backside etch. (b) Anisotropic dielectric etch. (c) Anisotropic silicon etch for release.

enables a variety of wiring configurations within the moving microstructures [5-7]. One issue with CMOS-MEMS is that the residual stress and thermal coefficient mismatch in the embedded layers cause curling or bending [11]. Vertical curling can be compensated to first order through a curl matching frame [5], but the maximum size which can be compensated is limited and design complexity is increased.

CMOS backside micromachining process

In order to overcome some of the drawbacks of thin-film microstructures without losing the advantages of the multi-conductor structures, we propose a new process sequence building on the previous post-CMOS micromachining process. The basic idea is to introduce a single-crystal silicon (SCS) layer underneath the CMOS multi-layer structures in such a way that the mechanical properties are dominated by the SCS layer and electrical connections are provided by the CMOS microstructure layer.

The process flow is given in Fig. 2. We start with a deep anisotropic backside etch leaving a 10 to 100 μm thick SCS membrane (Fig. 2 (a)). This backside etch step is used to control the thickness of microstructures as well as to form a cavity to simplify the packaging process. Next an anisotropic dielectric etch is performed from the frontside (Fig. 2 (b)). Then in contrast to the prior work on post-CMOS processing, we use an anisotropic instead of an isotropic silicon etch for release (Fig. 2 (c)). Therefore, a thick SCS layer remains underneath the CMOS layer, resulting in a totally flat released microstructure. Thus, no curling compensation is needed and a microstructure can be designed to an arbitrary shape. Furthermore, the proof mass and comb-finger capacitance for CMOS-MEMS based inertial sensors is significantly increased. Fig. 3 shows the SEMs of a comb-drive actuator fabricated by using the new process. Both sides are flat (no visible curling). In a later section, we will discuss the optical and electrical characterization of this device in detail.

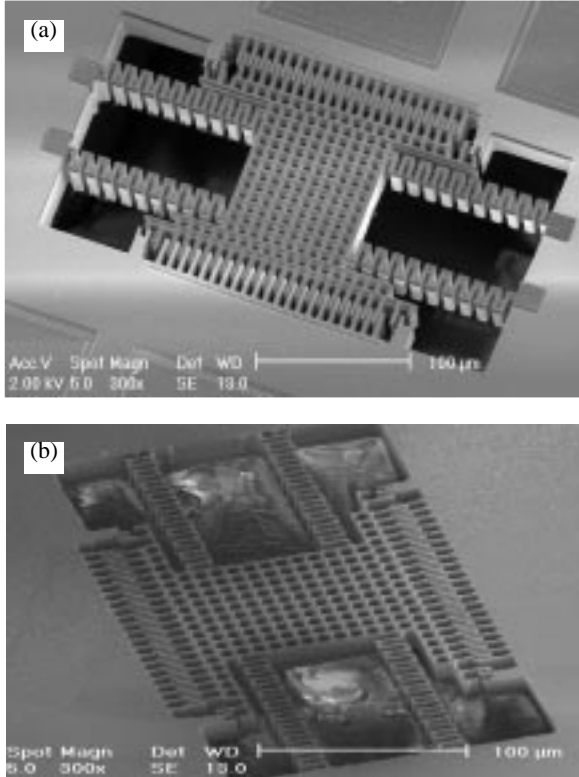
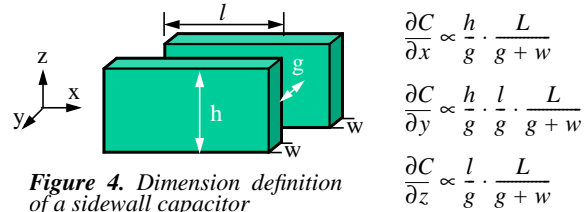


Figure 3. SEMs of the comb-drive actuator fabricated by using the new process. (a) Front-side view. (b) Backside view.

Design considerations

Since there is no fixed electrode underneath the microstructures, this technology is mainly suitable for sidewall capacitive sensing and actuation. Suppose there are two side-by-side beams, e.g., a pair of comb fingers, as shown in Fig. 4. The sidewall capacitance change versus displacement in the longitudinal, transverse and vertical directions have the following relationships,



$$\frac{\partial C}{\partial x} \propto \frac{h}{g} \cdot \frac{L}{g+w}$$

$$\frac{\partial C}{\partial y} \propto \frac{h}{g} \cdot \frac{l}{g} \cdot \frac{L}{g+w}$$

$$\frac{\partial C}{\partial z} \propto \frac{l}{g} \cdot \frac{L}{g+w}$$

Figure 4. Dimension definition of a sidewall capacitor

where l , g , h and w are the engaged length, gap, height and width of the comb fingers, respectively, and L is the total length of the comb-finger area. The total number of comb fingers is thus $L/(g+w)$. The gap aspect-ratio is h/g , which is fixed for the ASE process. If a fixed area is assumed, i.e., L is fixed, then the smaller the gap, the larger the capacitance change in all three directions. The height of the comb fingers may be set by the minimum possible gap. Thicker comb fingers would require a larger gap and result in a reduction in capacitive sensitivity. However, there is a minimum SCS layer thickness that just eliminates the stress-induced curling. Note that this minimum thickness value depends on the size of the designed microstructure as well as the thickness control accuracy of the deep RIE process. For inertial sensors, mass is a critical parameter that dictates resolution. For inertial applications, the SCS layer should be as thick as possible and there is a trade-off between the gap spacing and the structural thickness.

There is a small undercut in the deep RIE, which actually can be advantageous. If the width of a beam is smaller than two times the undercut, the SCS layer underneath this beam will be etched away. Through complete undercut of the silicon, released areas of bulk silicon can be electrically isolated. In addition, soft springs can be obtained by using the same principle. An electrically isolated SCS block is shown in Fig. 5, where the beam width is 0.8 μm and the CMOS bridge provides mechanical support as well as electrical wiring. To further guarantee the electrical isolation, the to-be-undercut silicon region is implanted as n-well (for p-silicon substrate) to form a p-n-p junction in case there is still a remaining thin layer of silicon.

Fabrication

We used single-chip processing to demonstrate the DRIE release sequence. The square CMOS chips (2 mm by 2 mm) are made in the Hewlett Packard 0.5 μm three-metal n-well process available through MOSIS.

The chips come with an unpolished backside. Prior to the deep etching process the backside was patterned in a photolithography step with a backside release mask using a 10 μm layer of a high viscosity photoresist (Shipley AZ 4620). The exposure was performed with a Karl-Suss MA 56 mask aligner. There is no need for a high backside-frontside alignment accuracy. The patterning has to guar-

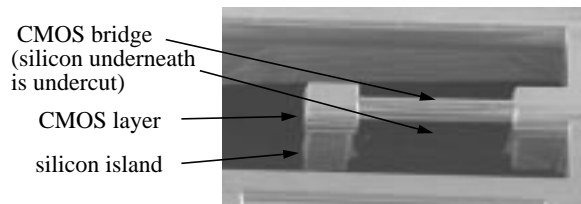


Figure 5. SEM of an electrically isolated SCS block

antee that a sufficient silicon frame for mechanical support of the silicon membrane remains after the deep etch. The chips were mounted on a 4" silicon wafer covered with photoresist. The backside ASE etch for defining the silicon membrane was performed in a Surface Technology Systems (STS) ICP etcher. The etching-process employed is a typical ASE process [8] with an etching rate of $2.9 \mu\text{m} / \text{min}$ for a small silicon load. The main plasma parameters for the etching part of the cycle are: 600 watt coil power; 12 watt platen power; 130 sccm SF_6 flow; and 23 mT chamber pressure. The passivation is performed at an identical plasma power and 12 mT chamber pressure with 85 sccm of C_4F_8 with no platen power. The duration of the etching cycle is 12 seconds and in the passivation cycle we deposit the fluorocarbon polymer for 8 seconds. The major demands for the etching process are good stability of the etching rate, low surface roughness and a sufficiently uniform structural thickness. A polishing of the chip backside prior to the backside deep etch improves the smoothness of the resulting silicon membrane surface but is not necessary. The backside etch step defines the thickness of the remaining silicon membrane and high accuracy measurements of the thickness of the chips and the etch depth are necessary. We employ an optical microscope to perform these measurements. By using a 50x microscope objective, accuracies of $\pm 3 \mu\text{m}$ can be achieved. After removal of the chips from the carrier wafer and an oxygen plasma clean of the chip frontside, the oxide RIE etch of the CMOS-micromachining process (Fig. 2(b)) is performed in a Plasma-Therm 790 reactor.

For performing the anisotropic silicon release step (Fig. 2 (c)) in the STS ICP etcher, the chips were mounted on a 4" photoresist-covered silicon wafer. The top metal of the CMOS layers served as the mask. We observed no degradation of the top metal layer even for etching durations of several hours. We could not detect any performance decrease of the ICP etcher due to use of the Al mask. Only die-sized samples were processed, which limited the amount of aluminum exposed in the chamber.

The SEM in Fig. 6 shows the depth differences for three trench-widths due to well known micro-loading effects of the ASE process [12]. The trenches with a larger width are etched faster. Therefore the large open areas are etched through to the backside first before the narrow gaps. This results in polymer-deposition on the remaining silicon backside during the passivation steps of the ASE.

Fig. 7 (a) shows a close-up of the backside of a comb drive actuator after performing

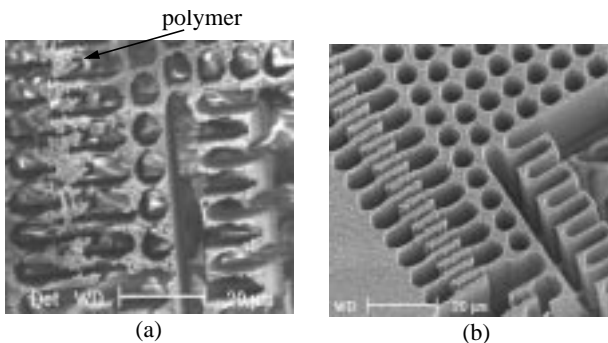


Figure 7. SEMs of the backside of the comb-drive actuator.
 (a) No oxygen plasma clean step during the anisotropic release.
 (b) Smooth and clean backside after oxygen plasma cleaning.

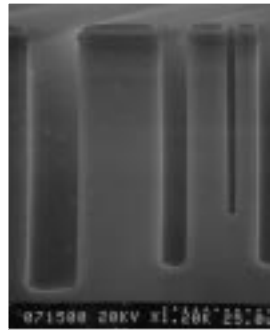


Figure 6. Microloading effect of the ASE process.

the anisotropic etch step. The polymer deposited on the backside of the SCS layer due to the relatively early etch-through of the wider gaps forms a residual structural layer that cannot be etched by continuing the ASE process. The polymer layer is removed by using a zero-bias oxygen plasma clean at the end of the process flow after the narrow gaps are etched through to the polymer film. Fig. 6 (b) shows the backside of a clean device after an oxygen plasma step is used at the end of the release procedure.

CHARACTERIZATION

Beam resonator

In order to investigate the mechanical properties of the composite microstructures with stacked CMOS and SCS layers, a $110 \mu\text{m}$ -long and $3.0 \mu\text{m}$ -wide cantilever beam was designed. Fig. 8 shows the released beams. The gap is $2.1 \mu\text{m}$, which limits beam thickness to a maximum of $55 \mu\text{m}$ for an aspect-ratio of 25. The fabricated beam thickness is $45 \mu\text{m}$. In the figure, the typical scallops of the ASE process and an undercut of about $0.4 \mu\text{m}$ were observed. The measured resonant frequency is 254 kHz, which is in good agreement with the finite element simulation of 249 kHz. The Young's modulus of the SCS layer is assumed to be 168 GPa [13] and the CMOS layer has an effective Young's modulus of 63 GPa [11].

Comb-drive actuator

Fig. 9 is a close-up of the comb-drive actuator shown in Fig. 3. The gap of the comb fingers is $1.2 \mu\text{m}$ and thus the underlying SCS layer has been thinned down to $25 \mu\text{m}$ thick for an aspect-ratio of ~ 25 . The lateral displacement versus the applied DC voltage squared is plotted in Fig. 10. The plot shows that the stiffness of the serpentine springs is increased by a factor of 4 by the underlying thick SCS layer. Note that the underlying SCS beam width is $\sim 0.8 \mu\text{m}$ narrower than the CMOS microstructure due to the $0.4 \mu\text{m}$

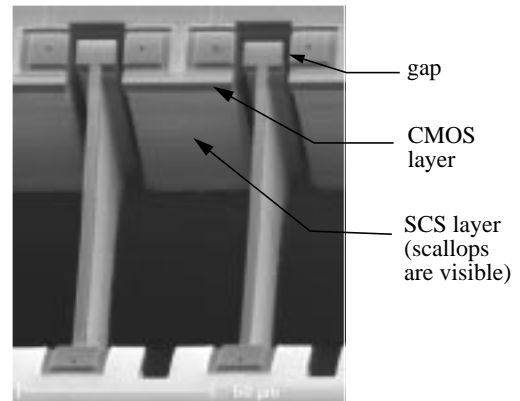


Figure 8. SEM of the beam-resonators

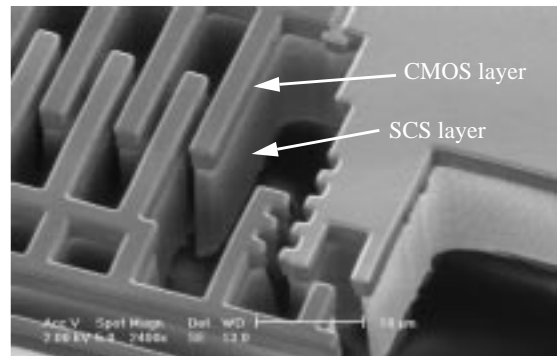


Figure 9. Close-up of one corner of the comb-drive actuator (see Fig. 3).

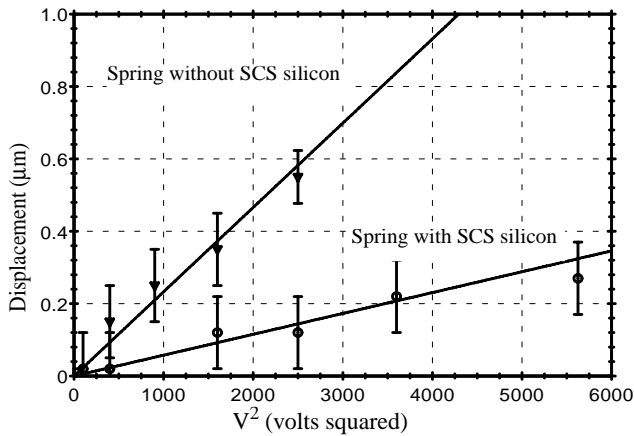


Figure 10. Measured displacement of comb drive actuators versus squared voltage.

undercut. Also note that the underlying SCS is not electrically isolated from the silicon substrate in this comb-drive actuator.

To evaluate the topography of the released structures, we employed a Linnik-type Michelson interferometer with LED illumination ($\lambda=610$ nm). The topography is calculated from a series of fringe patterns using a phase shifting technique. We achieved a measurement accuracy of better than 40 nm for the z-curling. Fig. 11 (a) shows the measured topography of a comb-drive actuator with no underlying SCS layer. The peak-to-valley curling measured on the whole device is 1.2 μm . For a device with underlying SCS, we found a curling of 0.15 μm -- nearly an order of magnitude decrease (Fig. 11 (b)).

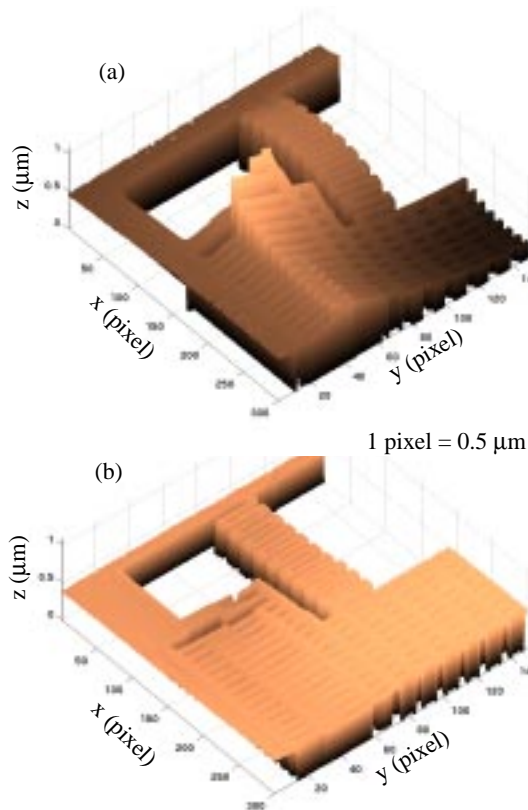


Figure 11. The topography of the released comb-drive actuator (see Fig. 3) (only one quarter is shown) obtained by using phase shifting interferometry. (a) Conventional release. (b) Backside release.

CONCLUSIONS

The new post-CMOS micromachining process is demonstrated by using a beam-resonator and a comb-drive actuator. This process is CMOS compatible and can generate flat and thick microstructures with optimized gap spacing. The unique electrical isolation of the silicon and multi-conductor features provide high expectations for capacitive sensing and actuation. The resultant large mass and increased comb-finger capacitance will give rise to high resolution and high sensitivity for inertial sensors as well as larger forces for microactuators.

The microloading effect is crucial in this process, which can be used to realize electrical isolation of silicon and soft springs. The silicon membrane thickness control is another important issue which is under further active investigation.

ACKNOWLEDGEMENT

This project is sponsored by the DARPA-MEMS program, under contract F30602-97-2-0323.

REFERENCES

- [1] R.T. Howe, B.E. Boser, A.P. Pisano, "Polysilicon integrated microsystems: technologies and application", *Sensors and Actuators A (Physical)*, vol.A56, no.1-2, p. 167-77.
- [2] A.E. Franke, D. Bilic, D.T. Chang, P.T. Jones, T.-J. King, R.T. Howe, G.C. Johnson, "Post-CMOS integration of germanium microstructures", *MEMS'99*, Orlando, FL, USA; 17-21 Jan. 1999, p630-637.
- [3] C. Hierold, "Intelligent CMOS sensors", *MEMS'2000*, Miyazaki, Japan, 25-28 Jan. 2000, p1-6.
- [4] G.K. Fedder, S. Santhanam, M.L. Reed, S.C. Eagle, D.F. Guillou, M.S.-C. Lu, L.R. Carley, "Laminated high-aspect-ratio microstructures in a conventional CMOS process", *Sensors and Actuators A*, vol.A57, p.103-110.
- [5] G. Zhang, H. Xie, L. deRosset, G.K. Fedder, "A lateral capacitive CMOS accelerometer with structural curl compensation", *MEMS'99*, Orlando, FL, USA; 17-21 Jan. 1999, p606-611.
- [6] H. Xie, G.K. Fedder, "A CMOS z-axis accelerometer with capacitive comb-finger sensing", *MEMS'2000*, Miyazaki, Japan; 25-28 Jan. 2000, p496-501.
- [7] H. Xie, L. Erdmann, Q. Jing, G.K. Fedder, "Simulation and characterization of a CMOS z-axis microactuator with electrostatic comb drives", *MSM'2000*, San Diego, CA; 27-29 Mar. 2000.
- [8] F. Laermer and A. Schilp of Robert Bosch GmbH, "Method of Anisotropically Etching Silicon", US-Patent No. 5501893.
- [9] Chris Seung-Bok Lee, Sejin Han, N.C. MacDonald, "Multiple depth, single crystal silicon microactuators for large displacement fabricated by deep reactive ion etching", *Technical Digest. Solid-State Sensor and Actuator Workshop*, Hilton Head Island, SC, USA; 8-11 June 1998, p.45-50.
- [10] E.M. Chow, *et al.*, "Fabrication of high-density cantilever arrays and through-wafer interconnects", *Technical Digest. Solid-State Sensor and Actuator Workshop*, Hilton Head Island, SC, USA; 8-11 June 1998, p.220-4
- [11] M.S.-C. Lu, X. Zhu, G.K. Fedder, "Mechanical property measurement of 0.5- μm CMOS microstructures", *Symposium on Microelectromechanical Structures for Materials Research*, San Francisco, CA, USA; 15-16 April 1998, p.27-32.
- [12] J. Jiao, M. Chablotz, T. Matsuura and K. Tsutsumi, "Mask layout related area effect on HARSE process in MEMS applications", *Transducers'99*, Sendai, Japan; 7-10 June. 1999, p546-549.
- [13] J.C. Greenwood, "Silicon in Mechanical Sensors", *J. Phys. E, Sci. Instrum.*, 21,(1998), p.1114-1128.