FREQUENCY-HOPPING CIRCUITS BASED ON RECONFIGURABLE MEMS CAPACITORS

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Abstract

Post-foundry micromachining enables integration of RF electronics with RF MEMS suspended inductors and reconfigurable capacitors for single chip frequency-hopping (FH) radios. Spiral inductors are formed in the thickest metal layer of the BEOL foundry interconnect stack. Post-CMOS etching removes the oxide between the turns to increase self-resonance frequency and removes the silicon under the spiral to increase Q. RF MEMS capacitors are formed using interdigitated beams fabricated from the BEOL foundry interconnect. The capacitance can be varied by changing the gap between interdigitated beams using an electrothermal actuator that is heated using embedded polysilicon resistors. A Q of 52, 1.5 GHz, capacitor with tuning range from 42 fF to 148 fF (3.52:1) within a 12 V control voltage and 34 mW power has been designed, fabricated and characterized in a 0.35 μm CMOS process. Reconfigurable capacitors with higher Q (>200) and zero standby power (using mechanical latch stops) have been designed. They have been integrated with the suspended inductor to form a RF filter that hops between 1.2 and 2.1 GHz. The π-network filter uses two reconfigurable capacitors: 170 fF/400 fF for dc blocking and 140 fF/800 fF for the tank capacitor. The relative insertion loss difference between the two frequencies is simulated to be 2.8 dB. Integration of the RF MEMS passive inductor and capacitor devices with 47 GHz SiGe HBT, enables the design of a negative-Gm FH oscillator that can also switch between 1.2 and 2.1 GHz. The oscillator is based on a MEMS capacitor that can reconfigure between 360 fF and 1.2 pF. Simulations indicate that phase noise exceeds -110 dBc/Hz for this 4.1 mW oscillator. These FH circuits are being fabricated.

INTRODUCTION

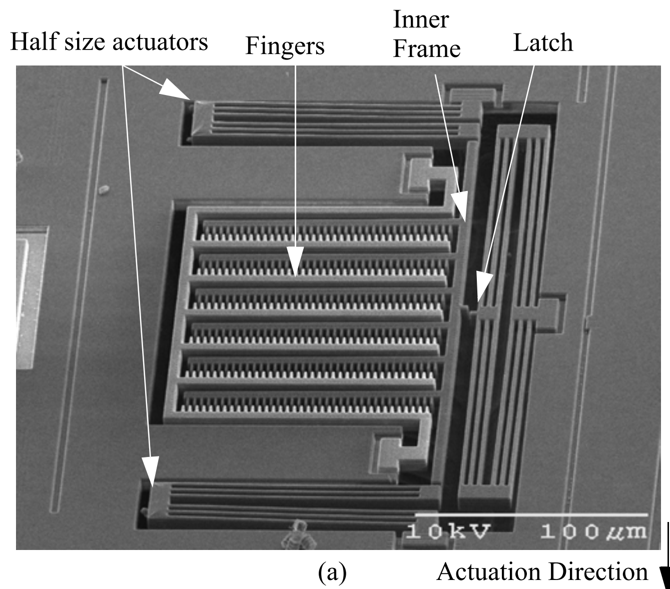
There is a continuing demand to monolithically integrate complete receiver on a single chip. These receivers require voltage-controlled oscillators (VCOs) with low phase noise and RF filters with low insertion loss. High-Q tunable capacitors improve the phase noise performance of VCOs. Micro-mechanical tunable capacitors have been used for getting high-Q for VCO applications [1-2]. Similarly, RF filters have been designed by using micro-mechanical tunable capacitors [3]. In the past few years, tunable capacitors based on MEMS technology have been designed [1-4], with tuning range in excess of 840% [3]. Other strategies used to achieve wide tuning range include diode or MOS varactors or switched capacitor banks. Compared with solid-state varactors, MEMS tunable lower capacitors have advantages of lower loss, larger tuning range and higher linearity.

In this paper, CMOS-compatible micromechanical reconfigurable capacitors are used with suspended inductors to design a RF filter and a VCO. Capacitor tuning ratios over 353% have been achieved, while still maintaining a Q above 50 at 1.5 GHz in a 0.35 μm CMOS process. Previous tunable MEMS capacitors have needed custom processing, and hence have to be bonded to a separately fabricated CMOS IC for potential applications like VCOs [1-2]. A key advantage of this approach is that CMOS electronics for VCOs and other possible applications are integrated on the same chip. Interconnect losses between chips are eliminated, resulting in lower phase noise and higher signal levels. Furthermore, off-chip interconnects introduce fixed capacitance to the VCO tank, which decreases its tuning range [1]. The new tunable capacitors can be used in wide-tuning-range VCOs and RF filters, having less parasitic capacitance.

RECONFIGURABLE CAPACITOR

Capacitor designs based on interdigitated beams and fingers are used, as the post-CMOS micromachining process [5] constrains structural design to a single mechanical layer. Gap tuning, achieved through electro-thermal actuation, is used to change the capacitance. These actuators can provide displacement from 1μm to 7μm [6]. Fig 1(a) shows a released tunable MEMS capacitor. In this design, two half-size electrothermal actuators are used to move the inner frame, changing the gaps between the fingers, hence the capacitance between the two electrodes. One of the design goals was switching between multiple capacitor values with low power operation. For these designs, lateral electro-thermal actuators are used to implement lateral latches. By using these latch structures, power is only consumed when switching between fixed capacitance values. The latch structures in the first TSMC 0.35 μm chip did not work as expected, due to lack of prior stress gradient characterization data during the design phase. Functional latches in future designs will require no power to operate statically at a given capacitance value. Previous designs consume continuous power for tuning [1-4]. Fig 1(b) and Fig 1(c) show a close-up view of the tunable capacitor fingers. The disengaged state is shown in Fig 1(b) after release without electro-thermal actuation. Fig 1(c) shows the engaged state with actuation of 12 V control voltage.

The high-aspect ratio CMOS micromachining technology is used for capacitor fabrication [5]. It begins with a conventional foundry CMOS process. After the foundry fabrication, several etch steps are used to release the structure. The undercut of silicon in the release step requires the placement of active circuits to be at least 40 μm away from the released MEMS structures.



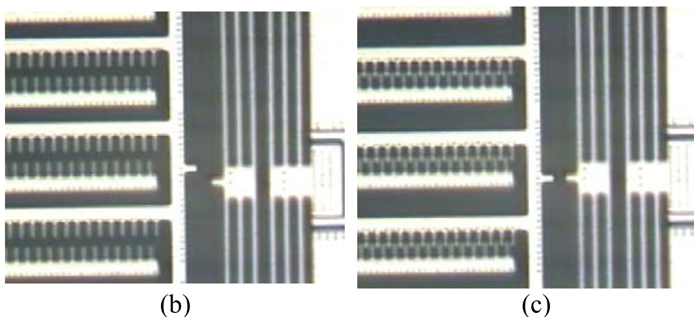


Fig. 1: (a) SEM of a released tunable capacitor in TSMC 0.35 μm CMOS process with half-size actuators. (b) disengaged mechanism for C_{MIN}. (c) engaged mechanism for C_{MAX} [7].

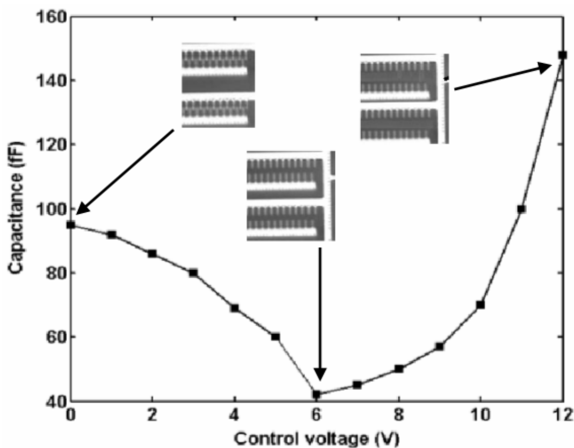


Fig. 2: Measured capacitance versus control voltage for a design with full-size actuators in TSMC 0.35 μm process [7].

S_{11} parameters of the tunable capacitors in TSMC 0.35 μm CMOS process are measured using an Agilent E8364A network analyzer from 45 MHz to 3 GHz. For these capacitors, large tuning ratios and high Q values have been achieved [7-8]. For the best of these designs, 3.52 to 1 tuning range has been measured with tuning from 42 fF to 148 fF within a 12 V control voltage and 34 mW power and Q of 52 at 1.5 GHz. Fig 2 shows the measured tuning characteristics of this design. With zero control voltage, the capacitance value is 95 fF, then it goes to 42 fF at 6 V control voltage, and achieves the highest value, 148 fF, at 12 V. The increase in capacitance for voltage above 6 V is due to the parallel-plate gap closing between adjacent banks of combs. This particular actuator design did not self-assemble in the intended fully engaged position due to the low residual stress gradients.

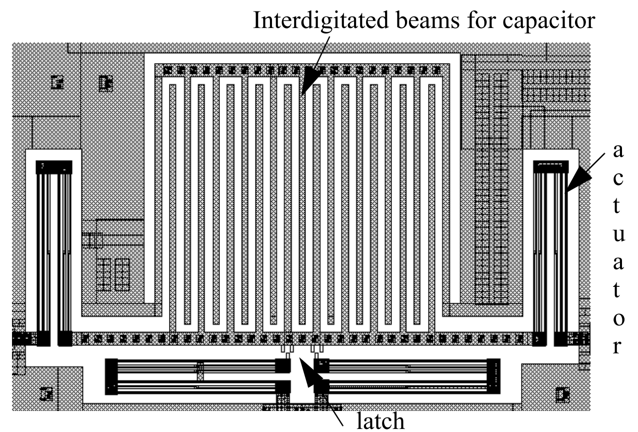


Fig. 3: Layout view of the reconfigurable capacitor design in IBM SiGe 6hp process.

Reconfigurable capacitors have been designed in IBM SiGe BICMOS 6HP process to be used for VCO and RF filter designs. The capacitor design concept is almost same with the ones in TSMC process, which are fabricated and characterized. The interdigitated fingers on the beams were removed to reduce the potential of contact between electrodes. Fig 3 shows a layout view of the design in IBM SiGe process.

FREQUENCY HOPPING RF FILTER DESIGN

A wideband RF filter has been designed that switches between two resonant frequencies by reconfiguring a MEMS capacitor between its engaged and disengaged states. The RF filter topology is a π-network, shown in Fig 4. The two resonant frequencies chosen for the design are 1.2 GHz and 2.1 GHz, with a fixed inductor value of 14 nH. The dc-blocking capacitors switch from 170 fF to 400 fF, and the tank capacitors switch between 140 fF and 800 fF. These values are chosen to provide minimal difference in the filter S_{21} response at the two resonant frequencies.

The filter layout has electrical and mechanical symmetry as shown in Fig 5. The SiGe BiCMOS 6HP inductors use the topmost metal layer. Undercutting of the silicon beneath the inductors is planned to increase their quality factor [10]. The inductors are mounted in a metal frame for compatibility with the CMOS micromachining process [5]. A corrugated frame is used to minimize eddy current losses.

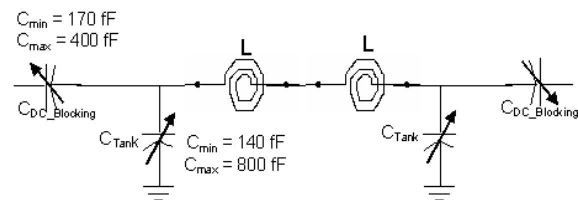


Fig. 4: RF filter π-network topology. Capacitors are reconfigurable MEMS capacitors.

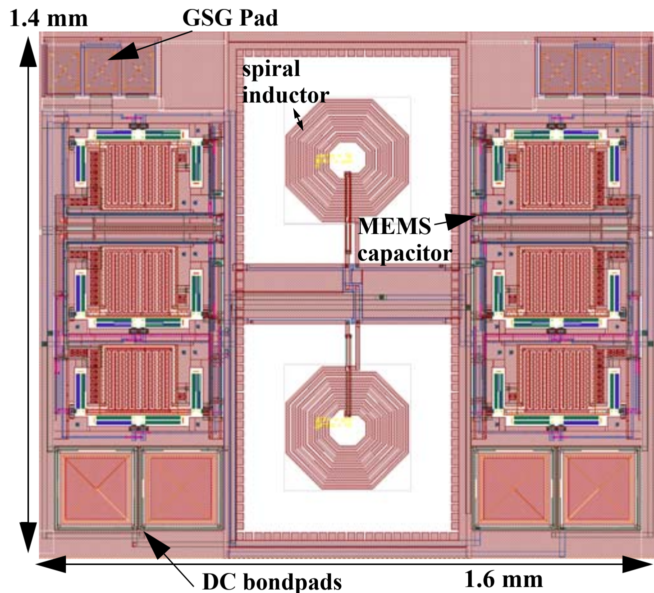


Fig. 5: RF filter layout comprised of wo suspended spiral inductors (37%) and four MEMS capacitors two of which are partitioned into an array of two building block capacitors (40%) with remaining area devoted to I/O pads.

The AC response of the filter with both the maximum and minimum capacitance values is shown in Fig 6. The filter has been designed to minimize the difference in insertion loss at the two frequencies of interest. The observed difference of 2.8 dB is not significant for application in dual-hop architecture, for which the filter has been designed. The simulations do not take into account the higher Q expected from suspending the inductors. For comparison, an RF filter has been designed using NMOS varactors. The AC response is shown in Fig 7. The varactor-based design has a higher insertion loss, and a limited tuning range. Additionally, optimal performance cannot be achieved as the DC blocking capacitors cannot be made tunable for the best insertion loss at both operating frequencies. This is because the MOS varactor is a two terminal device and the reconfigurable MEMS capacitor is a four terminal device.

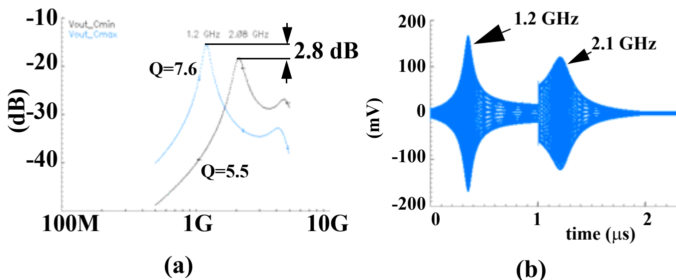


Fig. 6: (a) AC response of filter at both frequencies of interest and (b) transient response of filter showing reconfiguration at 1 μs.

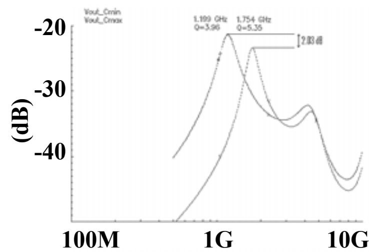


Fig. 7: AC response of filter by using NMOS varactors.

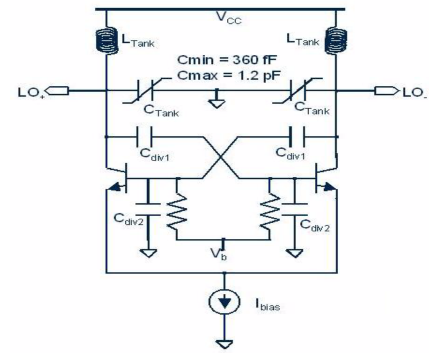


Fig. 8: Schematic of the frequency-hopping oscillator.

FREQUENCY-HOPPING VCO DESIGN

A frequency-hopping VCO has been designed which hops between 1.2 GHz and 2.1 GHz through voltage-controlled reconfiguration of MEMS capacitors. Fig 8 shows the standard symmetric cross-coupled implementation of the VCO core to cancel the tank losses [9]. The inductors used in the tank have their substrate etched to enhance their quality factor [10]. The MEMS tunable capacitors form the capacitive part of the tank. Since the bipolar implementation suffers from low voltage swing, a capacitive divider, consisting of 90 fF Metal-Insulator-Metal (MIM) capacitors, has been placed between the drain and gates of the transistors.

Since the 1/f noise of the bipolar transistors is less than its MOS counterpart, the predominant concern in the design is the down-converted white noise. Care is taken to minimize the $1/f^2$ phase noise contributed by the resistors that bias the core. Increasing the bias current increases both the carrier power (which decreases the phase noise) and the BJT shot noise (which increases the phase noise). To find the optimum bias current, provisions are made to vary the bias current externally. SpectreRF simulations show a phase noise of -109 dBc/Hz and -112 dBc/Hz at 600 kHz offset from the carrier at 2.1 GHz and 1.2 GHz respectively. The core power consumed is 2.25 mW and 3 mW respectively. An emitter follower buffer is used to drive the 50 Ω load of the GSG probe. The output buffer is designed to deliver 0 dBm to the load. Fig. 9 shows the simulated switching between the the 1.2 GHz and 2.1 GHz frequencies by changing the control voltage to the MEMS reconfigurable capacitors at 15 ns.

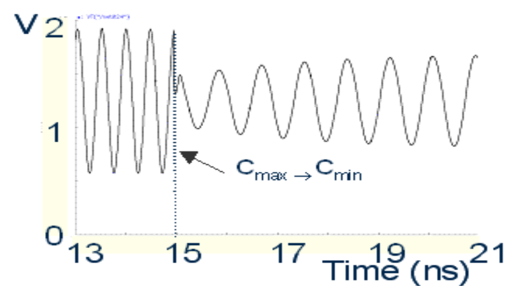


Fig. 9: Oscillator output hops in frequency at 15 ns through reconfiguration of MEMS capacitors.

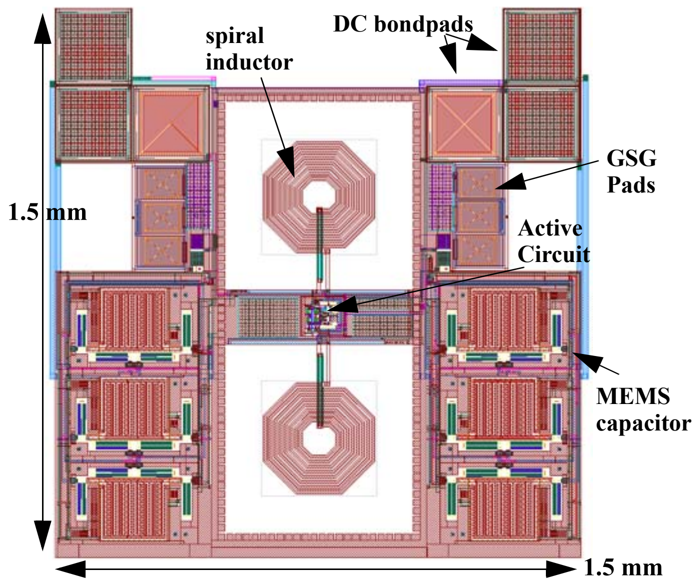


Fig. 10: VCO layout with two suspended spiral inductors (40% — also includes active circuit) and two MEMS capacitors each partitioned into an array of three building block capacitors (37%) with remaining area devoted to I/O pads.

Fig 10 shows the layout of the VCO. The output buffers are placed near the GSG probe pads to minimize the parasitic capacitance to the substrate. The inter-wiring capacitance to ground in the tank is also minimized as that would decrease the VCO tuning range. Effort is also made to ensure the symmetry of the balanced circuit during layout. The area occupied by the layout as shown in Fig 10 is 1.5 mm x 1.5 mm. As a comparison, a VCO was designed based on accumulation region MOS varactors, for operation at the same bias current as the reconfigurable MEMS capacitor-based design. The simulated phase noise (at 600 kHz offset from the carrier) when the oscillator is configured for 1.2 GHz operation is -93 dBc/Hz; at 2.1 GHz the phase noise is -95.5 dBc/Hz. These results illustrate the lower loss associated with the reconfigurable MEMS capacitor.

The RF filter and VCO designs have been fabricated in IBM SiGe 6HP (a die shot is shown in Fig 11). Following post-foundry micromachining, the filter and oscillator will be characterized. A wideband LNA that interfaces with the fiter and oscillator set the target frequency for this design. Also included on the chip are test structures to extract the residual stress gradients needed for optimization of the electro-thermal actuators controlling the MEMS reconfigurable capacitor.

CONCLUSIONS

CMOS-compatible RF-MEMS reconfigurable capacitors have been integrated with suspended inductors to form a RF filter and VCO, which hop between 1.2 and 2.1 GHz. For diode or MOS varactors, the tuning range and Q factor (insertion loss and phase noise) have to be traded-off with each other. The reconfigurable RF MEMS varactor eliminates this trade-off, since its Q factor is constant (determined by layout). The post-CMOS micromachining used to fabricate the reconfigurable capacitor can also be used for suspending the inductor (for improved Q). Designs targetting a wider frequency range, with reconfiguration to multiple bands are currently under way.

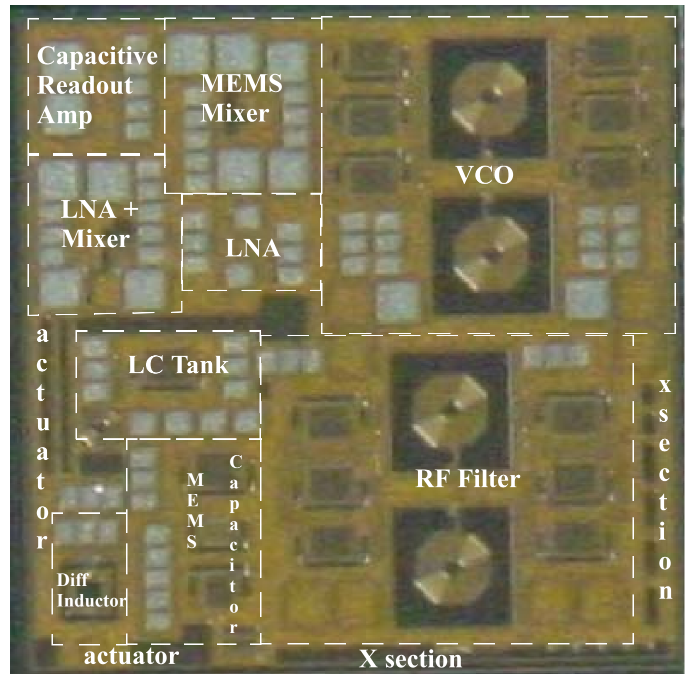


Fig. 11: Die shot of fabricated SiGe 6HP chip showing the oscillator on the top right, the RF filter in the bottom right, a wideband LNA with MEMS mixer-filters in the top left and a variety of test structures for RF MEMS capacitor characterization in the bottom left.

Acknowledgement

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