Micromachined High-Q Inductors in 0.18μm Cu Interconnect Low-K CMOS Process

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ABSTRACT

Spiral inductors fabricated in a 0.18μm 6-level Cu interconnect low-K dielectric process suspended 100μm above the substrate with sidewall oxide removed are described. A maskless post-CMOS micromachining process has been developed for the low-K dielectric copper interconnect process. Post-CMOS process enhancements of inductors provide higher quality factors and self-resonant frequencies by undercutting silicon to eliminate substrate losses and etching inter-turn dielectrics to reduce self-capacitance. The micromachined inductors have significantly greater quality factor at higher frequencies extending the operational frequency range. Quality factors of greater than 7 were obtained at 5.5 GHz for inductors with silicon undercut and inter-turn oxide removed, while Q was 5.5 at 2.5 GHz for inductors having only their inter-turn oxide removed.

INTRODUCTION

Advances in CMOS process technology is enabling integration of greater RF functionality in system-on-chip solutions. Substrate losses limit the performance of inductors at higher frequencies. Research has focussed on improving the Q factor of CMOS inductors by using custom process modules. These include fabrication of inductors with thick copper layers on Saphire substrates[1], and removal of the underlying silicon by wet etchants [2][3]. The approach suggested in this paper differs from the above that is does not require any additional masks and the fine line geometry structures can be defined due to the 2 step dry etching.

The Carnegie Mellon University MEMS group has developed a maskless post-CMOS fabrication process to integrate micro-mechanical structures along with CMOS circuits[4][5]. Previously this micromachining process has successfully been demonstrated on three generations (0.8μm, 0.6μm, 0.35μm, 0.18μm) of CMOS processes. The post fabrication recipe has been modified to work with Cu-interconnect and low-K dielectric of the modern CMOS processes. Combining the advantages of Cu interconnect technology with the CMOS micromachining process, it is possible to design high performance RF passive components. A combination of high speed transistors and low interconnect resistance in the United Microelectronics Corporation (UMC) process[6] with suspended low substrate loss inductors enable design of high performance RF circuits.

Inductor design is improved by post-CMOS micromachining as the inductor can be suspended 100μm over the substrate. Copper is more inert to erosion and oxidation than aluminum; this property is advantageous especially for the post-CMOS RIE process. The top metal layer used as a mask for the micromechanical structure is milled by 0.5μm in the Al interconnect process, resulting in increased in sheet resistance of about 30~40% for that layer. This loss is unacceptable since this layer will be used as inductor wire. The increased resistance of the aluminum top layer reduces the quality factor of the inductor.

CMOS MICROMACHINING PROCESS

A 0.18μm 6-metal-level Cu interconnect Low-K dielectric process[6] was used to fabricate define the CMOS circuits and the inductors. The interconnect thickness for the process are metal 1,2 0.3μm, and metal 3-6, 0.45μm. The low-K dielectric has a dielectric constant of 3.7. The process flow, shown in Figure 1, enables fabrication of micromachined structures in CMOS. The conventional CMOS processing is followed by an anisotropic reactive-ion etch (RIE) with CHF_3 and O_2 to etch away oxide not covered by any of the metal layers, resulting in high-aspect-ratio vertical sidewalls. A combination of anisotropic and isotropic silicon etching in a STS Deep Reactive Ion Etching (DRIE) removes the underlying silicon, thus releasing the microstructure[9].

In the Cu process, The metal-layer thickness reduces less than 0.2μm after the post processing. The post-processed Cu inductors are better than the aluminum inductors with same starting sheet resistance. The lower resistance of the all copper via also helps reduce the DC resistance of the inductor. The lower dielectric constant of the oxide layers reduces the parasitic capacitance leading to higher self resonant frequencies.

The micromachined structural elements are formed by a sandwich of metal and dielectric layers. Due to the differences in residual stress of the two layers, the structures exhibit out-of-plane curl. The Copper interconnect structures have lower out-of-plane curl compared to that of Al interconnect structures. The radius of curvature out of plane is inversely proportional to the flexural rigidity[7].The flexural rigidity, the product of Youngs Mod-

ulus and Moment of Inertia is higher for the Cu beams as the Youngs Modulus of Cu is 130 GPa, about 1.9 times that of aluminum[8]. This produces beams that are much stiffer. Also, the thickness of beams using all metal layers is 6µm in the Cu process compared to 4.5µm of a 3-metal Al process (HP0.5µm) process. This increases the out-of-plane bending moment of inertia by a factor of 2.3.[9]

INDUCTOR DESIGN

The inductor topology is shown in Figure 2. To minimize the coil resistance and maximize the Q within the smallest area, all metal layers are utilized. The top two metal layers (Metals 6-5) act together as a single wire about 0.7µm in thickness and compose the inductor plus an output port; the other layers (Metals 4-3-2-1) act as another output port wire about 1.5µm in thickness. The thickness of the top-most metal layer was reduced by 0.2µm due to ion milling during the anisotropic silicon etching. The inductors were designed with an expected metal 5-6 combined thickness of 2µm, however due to process issues thinner top metals were obtained. Better process optimization can reduce this metal thickness degradation. The width of all the wires used is 20µm. The inductance value were calculated using FASTHENRY[10]. The metal layers are connected through stacked vias as illustrated in Figure 2.

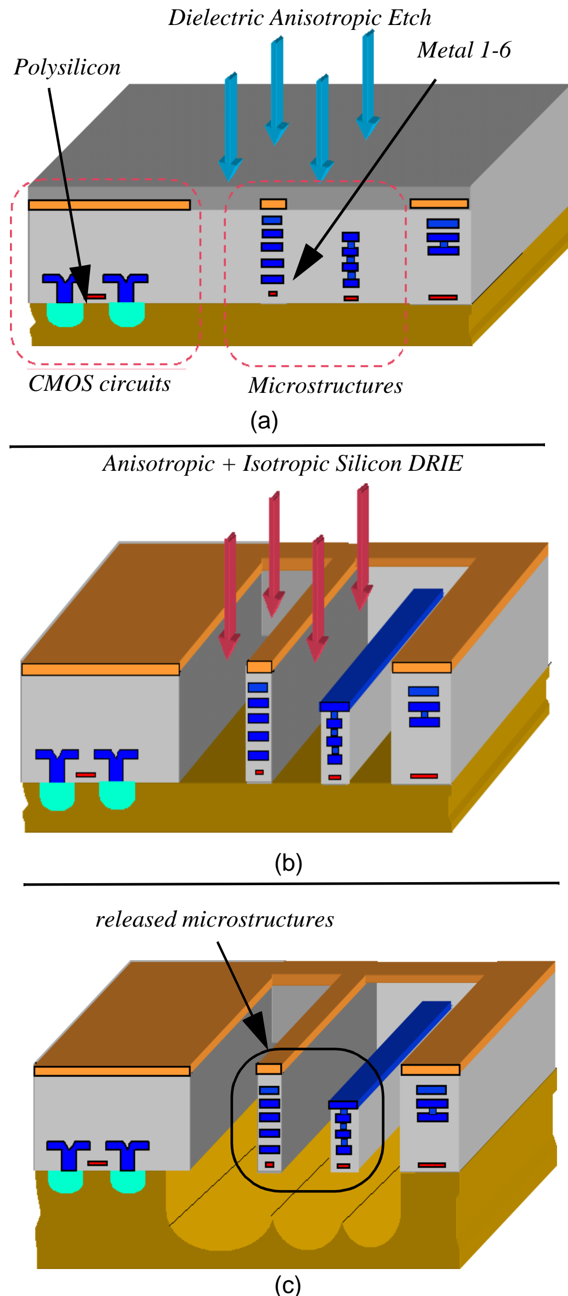

Figure 1. Cross sections of device in each stage of the process flow.
(a) Device after CMOS processing.
(b) After anisotropic etch of isolation layers.
(c) After anisotropic and isotropic Si etch to release the mechanical structure.

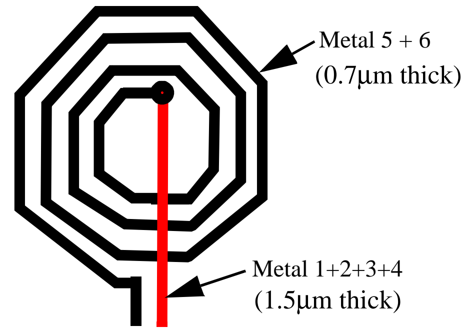

Figure 2. (Schematic of the inductor design. It consists of 4 turns. The spiral represents Metal 6 and 5 in parallel. The lower line represents Metal 4, Metal 3, Metal 2 and Metal 1 in parallel. The dot represents contact vias between Metal 6, Metal5, Metal 4, Metal 3, Metal 2 and Metal 1.

INDUCTOR CHARACTERIZATION

The inductance and Q factor of the devices was derived from 2-port S-parameter measurements. Measurements were made using GSG waveguide probes connected to a HP8752 network analyzer from 50MHz to 20GHz. Probe calibration was done by a CS-5 calibration substrate and the probe pads were de-embedded by making measurements on dummy pad structures (open and short). SEM of the oxide + silicon released inductor is shown in Figure 3.

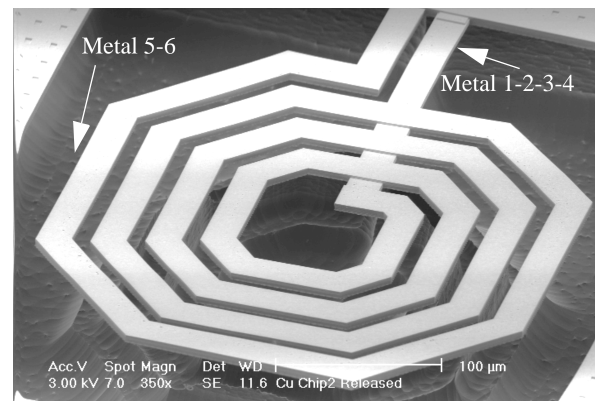

Figure 3. SEM of an oxide + silicon released inductor.

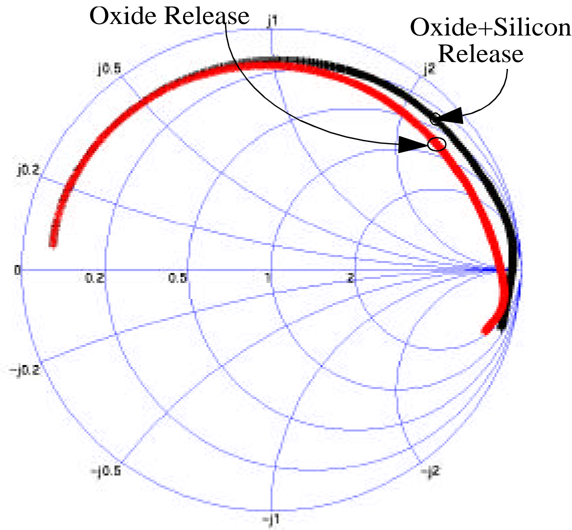

Figure 4. Comparison of S11 characteristics of inductor with oxide removed and oxide removed+silicon released.

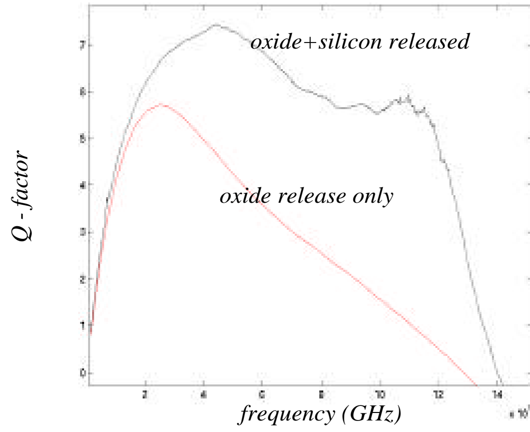

Figure 5. Comparison of Q of the oxide released and oxide removed and silicon released inductor (L1).

Measurements were made on four sizes of octagonal inductors with inductances ranging from 3.1nH to 4.4nH on 2 chips, one with oxide removed (N1-4) and the other with the oxide removed and the silicon (B1-4) released. Comparison of the S11 parameters for inductor B1 and N1 are shown in Figure 4. A comparison of the quality factor of the two inductors is shown in Figure 5. The substrate undercut inductor exhibits a higher quality factor above 1.5 GHz. At low frequencies, losses due to the DC resistance dominate[11], and the quality factor is about the same for both the inductors. The substrate losses that dominate at higher frequencies are reduced by the silicon removal. The substrate under-cut inductor can be modeled by the lumped parameter circuit model for the released inductor is shown in Figure 6. C_p is the parasitic capacitance due to the return port crossover the inductor. R_{dc} is the DC resistance of the inductor. The skin effect and the current crowding effects are modeled by expressing the series resistance, R_d, of the inductor as

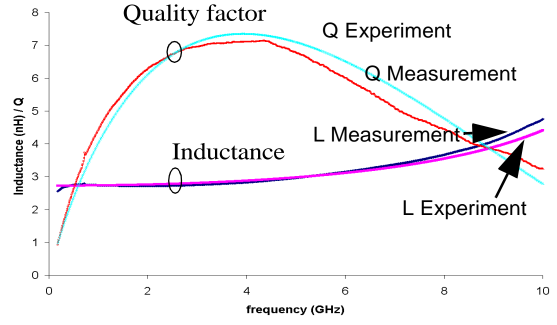

Figure 7. Comparison of Q factor and inductance from model to experiment for inductor L1.

$$R_d = R_{dc}e^{\sqrt{\frac{f}{f_{crit}}}} \quad (1)$$

R_s and C_m are used to model the frequency dependence of the substrate losses. This simplified model holds up to 10GHz, the intended range of operation of the inductor which is relevant to circuit designers.

Table 1: Summary of inductor model parameters

Model Parameter	B1	B2	B3	B4
L (nH)	2.82	3.60	3.87	4.41
C_p (fF)	36.5	37.5	41	47
R_{dc}(Ω)	2.53	3.33	3.53	4.23
R_s (Ω)	1500	2100	2300	2900
f_{crit} (GHz)	4.1	4.1	4.1	4.1
C_m (fF))	3	3.3	3.3	3.6
Q_{max}	7.5	7.25	7.3	7.0
f @ Q_{max} (GHz)	4.4	5.0	5.4	5.2
f_{res}(GHz)	13.9	12.0	11.3	10.9

Table 1 summarizes the performance of the four inductors measured. The values of the Q factor with frequency for the various inductors is shown in Figure 7 Comparison of the performance of the inductors with oxide removed and inductors with oxide removed (N1-4) and silicon released (B1-4) inductors is shown in Table 2. There are no significant differences in the self resonance frequencies of the two types of inductors. This is mainly due to the removal of the oxide in both the cases. The inductances after removal of the silicon is lowered by

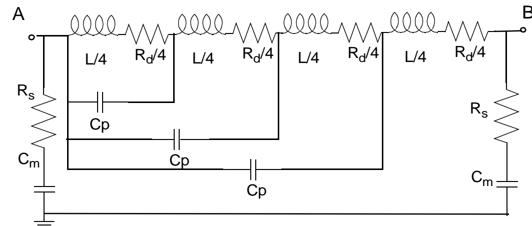

Figure 6. Lumped parameter circuit model of the silicon and oxide released inductor.

about 10%. This is due to removal of the silicon and out-of-plane curl that reduce flux linkage between turns.

RELAIBILITY OF SUSPENDED STRUCTURES

For application of this technology in commercial devices the reliability of the suspended inductor after release was verified. The entire die was covered by metal 6 to protect the circuit etching. The removal of the cover glass exposed the top metal to the ambient. This is a concern for long term reliability due to possible environmental corrosion. The released chip was placed in an environmental chamber at 70°C, with 90% humidity for 24 hours. No significant metal corrosion was observed. The chips were wire bonded using the same equipment and settings as the aluminum chips.

CONCLUSION

A maskless post CMOS micromachining technique for possible application to fabrication of higher frequency RF applications has been developed. This technology can also be applied to minimize RF crosstalk through the conductive silicon substrate as suggested in [2]. Monolithically integrated IC inductors in aluminum interconnect CMOS devices have reported with maximum Q factors of about 10 after using thick top metal layer. The quality factor degradation due to substrate losses at higher frequency make it difficult to extend the operating frequency to beyond 4 GHz. A combination of copper interconnect for lower DC resistance and the maskless micromachining technology can deliver higher Q factors at higher frequencies. Simulations indicate that Q factors can be increased to over 20 if 2μm of Cu is used for the spiral coil.

Table 2: Comparison of Oxide removed and Oxide and Silicon released inductors

	L1		L2		L3		L4	
Parameter	**B1**	**N1**	**B1**	**N1**	**B1**	**N1**	**B1**	**N1**
L_m (nH)	2.82	3.05	3.60	3.97	3.87	4.27	4.41	4.9
R_{dc} (Ω)	3.25	3.75	4.3	4.25	4.8	5.25	5.25	5.8
Q_{max}	7.5	5.5	7.25	5.7	7.3	5.4	7.0	5.1
ft_{max} (GHz)	4.4	2.6	5.0	2.5	5.4	2.5	5.2	2.4
f_{res}(GHz)	13.9	13.5	12.0	12.3	11.3	12.0	10.9	10.5
Area ($x10^{-8}$ m^2)	9.61	9.61	10.5	10.5	10.5	10.5	11.6	11.6

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REFERENCES

1. J. N. Burghartz, D. C. Edelstein, K. A. Jenkins and Y. K. Kwark, “Spiral inductors and transmission lines in silicon technology using copper-damascene interconnects and low loss substrates,” *IEEE Transaction on Microwave theory and techniques*, Vol. 45, No. 10, October 1997, pp.1961-1968.
2. K Ng, N. Pham, L. Sarro, B. Rejaei, J. Burghartz “Characterization of a Bulk-Micromachined Post-Process Module for Silicon RF Technology” 2000 Topical Meetings on Silicon Monolithic Integrated Circuits in RF Systems. pp 99-102 April 2000
3. J. Y. C. Chang, A. A. Abidi, and M.Gaitan, “Large suspended inductors on silicon and their use in a 2 μm CMOS RF amplifier,” *IEEE Electron Device Letters*, Vol. 14, No. 5, May 1993, pp.246-248.
4. G. K. Fedder, S. Santhanam, M.L. Reed, S.C. Eagle, D.F.Gulliou, M.S.-C. Lu, L.R.Carley, “Laminated high-aspect-ratio microstructures in a conventional CMOS process,” *Sensors and Actuators*, A57, pp.103-110 (1996).
5. US Patent 5717631, “Microelectromechanical structure and process of making same”.
6. United Microelectronics Corporation WWW address: http://www.umcgroup.com
7. H. Lakdawala and G.K. Fedder, “Analysis of Temperature-Dependent Residual Stress Gradients in CMOS Micromachined Structures”, Transducers 99, Sendai Japan
8. CRC Handbook of Chemistry and Physics, 77th Edition 1996-1999
9. X. Zhu, D. W. Greve, R. Lawton, N. Presser, G.K. Fedder, “Factorial experiment on CMOS-MEMS RIE post processing”, in Proc. of the 194th Electrochemical Society Meeting, Symposium on Microstructure and microfabricated system, Boston, MA, Nov. 1-6th, 1998, pp.41-44.
10. FastHenry User Manual, software available for download at ftp://rle vlsi.mit.edu/pub/fasthenry/
11. W. Kuhn, N. Ibrahim, “Approximate analytical modeling of current crowding effects in multiturn spiral inductors”, 2000 IEEE MTT-S International Microwave Symposium Digest, pp 405-8, June 2000