Layout Extraction for Integrated Electronics and MEMS Devices

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SUMMARY

Lumped parameter simulators are increasingly being used for schematic-based MEMS design. However, as layout continues to be the design representation of choice for MEMS manufacturing, layout verification is crucial. Schematic-based simulation tools can be used for this verification through the extraction of the schematic from the layout representation. Furthermore, integrated MEMS needs combined extraction and simulation of conventional electronics and electromechanical components in order to correctly capture the interaction between these components. This paper introduces the concept of mechanical parasitics, which, when combined with electrical parasitics, enables the accurate verification of integrated electronics and MEMS devices.

Keywords: CMOS micromachining, integrated MEMS extraction, micromechanical parasitics

INTRODUCTION

Integration of MEMS sensing and actuation with electronics is drawing increasing interest in the development of mixed-domain devices. Layout verification of such devices is no longer possible using the classical approach of solid modeling, meshing, and continuum simulation, as electronics and electromechanics cannot be simulated simultaneously. Instead, layout verification has to rely on layout extraction [1] followed by schematic-based mixed-domain simulation [2]. The accurate capture of the entire layout in the form of a schematic requires the extraction of the mechanical parasitics in the mechanical and electromechanical layout areas and the electrical parasitics in the electromechanical and electronic layout areas. Designers have long used manual extraction of electrical parasitics in the electromechanical-electronic interface, particularly for the domain of capacitive transducers [3]. This paper proposes the use of mechanical parasitics, in conjunction with electrical parasitics for verification of the design. Additionally, we present an extractor that automatically extracts the parasitics of the integrated MEMS device using hints from a Layout Parasitic Extraction (LPE) technology file.

This paper focuses on the CMOS micromachining process [4] as a representative integrated MEMS process. The standard CMOS process is followed by two maskless dry etches to release the microstructure protected by the top-most metal layer. Cross-sections of the microstructure during various points in the CMOS post processing are shown in Fig1.

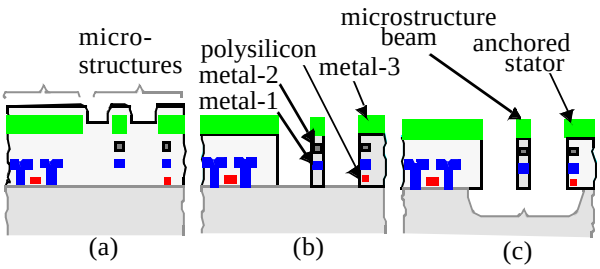

Fig 1: *Cross-section of CMOS micromachining process [4]; (a) after standard CMOS process, (b) after anisotropic etch, (c) on final release using isotropic etch*

PARASITICS IN INTEGRATED MEMS

The added flexibility in electrical connectivity within the MEMS components and the presence of mechanical and electrical parasitics in the CMOS micromachining process [4] leads to a significantly more complex extraction problem than in polysilicon MEMS [1]. Mechanical parasitics that more accurately capture lay-

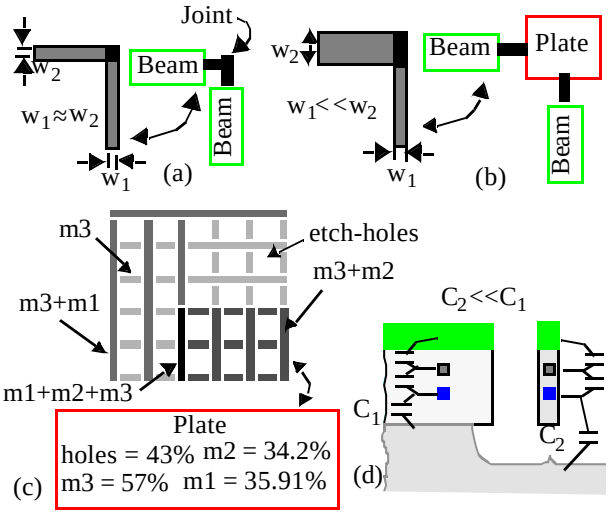

Fig 2: *Electrical and mechanical parasitics: (a) a joint between two nearly equal beams neglected in the model, (b) a joint between two beams of different aspect ratios modeled as plate to account for its parasitic effects, (c) layout of plate area in MEMS and corresponding schematic with parasitic values, (d) parasitic capacitances*

out details for schematic simulation include the effect of parasitic mass in the plates and the effect of parasitic joints between beams. Parasitic joints (Fig2(a), (b)) occur between beams which differ significantly in their widths. Such joints need to be modeled using plate elements to accurately capture the transfer of moments between the beams. Parasitic mass in plates (Fig2(c)) results due to routing in lower metal layers (topmost metal layer defines the structure) and also from the etch-holes in the plate. Electrical parasitic capacitances (Fig2(d)) in MEMS areas tend to affect the interface between MEMS and circuits and hence need to be accurately captured in the integrated schematic. While estimating the parasitic capacitance in the MEMS areas the gap between the substrate and the suspended structures, due to the release etch, needs to be taken into account. These process related information can be encoded into the LPE file which can then be used by the extractor to reconstruct an integrated schematic together with all the parasitic information.

EXTRACTION FLOW

The current extraction methodology is capable of recognizing the MEMS and electronics components of integrated MEMS layouts and uses two separate extractor modules, an improved MEMS extractor and a commercial electronics extractor, to generate schematic representation [5] for both components. The top-level master-extractor 'stitches' the two extracted schematics together to obtain a combined schematic which accurately captures the parasitic effects and their interactions.

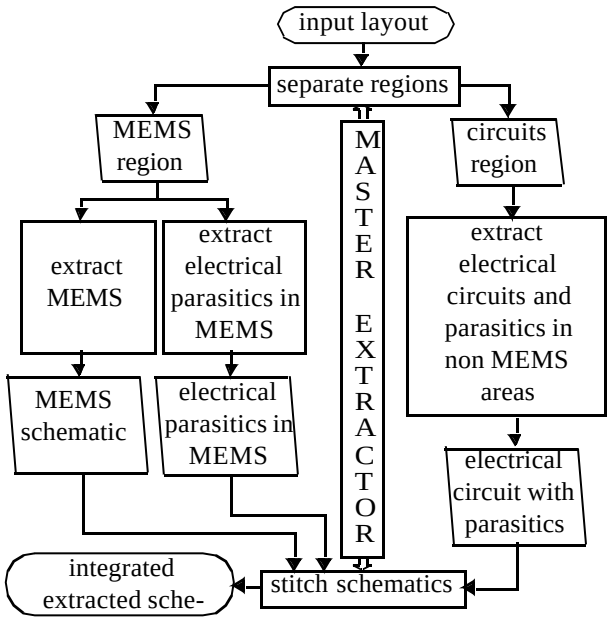

Fig 3: *Overall extraction flow*

The overall extraction flow is shown in Fig3.

RESULTS

This section presents an in-depth study of the effects of mechanical and electrical parasitics observed in two representative examples. The first example (an accelerometer) shows how integrated simulation leads to better designs. The second example (a filter) shows a comparative study between the results from designed schematic, extracted schematic and experimental data.

Accelerometer

Consider the CMOS-MEMS *y*-accelerometer [6] with an on-chip capacitive sensing interface. The initial design uses a differential comb drive on each side of the accelerometer as the electromechanical transducer (Fig4(a)). When the integrated schematic was simulated, a cross axis signal was observed (experiment 1 of Table1). This can be explained from the dc voltage on the sense fingers of the comb drives, resulting from the sense circuit's operating point, which results in an unbalanced moment. This moment leads to a dc displacement in the *x* and *y* directions and in turn causes the cross axis coupling. To verify this effect, the MEMS schematic (without the circuit) was simulated with different dc voltages on the sense fingers. The results plotted in Fig4(c) show the effect of a dc voltage on the sense finger. The dependence on the dc voltage can be removed if the common centroid topology (shown in Fig4(b)) is used. Such an arrangement leads to complete balancing of the forces

Table 1: *Results for accelerometer when a 1g input pulse acceleration was applied in y direction (D_{ma} stands for MEMS designed schematic with single comb drive, D_{mb} stands for common centroid MEMS schematic, D_{ca} stands for designed schematic for circuit, E_{ca} stands for extracted schematic for layout using metal2 for wiring sense comb, E_{cb} stands for extracted schematic for layout using metal1 layer for wiring, E_{ma} stands for extracted schematic for the MEMS part of common centroid design)*

Experi-ment	Circuit MEMS	x displacement (fm)	y displacement (nm)	o/p of sense circuit (mV)
1	D_{ca} D_{ma}	1.63	5.37	4.44
2	D_{ca} D_{mb}	0	5.37	4.44
3	E_{ca} E_{ma}	47.82	5.03	4.12
4	E_{cb} E_{ma}	47.82	5.03	4.16
5	D_{ca} E_{ma}	47.82	5.03	4.16

and the moments thus eliminating cross coupling (experiment 2 in Table 1) due to the circuit operating point on the comb drives.

The layout of the common centroid accelerometer (with integrated electronics) is shown in Fig5(a), with the extracted MEMS schematic in Fig5(b). Comparison between the results of designed and extracted schematics (experiments 2 and 3) show a 6.3% degradation in *y* displacement and 7.2% degradation in the output. This is in accordance to the sensitivity equations for the accelerometer, which are given by $y/a = k/m$ and $V_0/a = (2C_0 m V_m)/(kg_0(2C_0 + C_p))$ where, V_0 is the output voltage, a is the input acceleration, C_0 is the initial capacitance between fingers, m is the effective mass, V_m is the applied bias, C_p is the parasitic capacitance, k is the spring constant, g_0 is the initial inter-finger gap and y is the displacement in the y direction. The extracted schematic captures the actual metal1 and metal2 areas used for signal routing in the plate, leading to as smaller mass (m) than in the designed schematic. The parasitic joints (identified by the extractor) in the springs lead to a smaller spring constant (k) in the extracted schematic, as compared to the design schematic. The additional degradation in the transducer output was due to the parasitic capacitance originating primarily from the routing for the sense finger of the comb drives which was done using metal2. To reduce this parasitic capacitance, the layout was regenerated using metal1 as the routing layer (since metal1 is further away from top most metal layer which is grounded); the results are shown in experiment 4 of Table 1. The parasitic capacitance is negligible in this case which is highlighted in experiment 5 where the extracted MEMS schematic was simulated with the circuit schematic without the parasitic capacitances.

This example demonstrates the capability of the integrated simulation methodology in capturing the mutual interaction of the mechanical, electromechanical and electronic domains in an integrated device and also

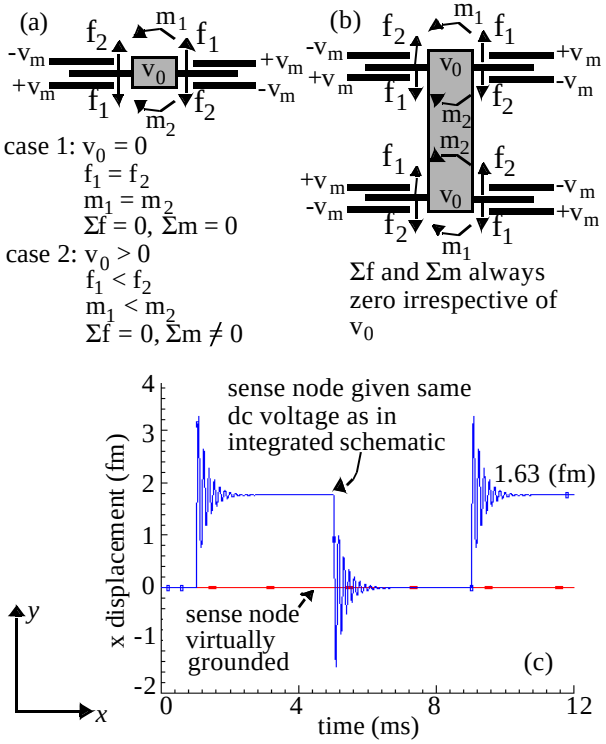

Fig 4: *(a) Symbolic picture of a rotor (center) with differential comb drive showing all the forces and moments due to a dc voltage on the sense finger, (b) arrangement of four comb drives to remove moment due to dc voltage, (c) cross axis displacement for 1g input pulse with and without dc voltage at the sense node of the MEMS schematic in (a)*

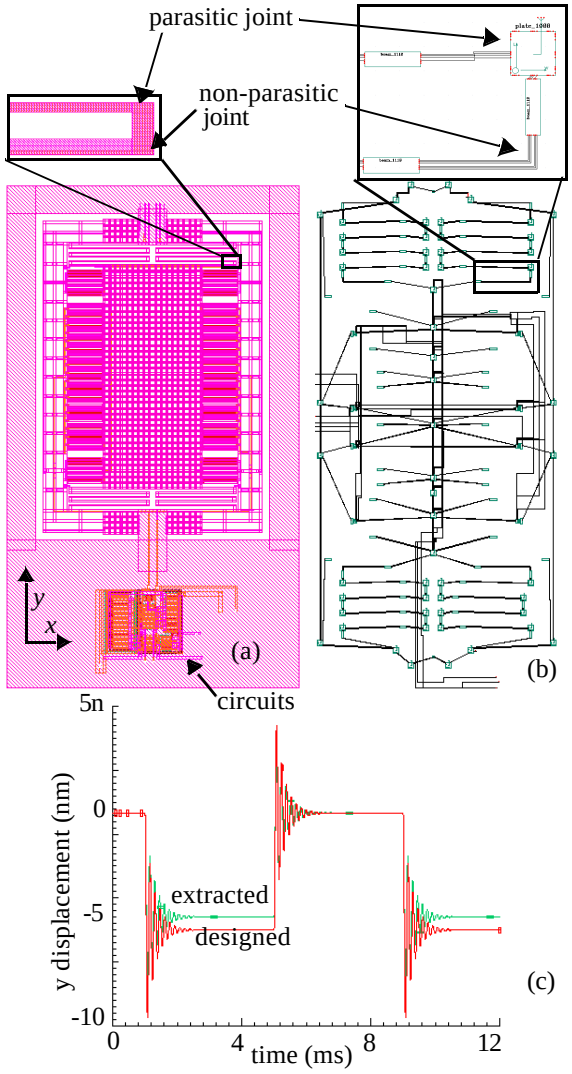

Fig 5: *CMOS accelerometer: (a) layout, (b) extracted schematic, (c) y displacement for 1g input pulse in the y direction*

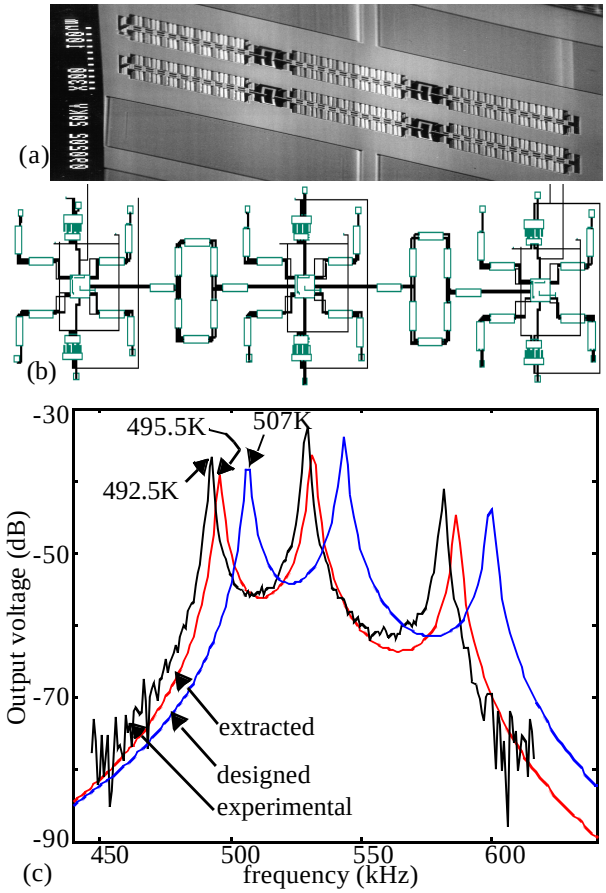

Fig 6: *(a) SEM of the filter, (b) extracted schematic, (c) comparison of results*

shows the usefulness of the extractor in capturing the various parasitics.

Filter

Fig6(a) shows an SEM of a CMOS-MEMS band-pass filter [7] with an on-chip electrical interface. The frequency responses of the extracted schematic (Fig6(b)) and the designed schematic are shown in Fig6(c) together with the experimental data [7]. Table2 shows the details of the simulation results for the first resonant peak. The additional routing mass resulted in a decrease in the resonant frequencies by 2% while increasing the overall displacement at the resonant peaks by the same factor. However the effect of parasitic capacitance at the sense comb drive dominates and results in an overall degradation of the output by 15.4%.

Table 2: *Comparison of data for the first resonant peak in the band pass filter for the designed and extracted schematics (ac i/p 1V, bias ±20V)*

	o/p voltage (mV)	transducer o/p (mV)	displacement (nm)	resonant frequency (kHz)
designed	12.86	86.24	32.09	507
extracted	10.88	72.98	36.74	495.5

CONCLUSION

Integrated simulation is essential to capture the true behavior of a device containing MEMS and electronics. Such a simulation can only be performed at the schematic level. This paper introduces the concept of mechanical parasitics that are needed in addition to electrical parasitics in order to accurately represent the device layout as a schematic. An extractor has been presented which uses a Layout Parasitic Extraction (LPE) file to automatically generate an integrated schematic representation from the layout. Examples showing how the extractor can be used to identify and minimize the impact of deleterious parasitics were presented.

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REFERENCES

[1] B. Baidya et al, "MEMS Component Extraction," *Proc. MSM '99*, p. 143-6.

[2] G.K. Fedder, Qi Jing, "A Hierarchical Circuit-Level Design Methodology for Microelectromechanical Systems," *TCAS II*, v. 46, no. 10, Oct. 1999, p. 1309-15.

[3] K. Wang, C.T.-C. Nguyen, "High-Order Micromechanical Electronic Filters," *Proc. IEEE Int. Workshop on MEMS*, 1997, p. 25-30.

[4] G.K. Fedder, et. al, "Laminated high-aspect-ratio micro-structures in a conventional CMOS process," *Sensors & Actuators*, v. A57, no. 2, p. 103-10.

[5] B. Baidya, T. Mukherjee, "Challenges in CMOS-MEMS Extraction," *Proc. of MSM'01*, p. 108-11.

[6] H. Luo, G.K. Fedder and L.R. Carley, "A 1mG Lateral CMOS-MEMS Accelerometer," *Proc. of MEMS '00*, p. 502-7.

[7] Q. Jing, et. al, "CMOS micromechanical band-pass filter design using a hierarchical MEMS circuit library," *Proc. of MEMS '00*, p. 187-92.