Copper Interconnect Low-K Dielectric Post-CMOS Micromachining

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ABSTRACT

A post-CMOS maskless dry etch process has been developed to fabricate MEMS structures compatible with commercial low-k copper interconnect processes. The micromachining in the copper low-k process enables the fabrication of an RF inductor with quality factor of 12 at 7.5 GHz and a variable capacitor operating up to 3GHz. Reduction of fluorine concentration in the plasma for the low-k dielectric etch solves the metal delamination problems. Argon/oxygen plasma cleaning of fluorine residue from the copper surface greatly reduces the metal erosion when exposed to high humidity.

Keywords: copper interconnect, low-k dielectric, post-CMOS micromachining

INTRODUCTION

In modern CMOS processes, interconnect delays begin to dominate overall device delays starting at 0.18 µm gate length. In order to achieve higher speed and less power consumption, which is limited by the resistance of the metal wires that connects transistors and the capacitance between the wires, the semiconductor industry is moving from Al interconnect SiO_2 dielectric technology to Cu interconnect low-k dielectric processes. The obvious reasons are that copper has lower resistance than aluminum and low-k dielectrics have lower capacitance than SiO_2 [1]. By developing post-CMOS micromachining for these Cu low-k processes, new MEMS devices can take advantages of the high conductivity and electromigration of Cu and of the multilayer interconnections. High quality factor passive components for RF system-on-chip are good examples.

A six-layer interconnect in UMC 0.18 µm Cu Damascene processing is shown in Fig. 1. The post-CMOS micromachining process does not require additional masks. The fine line geometry structures can be defined by post-CMOS reactive ion dry etching, which is 100% compatible with CMOS design rules[2]. The process flow, shown in Fig.2, enables fabrication of micromachined structures in CMOS. The conventional CMOS processing (Fig. 2(a)) is followed by an anisotropic reactive ion etch (RIE) with CHF_3 and O_2 to etch the low-k dielectric, resulting in high-aspect-ratio vertical sidewalls (Fig.2(b)). The top-most Cu layers act as a mask for the microstructures. The following anisotropic etch (Fig.2(c)) and isotropic silicon etch (Fig. 2(d)) remove the underlying silicon to release the microstructure[3][4]. The anisotropic etch is used to obtain the desired spacing between the mechanical structures and the substrate. The isotropic etch undercuts the silicon beneath the microstructures. This process allows placement of circuits less than 30 µm away from the MEMS structure area.

CHALLENGES IN POST COPPER CMOS MICROMACHINING

Challenges exist when migrating post-CMOS processing from Al-SiO_2 to Cu low-K interconnect CMOS. As an etch resist mask material, Cu is harder to RIE dry etch than Al even though Cu is a softer material with a doubling in sputter yield [5]. Comparing RIE dry etch of dielectric layers on Al and Cu interconnect chips, the Cu mask etch rate is 20% that of Al in a Plasma Therm 790 chamber with CHF_3 flow at 22.5 sccm, O_2 flow at 16 sccm, processing pressure at 125mT, d.c. bias 340 V and plasma density at 0.55 W/cm^2. The explanation is the reaction products of Cu are not volatile. It is still important to control the the power of the RIE to prevent the sputtering of Cu onto the dielectric surface.

The low-k dielectrics generate problems of adhesion and reliability of microstructures. For example, Novellus fluorinated oxide (FSG, k=3.6)[6] is a fluorine

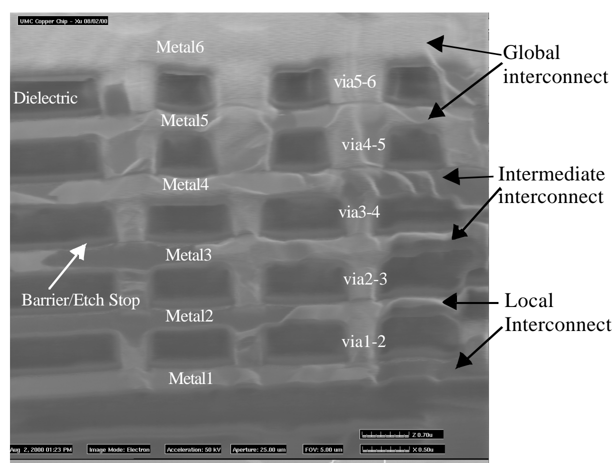


__Fig. 1.__ Six-layer interconnect in a Cu Damascene process with Cu vias.

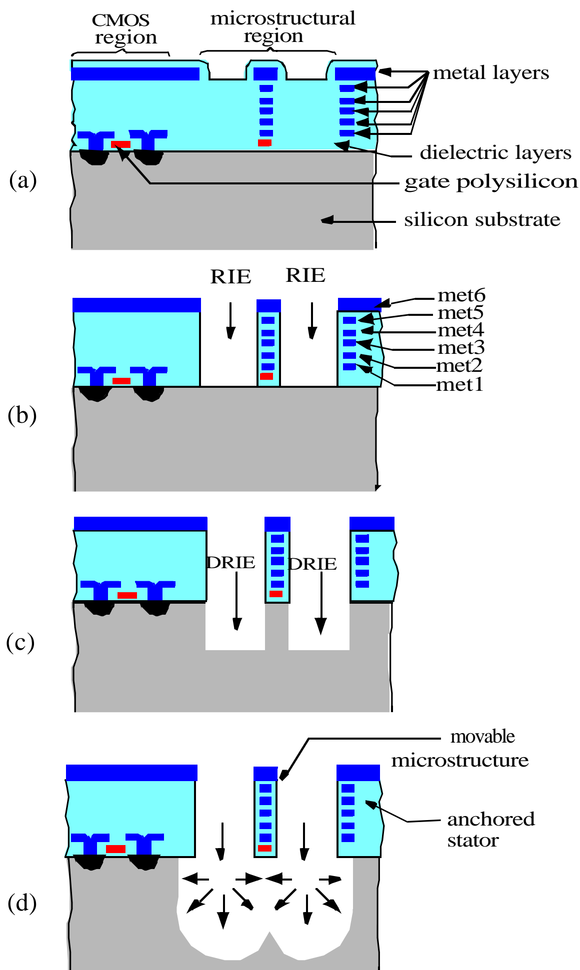


Fig. 2. *Cross sections of a microstructure in each stage of the process flow.*
(a) After CMOS processing.
(b) After anisotropic etch of dielectric layers.
(c) After anisotropic Si etch.
(d) After isotropic Si etch to release the microstructure.

enriched dielectric material. It is deposited by PECVD or HDP-CVD tools, adding silicon tetrafluoride (SiF_4) to silane (SiH_4), O_2 and argon gases [1]. The high electronegativity of fluorine atoms reduces the polarizability of the SiO_2 film, thus decreasing the dielectric constant. The downside is that fluorine may evolve from the oxide, and etch Ta/TaN/TiN barrier layers that exist to inhibit Cu diffusion into dielectric insulators. Even though the FSG can be etched as an undoped oxide, the fluorine may break the bond in the CVD film or may be generated from plasma disassociation and etch the barrier layers. This effect can cause delamination of metals in the microstructures, as shown in Fig.3, which is not seen in normal Al-SiO_2 microstructures. With the understanding of each process parameter's influence[3], the delamination issue is solved with the 50% reduction of

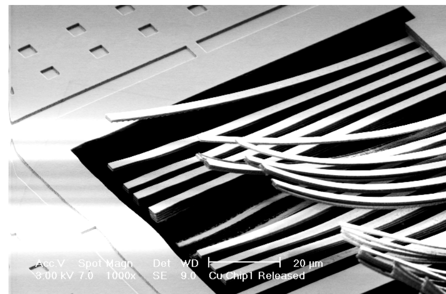


Fig. 3. *Delamination of the mechanical structures with the post-CMOS Al-SiO_2 microstructure etch recipe. The extra fluoride in the low-K dielectric causes severe delamination.*

etch rate. Doubling the O_2 flow rate and reducing the chamber pressure by 50% enhances ion bombardment and reduces fluorine reaction with the barrier layers.

Erosion of the Cu layer, shown in Fig.4, is another issue and occurs after prolonged exposure to moisture in the ambient. We hypothesize that fluoride-rich residue left from the etch produces acids when exposed to moisture of the environment and causes corrosion in the Cu. Such action is not seen in the aluminum post process due to a protective insulating aluminum oxide film that forms during the process to encase the exposed aluminum. Argon cleaning or IPA rinse after the dielectric etch significantly increases the Cu resistance to the erosion. Devices after all micromachining steps show no erosion after accelerated aging in a humidity chamber (90% humidity, 70°C) for 24 hours. The erosion rate of the Cu after the process was evaluated by four-point sheet resistance measurement of an inductor resistance, which reflects the sheet resistance change of Cu. A typical accumulated erosion curve is shown in Fig. 5. The first 20 hours contributes to most of the erosion followed by a much slower rate later. This is probably due to the fluorine-rich residue being thoroughly reacted with the Cu and not available for more etching on the surface. This is partially confirmed with the observation of chips without the cleaning procedure or coated with fluorine-rich polymers. The erosion doesn't stop on these samples even after 200 hours in humidity chamber. The correct coating material not only has to encapsulate the MEMS structures but also must not contain any chemistry which could react with Cu.

MATERIAL PROPERTIES

The curling measurements were made on two types of beams. One is made with field oxide as the most bottom layer and the other has only low-k dielectric in its entire composition. Each beam is 100 μm in length and 3.3 μm in width. The measurements were made using a interferometric optical system and are summarized in Table1. The least curled beam in the Cu process

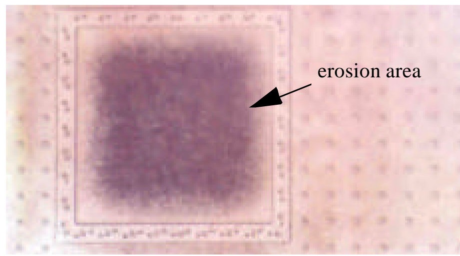


Fig. 4. *The effects of corrosion on the exposed copper surface. Shown here is a pad after 2 days exposed to the ambient.*

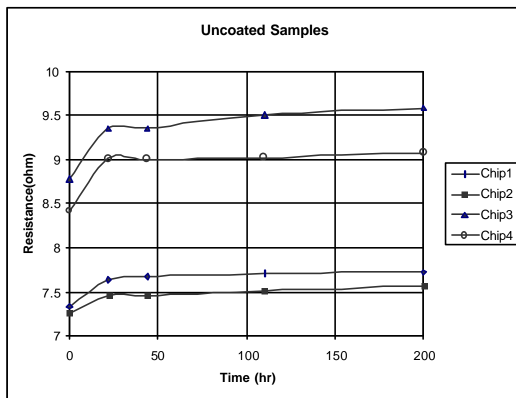


Fig. 5. Four-point measurement of the inductor resistance change (an indication of sheet resistance change) vs. the time of the inductor in the humidity chamber.

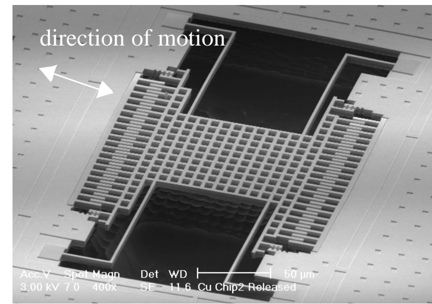
has a vertical tip deflection of 0.13 µm while that of the HP 0.5 µm Al interconnect process is about 1.5 µm.

The Young's modulus of the beam was obtained by measuring the resonant frequency of 130 µm long, 1.9 µm wide beams. A weighted average of the Cu and oxide is taken to compute the effective density in the calculation. The results are listed in Table2.

Measurements were taken of mechanical frequency response of a Cu low-k dielectric crab-leg resonator, shown in Fig.6, which is an identical design to a prior test structure in the HP 0.5 µm process. The Cu resonator has a mechanical quality factor of 70 at a frequency of 31.7kHz in the air. The aluminum structure has a resonant frequency of 41.5 kHz with a mechanical quality factor of about 40. The reduced resonant frequency is due to the higher density of the Cu.

RF APPLICATIONS

A MEMS inductor and variable capacitor for RF application is shown in Fig.7. A 50 µm silicon anisotropic etch followed by a silicon isotropic etch is used to release the microstructures from the substrate[4]. The removal of Si underneath the structures significantly reduces the substrate loss of RF components. The measurement results of the capacitor and inductor are shown



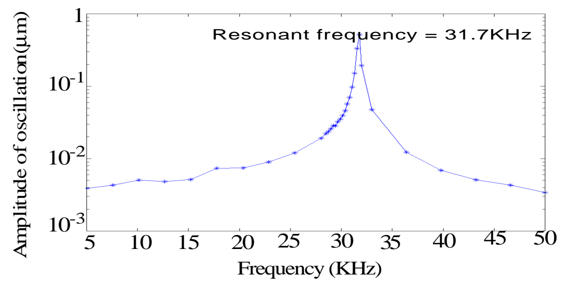


Fig. 6. *(a) Crab-leg resonator in Cu low-K dielectric interconnect process.*
(b) Frequency response of the crab-leg resonator, with 4VDC+4VAC driving voltage.

Table 1: Out-of-plane tip deflection for dielectric beams 100µm-long 3.3µm-wide(unit µm)

Beam Type	w/field oxide	w/o field oxide
M1-2-3-4-5-6	0.13	0.39
M2-3-4-5-6	1.17	1.04
M3-4-5-6	1.3	1.56
M4-5-6	1.56	1.56
M5-6	1.4	1.04
M6	0.52	0.78
M1-2-3-4-5	0.39	1.04
M1-2-3-4	1.62	2.86
M1-2-3	1.8	3.12
M1-2	5.98	7.3
M1	>9	>9

Table 2: Young's modulus of beams(unit: GPa)

Beam Type	Young's modulus
M1-2-3-4-5-6	91.6
M1-2-3-4-5	93.5
M1-2-3-4	91.6
M6	62

in Fig.8. The released capacitor has a constant capacitance value up to the 3 GHz, whereas the unreleased capacitance value reduces with frequency. The larger value of the unreleased capacitor at low frequency is due

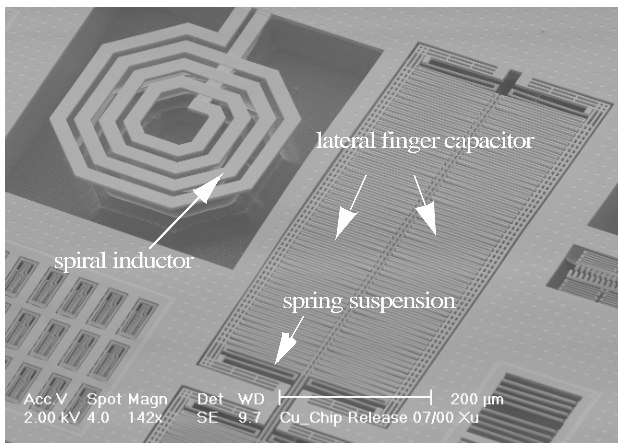


Fig. 7. *Micromachined MEMS inductor and capacitor in Cu low-K dielectric interconnect process for RF application.*

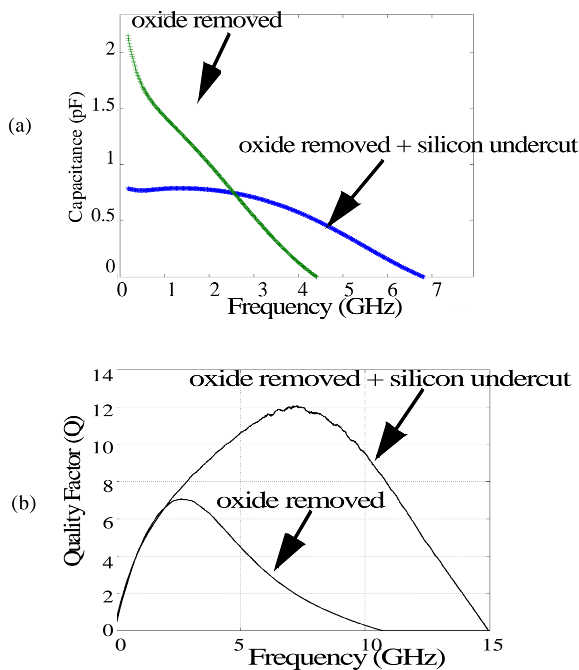


Fig. 8. *The measurement on MEMS RF components.*
(a) Comparison of the air gap capacitance of the oxide removed capacitor and the oxide removed plus silicon undercut capacitor.
(b) Comparison of the inductance of the inductor on the silicon substrate and suspended in the air after undercut silicon substrate.

to the parasitic capacitance to the substrate. The inductor's quality factor (Q) with the Si substrate removed reaches 12 with just 0.75 µm thick wire. The Q at 7.5 GHz is 6 times higher than the counterpart without Si substrate removed [7].

CONCLUSIONS

The migration of post-CMOS micromachining from the Al interconnect SiO_2 process to the Cu interconnect low-k dielectric process has been demonstrated. The major processing issues have been illustrated and the revised processing parameters have been set up. All these efforts in processing guarantee the successful fabrication of MEMS structures in the state-of-art of semiconductor processes. New applications for the post-CMOS technique are leveraging the properties of Cu. Fabrication of high quality RF components with the capability of on-chip integration is one example.

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