CMOS Micromachined Infrared Imager Pixel

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ABSTRACT

We report a CMOS micromachined infrared (IR) sensitive pixel that senses temperature by measuring capacitance change due to lateral motion induced by differences in thermal coefficient of expansion (TCE) of two materials. The temperature-induced capacitance change is measured by an on-chip circuit with input d.c. bias feedback and double-correlated sampling. The device is fabricated using a standard 0.5µm CMOS process followed by a maskless CMOS micromachining process. The area of the pixel sense element is 800 μm^2. Measured pixel sensitivity is 0.57 mV/K with equivalent temperature noise of 6 $mK/\sqrt{Hz}$, corresponding to 0.2 $aF/\sqrt{Hz}$ of equivalent capacitance noise.

INTRODUCTION

Uncooled infrared imagers consisting of an array of bolometers are commercially available. They require custom processes and therefore are costly, leading to a limited penetration of these IR imagers into the consumer market. CMOS imagers compete with traditional CCD cameras for visible light imaging applications due to advantages of cost brought about by use of standard processing. Similarly, a CMOS micromachined IR sensitive pixel may lead to cost effective uncooled IR imagers with widespread application. The dimensions of the reported pixel are 20 µm by 40 µm. Calculations indicate that this pixel could be integrated into an IR imager with less than 50 mK NEDT after process enhancements. Previous work on uncooled IR imagers has focussed on use of bolometers [1], suspended transistors [2], thermopiles [3], and thermomechanical capacitors [4]. This is first time lateral thermomechanical motion and capacitance change have been exploited for IR sensing, in contrast to vertical motion [4]. The pixel rejects common-mode mechanical effects like unwanted spurious external forces and spurious resonant oscillations.

CMOS MICROMACHINING PROCESS

The IR pixel has been fabricated in the high-aspect-ratio CMOS micromachining process developed at Carnegie Mellon University. The process flow, shown in Figure 1, enables fabrication of micromachined structures in a standard 0.5µm 3-metal CMOS process. The conventional CMOS process is followed by an anisotropic reactive-ion etch (RIE) with CHF_3 and O_2 to etch away oxide not covered by any of the metal layers, resulting in high-aspect-ratio vertical sidewalls. An isotropic RIE (using SF_6 and O_2) then removes the underlying silicon, thus releasing the microstructure. To reduce the thermal conductivity of the anchor, the anisotropic oxide etch time is increased to decrease the thickness of the top-most metal layer.

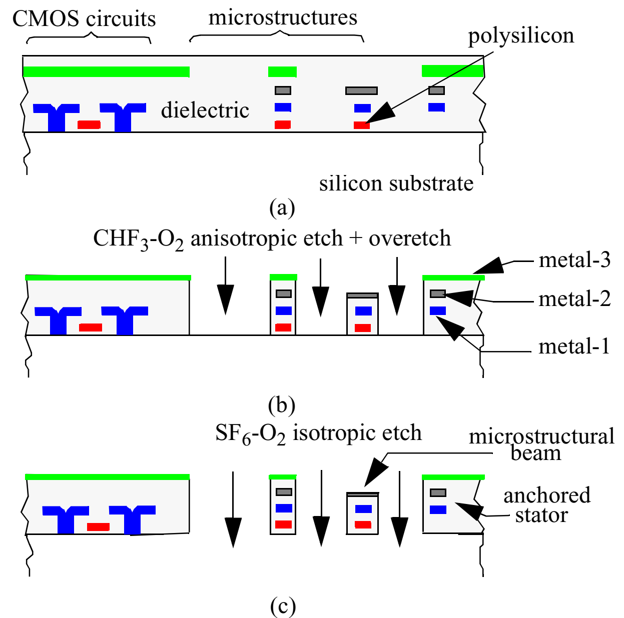

Figure 1. *Schematic of the process for micromachined structures in conventional CMOS.*

PRINCIPLE OF OPERATION

To illustrate the operating principle of the IR pixel, consider two adjacent CMOS micromachined beams that have embedded metal-1 and metal-2 layers intentionally aligned to the right and left sides, respectively, of the two beams (see Figure 2). The temperature coefficient of expansion (TCE) of aluminum (23µ/K) is much larger than

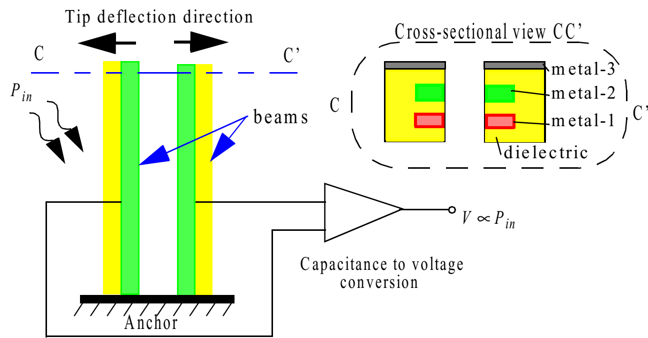

Figure 2. *Schematic of the pixel operation. Temperature change induces a lateral deflection that is measured as a capacitance change.*

that of the CMOS inter-layer dielectric (0.4μ/K). If a temperature change is induced in the beams due to incident IR, a lateral bending moment is produced. The beam bending is proportional to difference in the TCE of aluminum and inter-layer dielectric. The out-of-plane curl of two beams[6] is identical and does not contribute to performance degradation. The lateral motion increases the inter-beam separation and decreases the capacitance between the beams. This change in capacitance is measured by integrated CMOS circuits. The lateral motion at the tip of a beam (δ) of length L, width w, thickness t, and effective Young's Modulus, E can be expressed as

$$\delta = \frac{L^2}{2}\left(\frac{M_l}{EI_{zz}}\right) = \frac{6L^2M_l}{Etw^3} \quad (1)$$

where M_l is the lateral bending due to the beam cross-section and I_{zz} is the moment of inertia about the z axis expressed as $I_{zz} = \frac{1}{12}tw^3$. Temperature dependence of lateral bending moment is described in [6].

PIXEL DESIGN

The device area was minimized, given a desired nominal capacitance of at least 4 fF, to maximize the number of pixels can be placed economically on a single chip. The geometry of the pixel, shown in Figure 3, was designed for maximum sensitivity through manual iteration of the simulated response.

A meandering spring design with the beam cross-section similar to that shown in Figure 2 is used to maximize the tip deflection within the pixel area. The thermally induced lateral bending of the meandering spring acts similar to that of a single long beam.

The tip motion of the meandering spring is populated with interdigitated fingers to maximize the capacitance change. The different residual stresses in the embedded layers cause the comb fingers to move closer together after the mechanical release from the substrate. This leads to gaps that are smaller than the design rules of the process, thereby improving device sensitivity. Simulations [7] indicate the

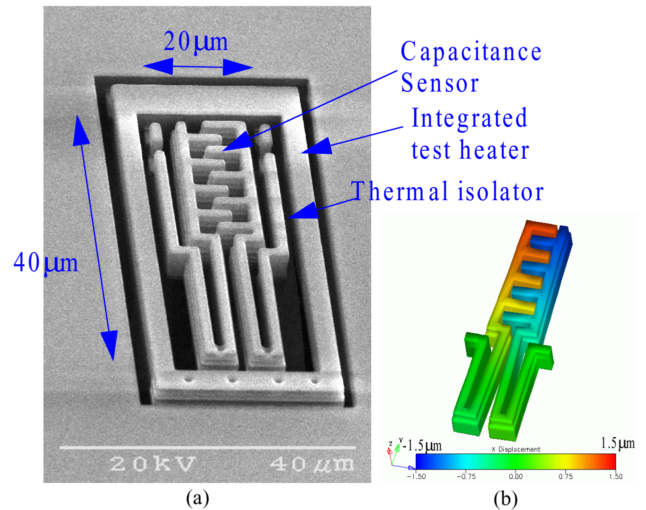

Figure 3. *(a) Scanning electron micrograph (SEM) of the IR pixel consisting of a thermal isolation beam and integrated heater for testing and sensitivity tuning.*
(b) Finite-element model illustrating reduction of comb separation due to release of residual stress.

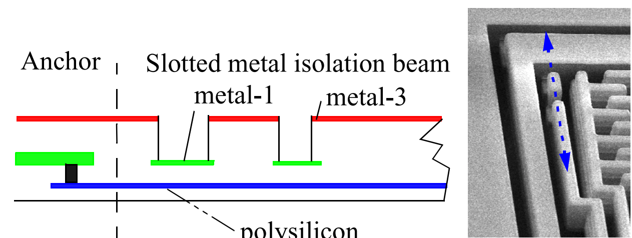

Figure 4. *Cross-section along the length of the thermal isolation beam as shown in SEM.*

nominal sense capacitance to be 4 fF after pixel self biasing due to residual stress, and the device sensitivity to be 40 aF/K.

Design of the thermal isolation between the device and the substrate is critical in IR sensor design. A high thermal resistance between the sense element and the substrate minimizes loss of incident IR radiation. The cross-section along the length of the thermal isolation beam is shown in Figure 4. To minimize thermal conductance, the thermal isolation beam has slotted metal lines, and electrical contact from the comb to the circuits is made by minimum width (0.6 μm) polysilicon interconnect. The higher electrical resistance of the interconnect does not pose limitations to the device performance unlike bolometers. The oxide beam is covered by thin metal layer that can be removed by a later post-CMOS processing step.

The capacitance sense circuit for the pixel uses double-correlated sampling to reduce 1/f noise and feedthrough. The schematic of the sense circuit is shown in Figure 5. The first stage is a source follower to minimize input parasitics. The gain is provided by a common-source amplifier. The d.c. bias at the input is set by a reverse-biased diode. The value of the d.c. bias voltage is determined by a replica biasing circuit such that the output voltage is centered. This biasing scheme reduces the effects of d.c. drifts and maximizes the dynamic

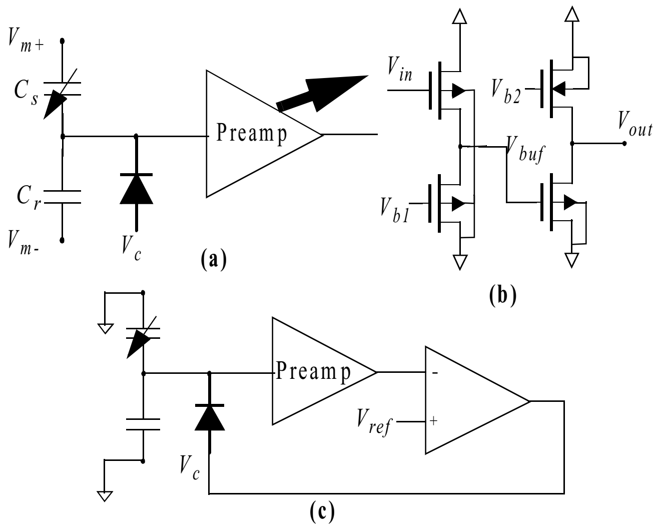

Figure 5. Schematic of the pixel capacitance sense circuit.
(a) The diode biased capacitance sense circuit.
(b) Schematic for the preamp circuit.
(c) The replica bias circuit that sets the diode d.c. voltage.

range. The diode can latch high, which is a potential problem, however this is prevented in the measurements by illuminating the diode.

To control electrical sensitivity and consequently the contrast of the imager, a polysilicon resistor is embedded within a frame surrounding the pixel sense element. The frame is heated by passing current through the resistor.

The right and the left parts of the device are not designed identically, resulting in different mechanical resonances for each side. This helps reject spurious mechanical oscillations of the device that affect device performance in high vacuum, as the beat frequency is out of the signal band.

EXPERIMENTAL RESULTS

Electrical Characterization

The experimental setup for measuring pixel electrical performance was simplified by using Joule heating in the surrounding frame. The capacitance change as a function of temperature change in the frame was measured. The temperature of the pixel was determined from the resistance of the polysilicon heater. The thermal coefficient of resistivity of the polysilicon heater resistance was obtained by measuring the resistance in a temperature-controlled oven and correcting for the device temperature gradient. The chip temperature was measured using the junction voltage of an on-chip well-substrate diode. The correction for the non-uniform heater temperature was made using a shape factor of the temperature profile obtained by electrothermal modelling [7]. An example temperature distribution due to the heating of the surrounding polysilicon resistor with 1 mA of current is shown in Figure 6.

Electrical feedthrough from the polysilicon heater was eliminated by use of correlated double sampling. Data was collected for sampling frequencies ranging from 100 kHz to

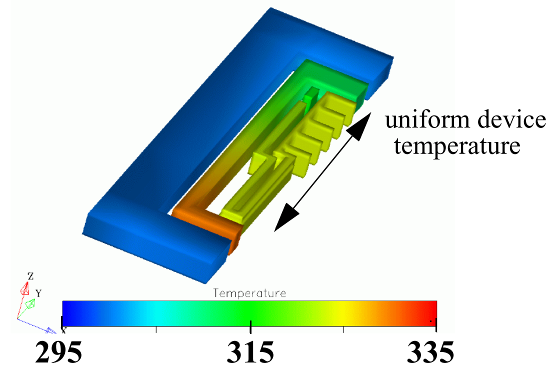

Figure 6. *Electrothermal finite-element simulation of the temperature distribution in the device in air for an 1 mA polysilicon heater current.*

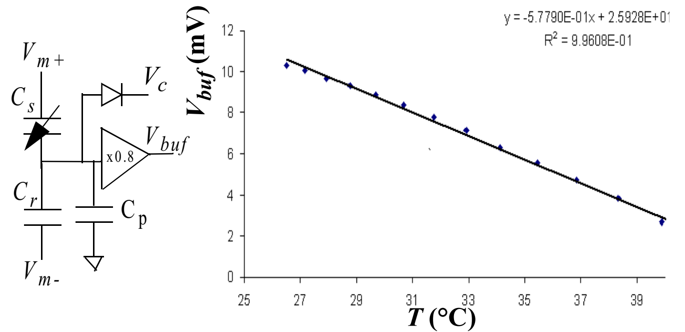

Figure 7. *The measured buffer output as a function of device temperature produced by the heater.*

2 MHz. The gain of the entire preamp was 10, with a gain of 0.8 in the first stage. A plot of the output of the capacitive bridge circuit with temperature is shown in Figure 7. The temperature sensitivity was 0.57 mV/K across the capacitive bridge (without gain). The spectral output of the sinusoidal heating of the integrated heater with a 25 mV, 30 Hz heater input signal, corresponding to a 12 mK peak temperature change is shown in Figure 8. The noise floor of the pixel was measured to be 6 $mK/\sqrt{Hz}$ after demodulation. This corresponds to 0.2 $aF/\sqrt{Hz}$ of equivalent capacitance noise. The transient response of the pixel with a sinusoidal temperature change induced by electrical heating is shown in Figure 9.

Mechanical Characterization

The lateral motion sensitivity was measured to be 126 Å/K (Figure 10) using the MIT microvision system [9]. Finite-element modeling predicted a lower sensitivity of 104 Å/K. Sidewall etching during the release process yields thinner beams that improve sensitivity. The mechanical resonant frequency of the right and the left half of the pixel was measured to be 245 kHz and 230 kHz, respectively. The beat frequency due to spurious resonances in both the beams is 15 kHz, which is outside the sense bandwidth of 30 Hz. The device was measured in a vacuum of 1 mT, and no peaks were observed due to low frequency electrostatic excitation of the

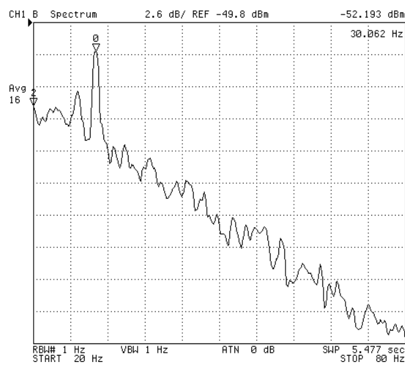

Figure 8. *Demodulator output for a 25 mV (peak), 30 Hz heater input signal corresponding to a 12 mK peak signal The equivalent temperature noise is 6 mK/$\sqrt{Hz}$.*

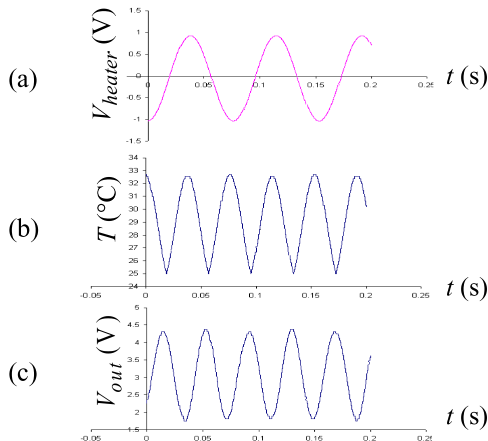

Figure 9. *Measured transient response of the IR pixel. (a) Voltage applied to the polysilicon heater. (b) Temperature of the pixel. (c) Output of the pixel sense circuit.*

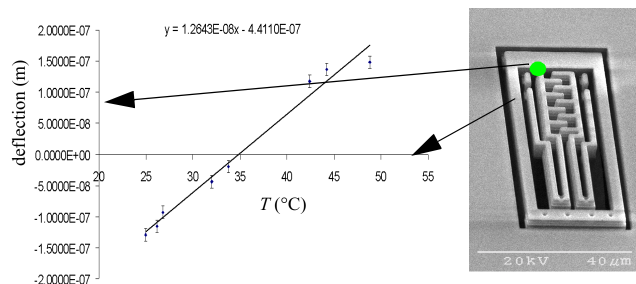

Figure 10. *Measured pixel tip deflection as a function of temperature produced by integrated heater.*

device at the beam resonant frequencies or the beat frequencies. The thermal time constant of the surrounding heater and imager pixel is 2.8 ms.

CONCLUSIONS

A new method of temperature sensing suitable for small infrared pixel applications has been demonstrated. The device performance is expected to improve with CMOS scaling. The thicker stack height due to the increasing number of interconnect metal layers in modern CMOS will increase the sense capacitance. Smaller feature sizes will also allow better definition of gaps and beam widths. The lateral motion produced due to temperature change has a cubic dependence on the beam width.

The advantage of capacitive sensing over resistive sensing (*e.g.,* bolometers) is that there is no self heating due to the sense current. This means that the thermal isolation between the sensor and substrate can be made out of very thin polysilicon lines without affecting sensitivity. An ion milling step can remove the top metal at the anchor leaving oxide with low thermal conductivity. Power and noise trade-offs can be made by the designer of the capacitive sense circuit. The bias scheme may be improved by eliminating the diode.

Our present focus is to improve the IR absorption of the pixel by deposition of IR absorbent material. The IR absorbance can also be improved by optimization of the release depth of the imager to create a resonant cavity for IR wavelengths.

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