

# SPEED: Synthesis of High-Performance Large Scale Analog/Mixed Signal Circuit

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## ABSTRACT

*Simulation-based cell level analog synthesis tools have been successfully proven by chip fabrication. Application of these synthesis approaches to larger circuits with high accuracy has been difficult due to two limitations: 1) large design space, 2) long simulation time. This paper addresses these limitations using a systematic methodology SPEED, Simulation Plus Equation-basED synthesis, to size the first two multiplying and sub-DAC stages in a 13-bit 40-MSample/s pipelined analog to digital converter for minimum power consumption. The resulting chip, which had a measured signal to noise ratio of 73.8dB and consumed 364mW @ 3.3V proves the efficacy of the proposed synthesis approach.*

## 1. INTRODUCTION

Analog design time is increasingly becoming the bottleneck in SoC designs. This problem becomes graver with system specification retargeting or process technology migration. Digital blocks can be adapted to new specifications or processes with minimum redesign or through standard cell library update. However, analog redesign needs almost the same amount of time as the original design.

Recent developments in analog synthesis have enabled rapid design of analog cells [1]. The ability of these designs to meet the cell performance is evaluated by either a simulation-based [2-5] or equation-based approach [6-9]. The choice between simulation-based and equation-based approaches is a trade-off between accuracy and speed. Simulation-based approaches are often preferable as they use SPICE-based simulators that have long been trusted by analog designers, but at the cost of simulation time. These design automation methods are appropriate and practical for cell level synthesis because 1) the number of design variables is small; 2) each simulation does not take too much time for simulation-based approach; 3) circuit is simple enough for accurate equation-based modeling.

Extending these approaches to beyond the cell level has been difficult. The larger search space arising from the increased number of design variables need more iterations to find the design optimum. Equation-based evaluation in each iteration has difficulty in accurately modeling the circuit performance, especially when linear and nonlinear features have to be embedded in the same model. The simulation-based performance evaluation requires enormous simulation time due to more devices, higher dynamic range and/or high resolution requirements at the simulation output. All these factors make it difficult to apply the existing cell-level synthesis flow at the higher level.

We propose the approach “SPEED”, Simulation+(Plus) Equation-basED evaluation to rapidly re-design the first two stage multiplying and sub-DACs (MDACs) of the “manual-designed and proved” 13-bit 40MSPS pipelined ADC. Our optimization goal is *power minimization* of the first two stages. The MDAC blocks in these stages have the same topology but with different specifications. Scaling the op-amp-based MDACs improves ADC performance, but, is very time consuming. Applying synthesis for this specification retargeting problem can speed-up the design time and lead to custom ADC performance. Using synthesis for only the first two stage of the MDACs as the design vehicle has three advantages. First, the performance of the ADC is dominated by the first two stages. Second, the power is mainly consumed by the first two stages. Third, it can highlight and isolate the problems if the performance does not meet the specifications.

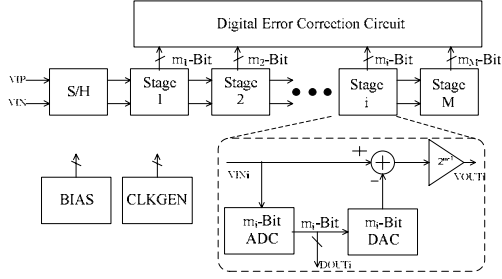
The contribution of this paper is to show that using SPEED can reduce simulation time while maintaining the accuracy. It enables reliable block-level synthesis of the MDAC for performance retargeting. The paper is organized as follows. Section 2 describes SPEED and synthesis of MDAC using SPEED. Section 3 describes ADC measurement results. Finally, section 4 presents some concluding remarks.

## 2. MDAC USING SPEED

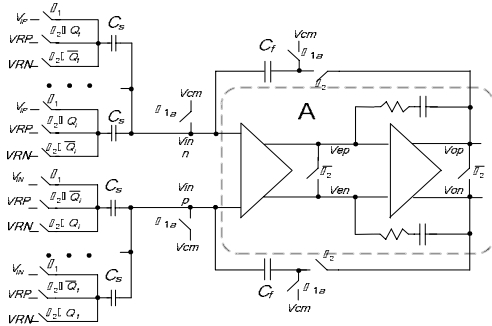
In this section we first overview the pipelined ADC architecture. Then we describe the methodology of SPEED. Finally, we present the MDAC synthesis using SPEED.

### 2.1 Pipelined ADC Architecture

Fig 1 shows that the pipelined ADC consists of a front-end sample and hold amplifier (S/H amplifier) and  $M$  pipelined stages. The S/H amplifier samples and holds analog input signal, then multiple data converter stages quantize the input signal subsequently. Each stage samples the signal from previous stage and quantizes to  $m_i$ -bits using a flash sub-ADC. Then, the quantized signal is subtracted and the residue is amplified by  $2^{m_i-1}$  through the inter-stage amplifier to be sampled by the subsequent stage. The functions of the sub-DAC, subtractor and residue amplifier are commonly combined into a Multiplying Digital to Analog Converter (MDAC) block as shown in the schematic in Fig. 2. The same procedure is repeated in each stage down in pipelining fashion to performance ADC. One extra bit from each stage is used to implement digital correction logic [10]. In this paper, the optimization goal is *power minimization* of the MDACs in the first two stages of the 13-bit 40 MSPS pipelined ADC, which are two of the most critical parts of the ADC, in the TSMC 0.25 $\mu$ m 3.3V symmetric CMOS process.



**Fig. 1 Pipelined ADC architecture**



**Fig. 2 MDAC block schematic**

## 2.2 SPEED Methodology

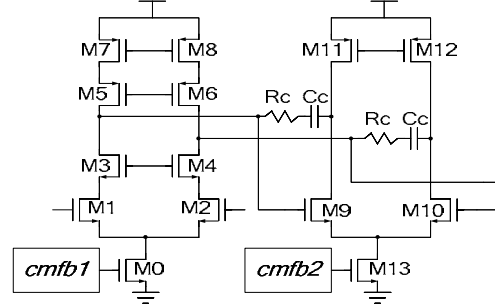
As the synthesis procedure is iterative, and circuit performance evaluation tends to dominate the time required for each iteration, a fast and accurate evaluation methodology is desirable. However, speeding up circuit evaluation is often at the cost of reducing accuracy, and vice versa. To overcome this, we propose the approach “SPEED”, Simulation+(Plus) Equation-based evaluation methodology. When circuits experience large dynamic swing, simulation-based evaluation produces trustworthy results within a short period of time. When circuit behavior is linear, equation-based transfer functions based on small signal parameters evaluate circuit performances accurately and efficiently. Combining these approaches has the advantage of high simulation accuracy and fast equation evaluation. One drawback of equation-based synthesis has been the time required for deriving the transfer functions [11]. While this may be true in general, derivation of only block-level closed-loop transfer functions is simple for experienced analog designers.

These symbolic transfer functions are derived only once, prior to iterative design using synthesis tools. A computational program that transforms numerical transfer functions (frequency domain) into step response (time domain) is also needed. This program employs the following procedure in each design iteration: 1) partial fraction expansion of the numerical transfer functions, 2) inverse Laplace transformation of each partial fraction term, 3) combination of non-linear simulation and linear inverse Laplace transforms to obtain settling time, 4) reporting the settling time as “ $t_{i, settle}$ ”.

Thus, evaluation of each candidate solution involves: 1) DC simulation to extract small signal values, 2) formulating the numerical transfer function, and using the program for SPEED. This evaluation procedure is performed automatically in each synthesis iteration. SPEED therefore helps estimate highly accurate settling times at speeds of 7~10 times faster than SPICE-based transient simulation.

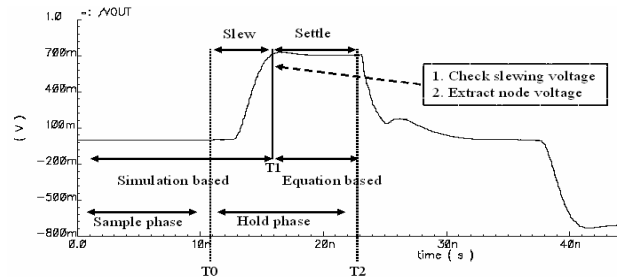
## 2.3 MDAC synthesis using SPEED

The op-amp cell of the MDAC (labeled A in Fig 2) is implemented with two-stage amplifier as in Fig. 3. Each MDAC operating cycle has two phases as shown in Fig. 4. In the sampling phase, the input signal is stored on the sampling capacitors ( $C_s$  in Fig 2). In the hold phase, the MDAC first operates under high dynamic swing (non-linear slew) then settles linearly.



**Fig. 3 Two-stage amplifier**

For MDAC behavior, high accuracy is only needed in the linear settling portion of the hold phase (about 1/4 of the whole cycle). However the entire simulation can only be done to the same level of simulation accuracy. Therefore, a lot of simulation time is wasted in achieving higher than needed accuracy for almost 3/4 of the MDAC cycle, making block-level simulation-based synthesis almost impossible. We propose SPEED, a hybrid method in which non-linear simulation of the large-signal part of the MDAC operation is combined with accurate equations from transfer function for the LTI settling portion of the MDAC operation for overall fast and accurate performance evaluation. When circuit behaves from sampling to the end of the slew part of the hold phase (e.g. from 0 to the time point T1 in Fig 4), simulation-based evaluation produces reliable results. Following a transient simulation (controlled by the transient test bench), we need to extract the node voltage information at time point T1 (in Fig. 4) for use in the equation-based settling time evaluation. A computational program that numerically solves the equations to extract the settling time performance of the circuit automatically in each synthesis iteration.



**Fig. 4 MDAC Behavior**

Defining a synthesis problem requires identifying the synthesis 1) goal, 2) the specification constraints, 3), the design variable ranges and 4) the test benches for SPEED. A commercial cell-level sizing engine (NeoCircuit) was used to optimize each MDAC block.

1) *Goal*

The synthesis goal is to *minimize* the MDAC power.

2) *Design Specification Constraints*

The constraints from device-level, cell-level and block-level can be combined with three constraints: 1) all the MOS in op-amp (Fig. 3) should be in saturation region; 2) MDAC noise must be lower than the MDAC noise constraints; 3) MDAC settling time has to meet its specification. Note that the cell-level op-amp specifications (gain, bandwidth, phase margin, etc.) are subsumed into the settling time and noise constraints, hence do not need to be evaluated separately. This helps reduce the simulation time during synthesis. The resulting constraints of the block-level MDAC can be enumerated as below:

Device constraint:

$$|V_{ds}| - |V_{dsat}| \geq 0.1 \quad \text{for } M_0 \sim M_{13} \quad (1)$$

Noise constraint:

$$n_q + \sum_{i=1}^M n_{i,input} < \frac{(2^{N-1} \Delta)^2 / 2}{10 \frac{SNR_{max}}{10}} \quad (2)$$

Settling time constraint:

$$t_{i,slew} + t_{i,sett} \leq \frac{1}{2 f_{sample}} \quad (3)$$

where

$M$ : number of stages

$N$ : total resolution of the ADC

$n_q$ : quantization noise of the ADC

$n_{i,input}$ : input referred noise power of stage  $i$

$\Delta$ : signal voltage corresponding to 1 LSB

$SNR_{max}$ : maximum signal to noise ratio for the ADC

$f_{sample}$ : target ADC sampling frequency

$t_{i,slew}$ : slewing time for MDAC output

$t_{i,sett}$ : time for MDAC output settling to required accuracy

To ensure that the assumptions of the SPEED are met, the constraint in (3) has to be modified to (4) and (5).

$$|V_{out}(t = T1) - V_{slew\_ideal}| \leq V_{tol} \quad (4)$$

$$t_{i,sett} \leq \frac{1}{2 f_{sample}} - (T1 - T0) \quad (5)$$

where

$V_{slew\_ideal}$  is the ideal  $V_{out}$  assuming the MDAC has met the desired slew rate

$V_{tol}$  is a tolerance parameter to guarantee slew rate and prevent too much overshoot.

When circuit behaves from sampling to the end of the slew part of the hold phase, the transient test bench provides the node voltage at T1, then (4) ensures that the MDAC has adequate slew rate and is not exhibiting too much overshoot. When circuit behavior is linear, symbolic transfer functions based on small signal parameters are derived. The noise test bench provides the small signal model parameters ( $g_m$ ,  $g_{ds}$ ) and the transient test bench provides the node voltage at T1. The computational program for SPEED (in section 2.2) that transforms numerical transfer functions (frequency domain) into step response (time domain) is needed to ensure (5). The effect of initial voltage on the output capacitances is taken into consideration

by using their transfer function from step response analysis. Since the slew is captured by T0 and T1 (ensured by (4)), the settling time constraint in (3) changes to (5).

3) *Design variables*

Designers determine design variables ( $W$ ,  $L$ ,  $M$  of transistors and capacitor values) and ranges according to designer knowledge.

4) *Test Bench*

Test benches are the critical for SPEED. Using fewer test benches that can check all the design specifications helps to reduce the simulation time and makes it possible to synthesize larger circuits. In this case, only two test benches are needed: 1) transient test bench, 2) noise test bench. The transient test bench simulates the MDAC for only two cycles in every synthesis iteration. The analog input switches in the two cycles to test for the worse case. The test bench checks slewing voltage for constraint (4) and extracts node voltage for the computational program that transforms numerical transfer functions (frequency domain) into step response (time domain). The noise test bench checks for both the device constraints (1) and the noise constraint (2). It also provides the small signal model parameters ( $g_m$ ,  $g_{ds}$ ) for the computational program.

### 3. CHIP MEASUREMENT RESULTS

The ADC die photo is shown in Fig. 8. The measured power consumption is 364 mW @ 3.3 V, for 40 MSPS operation. Die area with pad is 5650um \* 3100um.

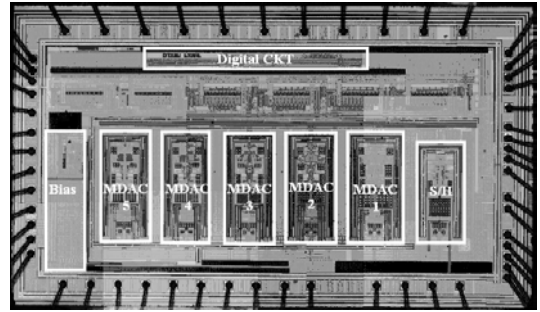


Fig. 8 ADC Die Photo

The measurement results for a fixed frequency 340 kHz sinusoid analog input ( $A_{in}$ ) and sampling frequency sweeping from 10 MHz to 50 MHz are shown in Fig. 9.

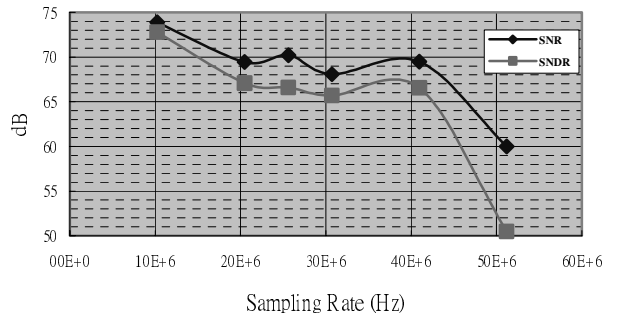


Fig. 9 Sampling frequency vs. ADC performance @  $A_{in}=340\text{KHz}$

The peak SNR is 73.8 from 10 MHz to 40 MHz which is equivalent to 12 ENOB. The performance degrades rapidly at 50 MHz, beyond the 40MSPS specification, showing that the synthesis method met the specifications without over-designing. The performance of  $A_{in}$  frequency swept from 340 kHz to 19.995 MHz (near Nyquist rate) at 40 MHz sampling rate is summarized in Fig. 10. The SNR is from 69.5dB to 64.3dB.

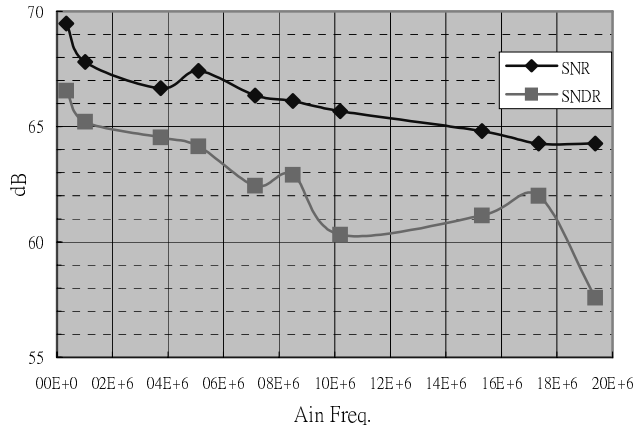


Fig. 10  $A_{in}$  vs. ADC performance @ 40MSPS

Fig. 11 demonstrates the FFT result of the output with a 340KHz sinusoid input at -0.73dBFS amplitude. The measured SFDR is 77.5 dB.

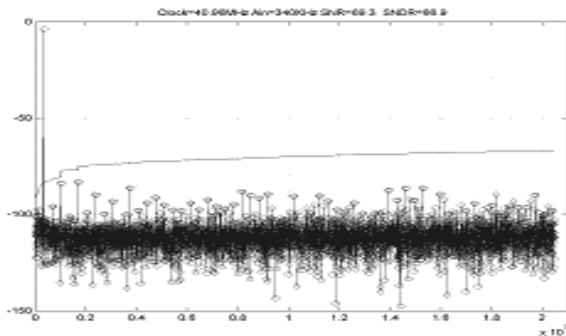


Fig. 11 FFT

3 weeks was needed for transfer function derivation as well as synthesis setup. Synthesis of the first MDAC stages took half a day. The primary setup effort for the second MDAC synthesis was specification retargeting (about a half day). The second MDAC also required a half day synthesis time. The method is inherently suitable for system level optimization of circuits that are composed of similar blocks with different specifications or re-usable circuits.

#### 4. CONCLUSION

This paper describes how to use SPEED reduces simulation time with maintaining high accuracy to make block-level synthesis feasible. The first two stages of the MDAC for 13-bit 40MSPS pipelined ADC is implemented in TSMC 0.25 $\mu$ m 3.3V symmetric CMOS process, 2.0 Vppd input consumes 364 mW @ 3.3V was designed using this

approach. The peak SNR is up to 73.8 dB. The measurement result shows that our synthesis methodology can be applied for synthesizing larger circuits with high accuracy.

#### Acknowledgements

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