RF CMOS-MEMS CAPACITOR HAVING LARGE TUNING RANGE

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ABSTRACT

Several CMOS-MEMS tunable capacitors have been designed, fabricated and tested. Large-tuning ranges and high Q values are achieved. The structures were made from the CMOS interconnect stack using a maskless CMOS micromachining process. The 1st generation capacitors were fabricated using Austria Microsystems (AMS) 0.6 µm and Agilent 0.5 µm CMOS process. These devices have a measured nominal capacitance of 209fF and a measured quality factor 28 at 1.5 GHz. The capacitance change is measured from 209fF to 294fF within a 24V control voltage, and 72.4 mW power at 1.5 GHz. 2nd-generation tunable capacitors in TSMC 0.35 µm CMOS process have larger tuning range and more power efficiency than the 1st generation designs. For these new designs, 3.52 to 1 tuning range has been measured with tuning from 42 fF to 148 fF within a 12 V control voltage, and 34mW power at 1.5 GHz. This recent design has a measured Q of 52 at 1.5 GHz. Electro-thermal actuation is used for all tunable capacitor designs. The essential differences between this work and prior work are the CMOS compatibility and using a maskless CMOS micromachining process.

INTRODUCTION

There is an increasing demand on tunable on-chip passive components, as this is the one of biggest impediments for designing system on chip (SOC) receivers. Recently, MEMS technology has begun to be used in wireless communication systems to improve performance of existing devices. In the past few years, tunable capacitors based on MEMS technology are under development [1-4]. In RF MEMS, micromechanical tuning avoids the high resistive-capacitive losses associated with semiconductor varactors at high frequencies and the movement linearly of MEMS devices also allows the capacitors to tune linearly. Tunable RF components such as voltage-controlled oscillators (VCO) and tunable filters have been developed using micromachining technology [1-3].

In this paper, we will present new CMOS-compatible tunable capacitors. Previous designs use separately fabricated CMOS electronics for potential applications like VCOs or tunable filters [1-3], as the capacitors are not CMOS compatible. For our designs, the structures were made using the CMOS interconnect stack and released with a maskless CMOS micromachining process [5]. A key advantage of this approach is that CMOS electronics for VCOs and other possible applications can be integrated on the same chip, thereby eliminating losses coming from interconnects between chips. For 2nd-generation tunable capacitors in the TSMC 0.35 µm CMOS process, tuning ranges of 352% have been achieved.

CMOS MICROMACHING PROCESS

The high-aspect-ratio CMOS micromachining technology [5] begins with a conventional foundry CMOS process. Versions of these actuators were fabricated using Austria Microsystems (AMS) 0.6 µm CMOS, Agilent 0.5 µm CMOS and TSMC 0.35 µm CMOS. After the foundry fabrication, three dry-etch steps, shown in Figure 1, are used to define and release the structure. Fig. 1(a) shows the cross section of the chip after regular CMOS fabrication. In the first step of post-CMOS processing (Fig. 1(b)), dielectric layers are removed by an anisotropic CHF_3/O_2 reactive ion etch (RIE) with the top metal layer acting as an etch resistant mask. After the sidewall of the microstructure is precisely defined, silicon trenches around the device are micromachined into the substrate using a deep RIE step. Then the final step is an isotropic SF_6/O_2 RIE used to etch away the bulk silicon and release the structure (Fig. 1(c)).

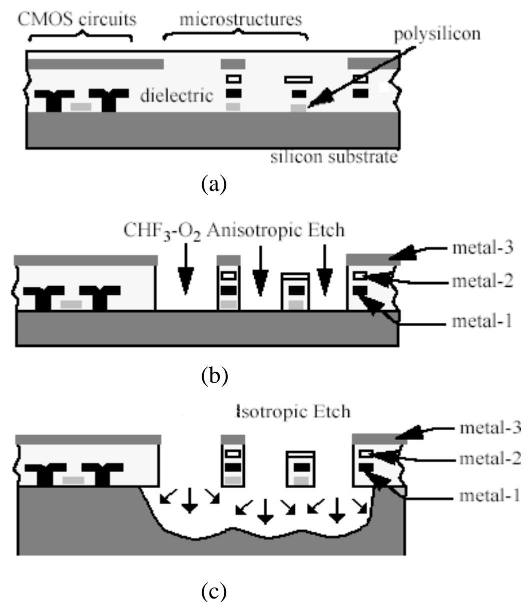

Figure 1. CMOS-MEMS process. (a) CMOS chip after fabrication, (b) anisotropic RIE removes dielectric layers, (c) isotropic RIE undercuts silicon substrate.

DESIGN AND MODELING

Interdigitated beams are used for our capacitor designs, as our structures are constrained to a single mechanical layer. Some previous designs are using parallel plates for their capacitors [3-4]. Our tunable capacitor designs can be classified into two categories based on their tuning schemes. Both comb gap and area tuning are used for 1st generation capacitors, and only gap tuning is used for the 2nd generation capacitors.

Tunable Capacitor Designs using Gap&Area Tuning. These tunable capacitors were fabricated using AMS 0.6 µm and Agilent 0.5 µm CMOS process. Electro-thermal actuators are used for our MEMS tunable capacitor design (Fig. 2). In contrast, some previous works used electrostatic actuators [2-3]. Polysilicon resistors act as heaters inside the inner frame. Upon heating the structure, the interdigitated beams curl down vertically and also curl sideways. This curling changes the area between interdigitated beams for tuning. The reason of this curling behavior is that metal and oxide layers inside the beams have different TCE values. Gap tuning is achieved by electro-thermal actuators. Compared to electrostatic actuators, thermal actuators have advantages of linear capacitance tuning and lower driving voltage, but consume more power in continuous operation.

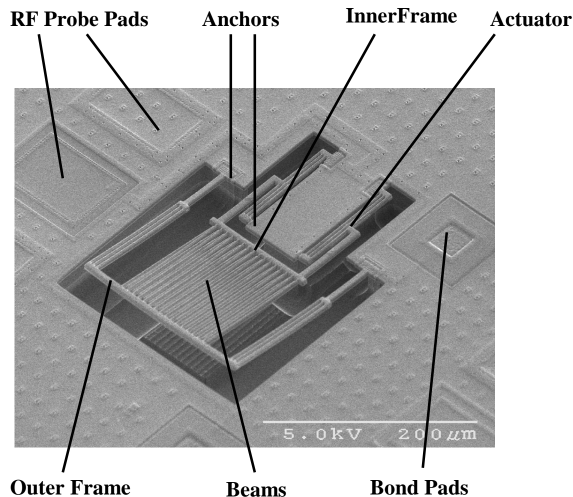

Figure 2. Scanning electron micrograph (SEM) of a released tunable capacitor in AMS 0.6 µm CMOS process.

Electro-thermal Actuator Designs. For this new actuator design, motion is induced in specific beams by designing a lateral stress gradient within beam flexures. The lateral stress gradient arises from purposefully offsetting the lower metal layers with respect to the top metal layer of a CMOS-MEMS beam, as shown in Fig. 3(a). Of particular importance is the ability to tailor the lateral stress gradient, and therefore lateral moment, as a function along the beam length. The primary concept of the lateral actuator is illustrated in Figure 3. This particular design is a folded-flexure to relieve axial residual stress. The metal layers inside the flexure beams are offset to one side of the beam for half the beam length, and to the other side for the remaining half of the length, as shown in Fig. 3(b). This arrangement provides a lateral stress gradient in one direction for half of the beam length, then switches to the other direction for the other half. For many CMOS-MEMS processes, the residual stress gradient in the offset aluminum layers is tensile, while the residual stress gradient in the surrounding silicon oxide layers is compressive. Therefore, the aluminum expands and the silicon oxide contracts once freed to move. Upon release, this tailoring of stress provides a self-actuating operation, where the beams move into a "S" shape. These electro-thermal actuators were fabricated using AMS 0.6 µm, Agilent 0.5 µm CMOS process and TSMC 0.35 µm CMOS process. Upon release, this self actuation operation was observed for actuators in AMS 0.6 µm, Agilent 0.5 µm CMOS processes [6]. The actuators in TSMC 0.35 µm CMOS process didn't move after release, as the residual stress and stress gradients in the TSMC process are much lower than Agilent and AMS processes. An SEM of a released actuator design in the TSMC 0.35 µm CMOS process is shown in Fig. 3(c).

Electrothermal actuation can be applied to any designed actuator. The heating is implemented by embedding a polysilicon heater resistor inside the beam. Motion is induced from the different Temperature Coefficient of Expansion (TCE) of the metal offset layers and the oxide.

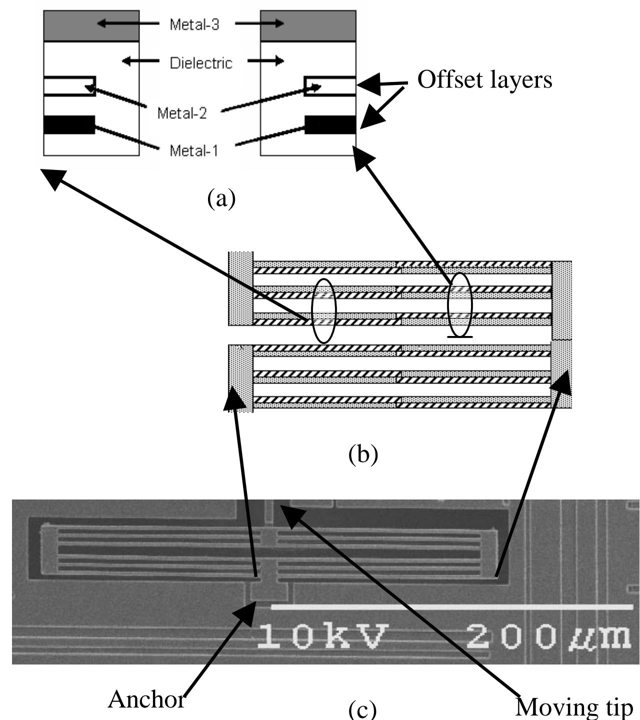

Figure 3. The concept of the electro-thermal actuator design. (a) cross-section view of beams. (b) half layout of the electro-thermal actuator. (c) SEM of a released tunable capacitor in the TSMC 0.35 µm CMOS process.

The offset aluminum layers have a much larger TCE than the surrounding silicon oxide. When heated, the side of the beam with the aluminum offset will expand relative to the other side. This effect leads to the actuated lateral motion. Simulations for calculating the lateral displacement are performed in FEA (Finite Element Analysis) tool Coventorware [7]. Simulated data is matched with measured data with error of 10% [6].

The actuator designs in the TSMC 0.35 µm process were tested by applying DC voltage to the polysilicon heaters, as shown in Fig. 4. There are two types of actuators designated as half size and full size. The full size actuator is shown in Fig.3 (c), and the half size actuator is shown in Fig. 5(a). Half-size actuators have advantages compared to full-size actuators of more area efficiency and less power consumption. For a half-size actuator with a length of 124 µm and a width of 22µm, 5.5 µm actuation is measured with 8.4mW of heating power in air.

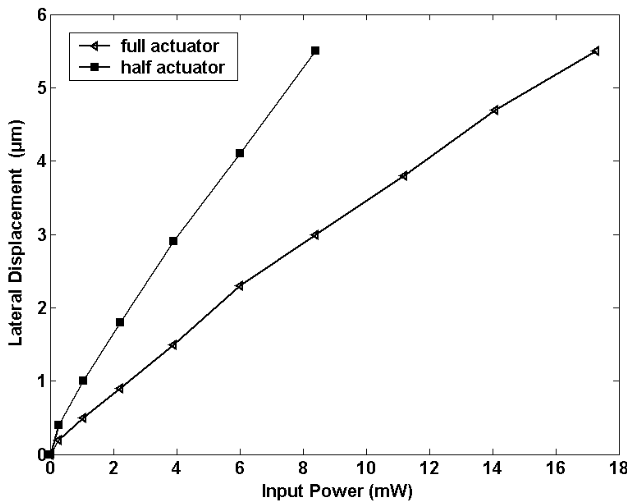

Figure 4. Measured lateral displacement versus input power for the half-size and full-size electro-thermal actuators in TSMC 0.35 µm process.

Tunable Capacitor Designs using Only Gap Tuning. These capacitors were fabricated using TSMC 0.35 µm CMOS process. Gap tuning is again achieved by electro-thermal actuators. Instead of interdigitated beams, small fingers are used to increase the tuning range and area efficiency. Fig. 5(a) is showing a 2nd generation released tunable MEMS capacitor with half-actuators. One of the design goals was switching between multiple capacitor values with low power operation. For these designs, lateral electro-thermal actuators are used for implementation of lateral latch structures. By using these latch structures, we intended to consume power only when we are switching between fixed capacitance values. The latch structures in the first TSMC 0.35 µm chip did not work, as the actuators displaced differently from the other CMOS process, because of the lower stress gradients. Functional latches in future designs will require no power to operate statically at a given capacitance value. Previous designs consume continuous power for tuning [1-4]. Fig. 5(b) and Fig. 5 (c) show a closer view of the finger parts of the tunable capacitors. The disengaged mechanism is shown in Fig. 5(b) after release without electro-thermal actuation. Fig.5(c) shows the engaged mechanism with actuation of 12V control voltage.

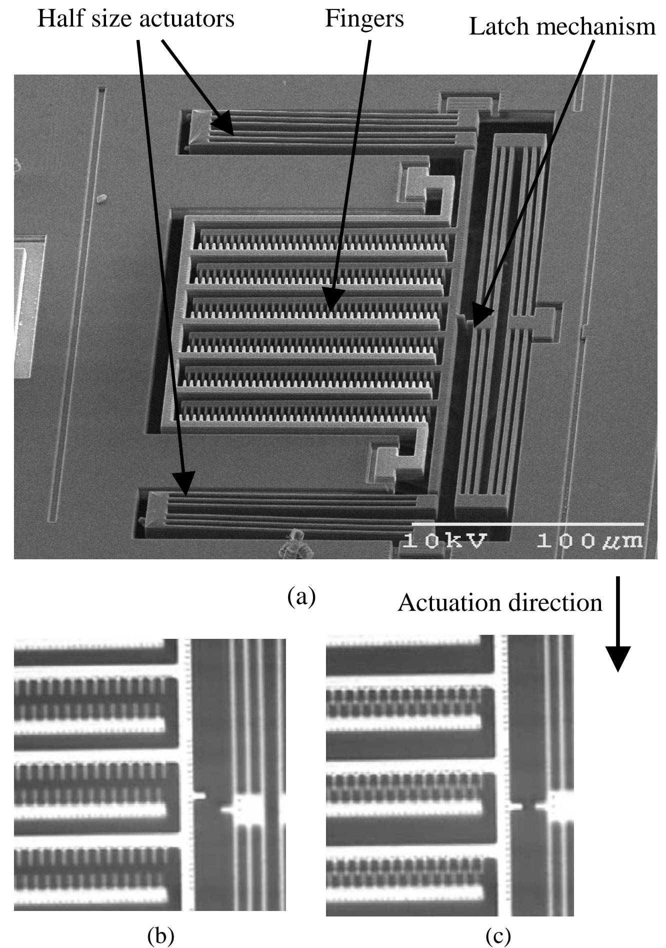

Figure 5. (a) SEM of a released tunable capacitor in TSMC 0.35 µm CMOS process with half-size actuators. (b) disengaged mechanism for getting C_{MIN}. (c) engaged mechanism for getting C_{MAX}.

MEASUREMENT RESULTS

The summary of the experimental tunable capacitors and their measured capacitances, power and Q values are shown in Table I. S_{11} parameters of the 1st and 2nd generation tunable capacitors are measured using an Agilent E8364A network analyzer from 45 MHz to 3 GHz. The 1st generation designs have low tuning ratios compared to the 2nd generation designs. The reason for this low tuning range in AMS 0.6 µm CMOS process is the excessive lateral beam curling, which causes the fingers to snap together [8]. The reason for the low tuning range in the Agilent 0.5µm CMOS process is the behavior of the electro-thermal actuators in that process; they displaced the opposite way of the intended direction, upon release [6].

TABLE I
CHARACTERISTICS OF CMOS-MEMS TUNABLE CAPACITORS

Device	Overall size(μm×μm)	C_{MIN} (fF)	C_{MAX} (fF)	Tuning Range	V_{TUNE} (V)	Power (mW)	Q at 1.5GHz
1st generation design in AMS process	170×220	153	175	14.4%	12	25.5	24
1st generation design in Agilent process	230×270	209	284	35.9%	24	72.4	28
TSMC design with full actuator	228×250	42	148	352.4%	12	34.2	52
Compact TSMC design with full actuator	228×230	40	98	245%	12	27.1	40
TSMC design with half actuator	150×250	53	108	203.8%	6	22.4	35
Compact TSMC design with half actuator	150×230	35	102	291.4%	6	18.3	48

For 2nd generation capacitors, large tuning ratios have been achieved, by using the finger gap tuning mechanism, instead of beam area tuning. These new capacitor designs have also higher Q values and less power consumption compared to 1st generation chips. The detailed RF characterizations of all these devices in Table I were presented [8]. Compact capacitors in Table I were designed to get the best area efficiency among TSMC designs. As it is shown in Table I, the best design for area efficiency is 1st generation design in Agilent process. The TSMC designs have less area efficiency, because as it can be seen in Fig. 5(c) the engaged mechanism is not working with 100% efficiency. During the engaged process, the fingers stick at some point. Future work is being carried out to solve this problem, which will increase both area efficiency and tuning range.

Fig. 6 shows the measured tuning characteristics of 2nd-generation design in TSMC process with full-size actuators. The tuning looks linear, but the problem is the high tuning range is coming from the ratio of the capacitances at 12 V and 6 V control voltages. So with zero control voltage, the capacitance value is 95 fF, then it goes to 42 fF at 6 V control voltage, and achieves the highest value, 148 fF, at 12 V. The increase in capacitance for voltage above 6 V is due to the parallel-plate gap closing between adjacent banks of combs. This particular actuator design did not self-assemble in the intended fully engaged position due to the low residual stress.

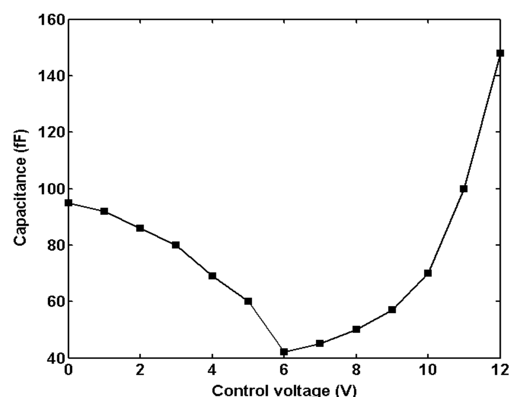

Figure 6. Measured capacitance versus control voltage for a design with full-size actuators in TSMC 0.35 μm process.

CONCLUSIONS

A new CMOS-compatible RF-MEMS tunable capacitor has been designed, fabricated and tested by using AMS 0.6 μm, Agilent 0.5 μm and TSMC 0.35 μm CMOS processes. The essential differences between this work and prior work are the CMOS compatibility and using a maskless CMOS micromachining process. The 2nd-generation tunable capacitor achieves large tuning range up to 352.4%. For future work, the latch mechanism for low power design will be implemented and the reasons for the sticking problem between fingers will be investigated. These efforts will lead to eventual optimization of the tuning range and area efficiency.

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