A Low-Noise Low-Offset Capacitive Sensing Amplifier for a 50-μg/$\sqrt{\text{Hz}}$ Monolithic CMOS MEMS Accelerometer

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Abstract—This paper describes a CMOS capacitive sensing amplifier for a monolithic MEMS accelerometer fabricated by post-CMOS surface micromachining. This chopper stabilized amplifier employs capacitance matching with optimal transistor sizing to minimize sensor noise floor. Offsets due to sensor and circuit are reduced by ac offset calibration and dc offset cancellation based on a differential difference amplifier (DDA). Low-duty-cycle periodic reset is used to establish robust dc bias at the sensing electrodes with low noise. This work shows that continuous-time voltage sensing can achieve lower noise than switched-capacitor charge integration for sensing ultra-small capacitance changes. A prototype accelerometer integrated with this circuit achieves 50-μg/$\sqrt{\text{Hz}}$ acceleration noise floor and 0.02-aF/$\sqrt{\text{Hz}}$ capacitance noise floor while chopped at 1 MHz.

Index Terms—Accelerometer, capacitive sensing amplifier, chopper stabilization, microelectromechanical systems (MEMS).

I. INTRODUCTION

OVER THE PAST decade, a number of monolithic surface micromachined capacitive accelerometers and gyroscopes have been demonstrated and commercialized [1]–[8]. Bulk micromachining [9]–[14] and surface micromachining are the two main technology categories for fabricating microelectromechanical systems (MEMS). Surface micromachining has the advantages of low manufacturing cost and easy integration with microelectronics. Capacitive sensing has low temperature coefficient, low power dissipation, and low noise, can be easily integrated with CMOS for monolithic sensing devices, and is compatible with VLSI technology scaling. The combination of surface micromachining and capacitive sensing is ideal for low-cost single-chip microaccelerometers.

Surface micromachined accelerometers in the current literature have noise floors between 2 μg/$\sqrt{\text{Hz}}$ and 1000 μg/$\sqrt{\text{Hz}}$ [3]–[8]. In most of these surface micromachined accelerometers, except [8], the total noise floor is dominated by electronic noise due to low transducer sensitivity and low sensing capacitance. Important applications of inertial
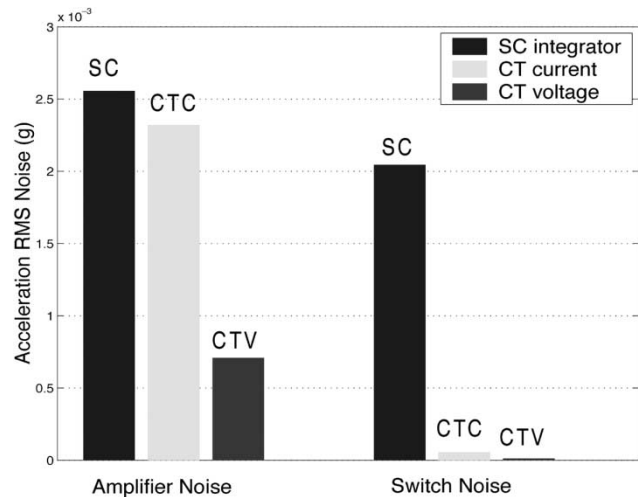
Fig. 1. Noise comparison of three capacitive position sensing methods: SC charge sensing with CDS, continuous-time current sensing and continuous-time voltage sensing. The sensing capacitance is 4 × 20 fF and the interconnect capacitance is 100 fF. The circuit bandwidth is 10× the operating frequency.

measurement such as GPS-aided navigation and virtual reality (VR) require μg resolution at low cost. While lowering mechanical resonant frequency and reducing thermal–mechanical Brownian noise via vacuum packaging may be necessary to reach such performance, low-noise capacitive sensing circuit that reduces the circuit noise below the Brownian noise limit is the crucial first step toward this goal.

The switched-capacitor (SC) charge integration method has been widely used in MEMS capacitive sensor interface circuits [4], [5], [8]–[10], [14], [15]. It is conveniently implemented in CMOS technology and is very robust. The main disadvantage of SC charge integration for low capacitance sensing applications is the high noise floor due to the following three reasons: high kT/C noise at low capacitance; thermal noise of resistive MOS switches; and noise folding in sampled-data systems. Although correlated double sampling (CDS) has been used to significantly reduce the kT/C noise [5], the noise folding and the switch noise still lead to higher noise in an SC sensing circuit than in a continuous-time sensing circuit at the same power dissipation. Fig. 1 shows a comparison of accelerometer input-referred noise of SC charge integration with CDS [5], continuous-time current (CTC) sensing using transimpedance amplifier [16], and continuous-time voltage (CTV) sensing [3], [6], [12], [16], at 4 × 20 fF sensing capacitance. The CTV sensing has superior noise performance compared to the other two methods.

This paper describes the interface circuit design for a monolithic CMOS MEMS accelerometer fabricated by post-CMOS surface micromachining [17]–[19]. The main advantages of the post-CMOS surface micromachining technology are the low interconnect capacitance and resistance between the MEMS and the circuitry. Its main disadvantages are the low sensing capacitance, which is typically lower than 100 fF, and the low capacitance sensitivity, which is typically around 0.4 fF/g. This low sensitivity makes minimization of the input-referred electronic noise a critical task. Due to the low sensing and interconnect capacitance, the low-noise interface circuit design is not simply a task of circuit noise minimization, instead it requires the maximization of the sensor signal-to-noise ratio (SNR) by capacitance matching between the sensor and the circuit.

In this work, CTV sensing with chopper stabilization is employed to reduce the $1/f$ noise, the dc offset, and the noise folding [20]. The sensor input-referred noise is minimized by sizing the input transistors to achieve optimum capacitance matching. A differential difference amplifier (DDA) is used to automatically cancel the dc offset due to circuit mismatch and to calibrate the ac offset due to sensor position mismatch. While the circuit is operating in continuous-time mode, robust dc bias at the high-impedance sensing electrodes is established by low-duty-cycle periodic reset to prevent the undesirable charging and the resulting bias voltage drift problems. This bias scheme provides low-impedance dc path, ultra-high ac impedance above $G\Omega$ level, ultra-small parasitic capacitance below 10 fF, and negligible noise folding at the same time, therefore, minimum noise is injected by the biasing circuit.

In this paper, Section II discusses three main nonidealities, i.e., noise, offset and charging in capacitive position sensing front end, and presents a model of accelerometer input-referred circuit noise. Section III describes the circuit design of the low-noise low-offset capacitive sensing amplifier. Experimental results are presented in Section IV and conclusions are given in Section V.

II. NOISE AND OTHER NONIDEALITIES

Fig. 2 shows noise sources and parasitic components in the capacitive position sensing front end. An accelerometer based on capacitive position sensing is governed by the following equation:

$$V_{\text{sense}} = \frac{2C_s}{2C_s + C_p + C_{gs} + C_{gd}} \cdot \frac{\Delta x}{d} \cdot V_m$$
$$= \frac{2C_s}{2C_s + C_p + C_{gs} + C_{gd}} \cdot \frac{V_m}{\omega_n^2 d} \cdot a. \quad (1)$$

where C_s is the sensing capacitance, C_p is the interconnect parasitic capacitance, C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances of the input MOS transistor, d is the gap distance between stator and rotor sensing electrodes, Δx is the proof-mass displacement to be sensed, V_m is the amplitude of the modulation signal, ω_n is the mechanical resonant frequency of the transducer, and a is the acceleration to be measured. A typical CMOS MEMS accelerometer has 6-kHz resonant frequency, 1.5-μm finger gap, and four 20-fF sensing capacitors in a fully differential configuration, which gives a total
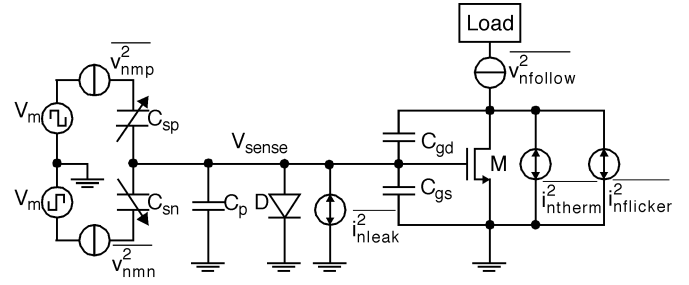

Fig. 2. Noise sources and parasitic components in capacitive position sensing front end.

capacitance sensitivity of 0.4 fF/g. Each of the two differential output has 100-fF interconnect parasitic capacitance. Due to the small sensing and interconnect capacitance, a significant amount of parasitic capacitance is contributed by the sensing circuit. At 1-V modulation signal amplitude, the overall voltage sensitivity is about 1 mV/g.

Electronic noise comes from the following sources: the thermal noise of the input transistor, the $1/f$ (flicker) noise of the input transistor, the shot noise due to leakage current of the diode in the biasing circuit, the noise from the modulation signal, and the noise from the following stages of the circuit. The modulation noise is cancelled by a fully differential capacitive bridge, and the noise leakage due to the imbalance of the bridge is negligible with small capacitance changes. The noise of the input transistor usually dominates over the noise contributed by the rest of the circuit. Therefore, the last two noise sources are neglected in the following discussions. The total voltage noise power spectral density (PSD) at the circuit input is given by [21]

$$\frac{\overline{v_n^2}}{\Delta f}(f) = \frac{\overline{v_{n\text{therm}}^2}}{\Delta f}(f) + \frac{\overline{v_{n\text{flicker}}^2}}{\Delta f}(f) + \frac{\overline{v_{n\text{leak}}^2}}{\Delta f}(f)$$
$$= \frac{K_t T}{W^\beta L^{\beta-1}} + \frac{K_f}{WLf}$$
$$+ \frac{K_s I_{\text{leak}}}{(2C_s + C_p + C_{gs} + C_{gd})^2 f^2} \quad (2)$$

where K_t, K_f, and K_s are the noise coefficients determined by process parameters and bias conditions, W and L are the channel width and length of the input MOS transistor, I_{leak} is the leakage current of the bias diode, T is absolute temperature in Kelvin, and f is the frequency where the circuit operates. In (2), $\beta = 1/2$ for long-channel MOS transistors, $\beta = 1$ for short-channel transistors in deep velocity saturation, and $1/2 < \beta < 1$ for transistors operating between the two extreme conditions [21]. According to (1), the PSD of the input-referred circuit noise in a capacitive accelerometer is given by

$$\frac{\overline{a_n^2}}{\Delta f}(f) = \frac{\overline{a_{n\text{therm}}^2}}{\Delta f}(f) + \frac{\overline{a_{n\text{flicker}}^2}}{\Delta f}(f) + \frac{\overline{a_{n\text{leak}}^2}}{\Delta f}(f)$$
$$= \frac{\omega_n^4 d^2}{4C_s^2 V_m^2} \cdot \left[\frac{K_t (2C_s + C_p + C_{gs} + C_{gd})^2 T}{W^\beta L^{\beta-1}} \right.$$
$$+ \frac{K_f (2C_s + C_p + C_{gs} + C_{gd})^2}{WLf}$$
$$\left. + \frac{K_s I_{\text{leak}}}{f^2} \right]. \quad (3)$$

Because the gate capacitances of MOS transistors are proportional to the channel width

$$C_{gs} + C_{gd} = \left(\frac{2}{3}L + 2L_{\text{ov}}\right)W = c_g W \qquad (4)$$

where L_{ov} is gate–source and gate–drain overlap distance, the acceleration noise floor can be rewritten as

$$\frac{\overline{a_n^2}}{\Delta f}(f) \propto \frac{K_t(2C_s + C_p + c_g W)^2 T}{W^\beta L^{\beta-1}}$$
$$+ \frac{K_f(2C_s + C_p + c_g W)^2}{WLf} + \frac{K_s I_{\text{leak}}}{f^2}. \qquad (5)$$

Equation (5) shows that the input-referred noise floor of a capacitive accelerometer is a function of both operating frequency and input transistor sizing. Unlike typical low-noise circuit design, even though increasing the size of the input MOS transistor reduces the thermal noise and the $1/f$ noise, it also increases the parasitic capacitance of the capacitive sensor and reduces the sensitivity. Therefore, there is an optimum transistor size that maximizes the SNR and minimizes the input-referred noise floor at each frequency. By setting the following derivative to zero

$$\frac{\partial}{\partial W}\left(\frac{\overline{a_n^2}(f)}{\Delta f}\right) = 0 \qquad (6)$$

the optimum transistor width is found to be:

$$W_{\text{opt}} = \eta \cdot \frac{2C_s + C_p}{c_g} \qquad (7)$$

which leads to the capacitance matching equation:

$$C_{gs} + C_{gd} = \eta(2C_s + C_p) \qquad (8)$$

where $\eta = 1$ for MOS transistors that are dominated by $1/f$ noise or in deep velocity saturation region, $\eta = 1/3$ for ideal long-channel transistors dominated by thermal noise, and $1/3 < \eta < 1$ for most practical situations. The capacitance matching equation (8) suggests that the gate capacitance must be equal or smaller than the combined sensing and interconnect capacitance to achieve maximum SNR and minimum input-referred noise floor. In many bulk and surface micromachining technologies, the interconnect parasitic capacitance is dominant such that capacitance matching could be ignored. In the post-CMOS surface micromachining technology, because the combined sensing and interconnect capacitance is usually smaller than 200 fF, the capacitance matching is important in guiding the interface circuit design where relatively small transistor size is used.

The minimum achievable accelerometer input-referred noise floor can be calculated from (3), (7), and (8). If the noise is dominated by $1/f$ noise, the minimum noise floor is given by

$$\frac{\overline{a_{n\,\min}^2}}{\Delta f}(f) = \frac{\omega_n^4 d^2 K_f(2C_s + C_p)\left(\frac{2}{3} + \frac{2L_{\text{ov}}}{L}\right)}{V_m^2 C_s^2 f}. \qquad (9)$$

If the noise floor is dominated by thermal noise of the long-channel MOS transistor, the minimum noise floor is

$$\frac{\overline{a_{n\,\min}^2}}{\Delta f}(f) = \frac{4\omega_n^4 d^2 K_t T(2C_s + C_p)^{\frac{3}{2}} L\sqrt{\frac{2}{3} + \frac{2L_{\text{ov}}}{L}}}{\sqrt{27}V_m^2 C_s^2}. \qquad (10)$$

If the noise floor is dominated by thermal noise of the short-channel MOS transistor in deep velocity saturation region, the minimum noise floor is

$$\frac{\overline{a_{n\,\min}^2}}{\Delta f}(f) = \frac{\omega_n^4 d^2 K_t T(2C_s + C_p)L\left(\frac{2}{3} + \frac{2L_{\text{ov}}}{L}\right)}{V_m^2 C_s^2}. \qquad (11)$$

In the above equations, C_s, C_p, ω_n, d, V_m, and L_{ov} are process parameters of the particular MEMS and IC technology, while K_t, K_f, and K_s are also mainly determined by the technology and are only weakly related to the bias condition. Because L_{ov} is much smaller than L, the transistor length L does not have significant effect on the $1/f$ noise and has a near linear relationship with the thermal noise. Therefore, minimum length will always be used to minimize the noise floor. This leaves the transistor width W as the only design variable for noise optimization and the value of the transistor width will be chosen based on the capacitance matching equations (7) and (8). According to (10), the theoretical limit of circuit noise in a typical CMOS MEMS accelerometer is 8 μg/$\sqrt{\text{Hz}}$ for 0.5-mA bias current. Due to the remnant $1/f$ noise and the short-channel effects, the actual limit will be higher than this number.

Fig. 3 plots the input-referred noise floor in a typical CMOS MEMS accelerometer with a pair of NMOS input transistors biased at 0.5 mA. It shows that the optimum width is smaller than 100 μm for 0.5 μm channel length, and under such condition, the $1/f$ noise is significant up to 10 MHz. As shown in Fig. 3(c), the minimum achievable circuit noise floor intersects the Brownian noise floor between 1–2 MHz. Operating the circuit above this frequency will not further improve the overall sensor noise performance because the Brownian noise starts to dominate. Although PMOS transistors are often chosen due to the lower $1/f$ noise, for this particular CMOS process, simulations show that the NMOS transistors achieve lower minimum input-referred noise floor than the PMOS transistors at frequencies above 500 kHz.

Offset is another major nonideality in microcapacitive accelerometers. There are two types of offsets: the dc offset due to circuit mismatch, and the ac offset at the modulation frequency due to sensor position offset. The mechanical and electrical sensitivities of a typical CMOS MEMS accelerometer are about 10 nm/g and 1 mV/g. In a 0.5-μm CMOS technology, the sensor position error due to lithography misalignment and post-CMOS structure release could be much greater than 100 nm. The CMOS circuit offset with the transistor size required by capacitance matching could be larger than 10 mV. Therefore, both circuit and sensor offsets may be greater than 10 g and larger than the full measurement range of the microaccelerometer. The sensor interface circuit must be able to suppress these ac and dc offsets in order to prevent them from blocking the signal and degrading the dynamic range.

Charging is the charge leakage to or from the sensing electrodes. It is a unique problem in CTV sensing circuits where the sensing electrodes have very high impedance. This is not an issue in SC charge-mode sensing where the charge is released in every clock cycle. If not suppressed, charging may cause drift of the input bias voltage and even completely swamp the circuit. In the past, the sensing nodes have been biased by reverse-biased diodes, subthreshold MOS transistors,
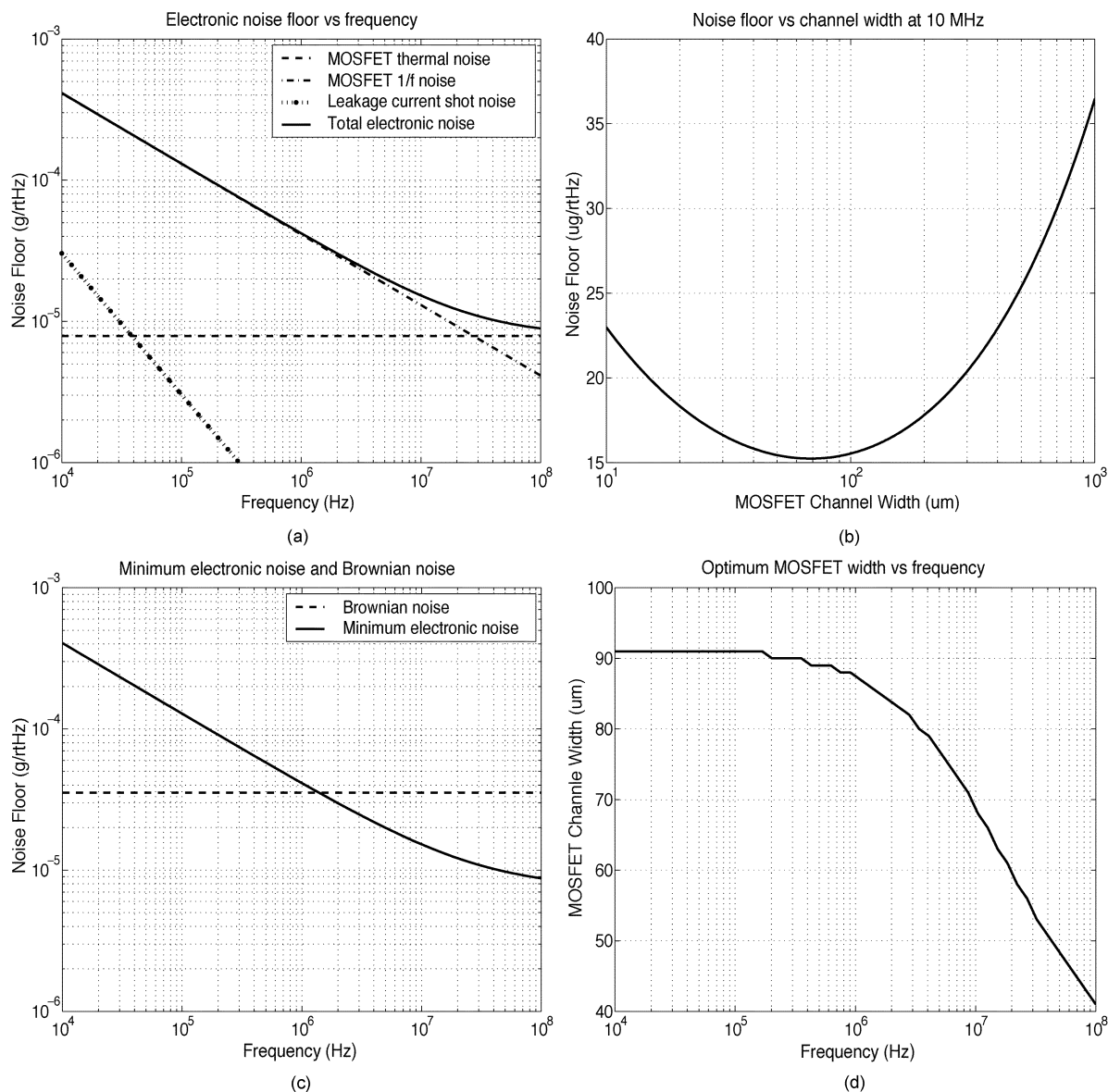
Fig. 3. Input-referred circuit noise floor: (a) noise components versus modulation frequency; (b) noise floor versus NMOS transistor channel width at 10 MHz with channel length of 0.5 μm; (c) minimum circuit noise floor and Brownian noise floor versus modulation frequency; (d) optimum channel width versus modulation frequency. The sensing capacitance is 4 × 20 fF and the interconnect capacitance is 100 fF.

long-channel MOS transistors, and large resistors [6], [7], [16], [18], [19]. The main tradeoff is that the biasing device must provide a robust dc charge-release path to suppress the charging effectively, meanwhile it must have high ac impedance and small parasitic capacitance at the same time to get lower noise, less signal attenuation, and higher SNR. In a typical CMOS MEMS accelerometer, the total capacitance at the sensing electrodes is 250 fF, which leads to an impedance value of 640 kΩ at 1 MHz. A leakage current of 1 pA could result in voltage drift of 4 V within 1 s. To ensure less than 10% of signal attenuation, the ac impedance of the biasing device must be greater than 6.4 MΩ, and a resistor of such a high value usually possesses large parasitic capacitance which would cause large signal attenuation in a capacitive sensing circuit. In conclusion, CTV-mode sensing offers potentially improved SNR compared to SC charge-mode sensing circuits; however, the noise due to the biasing circuit must be taken into account in determining the

best overall front end design, and to bias the sensing electrodes with robust dc path, high ac impedance and small parasitic capacitance simultaneously is a major challenge.

III. CIRCUIT DESIGN

The low signal level in CMOS MEMS accelerometers demands that the SNR of the interface circuit be maximized. A CTV sensing amplifier is designed so that the noise is not limited by the noise folding and the switch noise. To avoid the $1/f$ noise and the dc offset, chopper stabilization is used and the circuit operates at frequencies from 50 kHz up to 3 MHz, which is the frequency where the Brownian noise starts to dominate.

The block diagram of the sensing amplifier is shown in Fig. 4. A fully differential topology with a full-bridge capacitive sensor is employed to reject common-mode noise and power supply
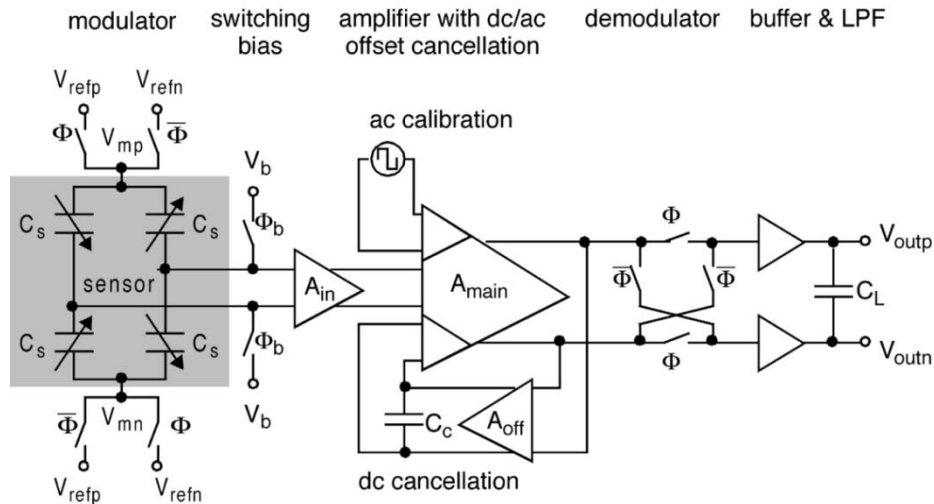
Fig. 4.   Block diagram of the capacitive sensing amplifier.

noise. The dc bias of the amplifier input is established by periodic reset with low duty cycle. The amplifier uses a two-stage configuration. The first stage is optimized for noise and provides only a small gain. Because the capacitance matching requires that the input transistors have relatively small sizes, the two-stage design relieves the input transistors from providing large transconductance so that the input-referred noise floor and the SNR can be optimized without other design constraints. Most of the gain is provided by the second stage. The total voltage gain of the circuit is about 42 dB, which gives an overall sensor gain of 130 mV/g. In order to investigate the frequency dependence of the sensor noise, the amplifier is designed with 3-dB bandwidth of 3 MHz. The second stage is a three-input DDA. A dc feedback loop is formed by one auxiliary input of the DDA, a low-bandwidth offset amplifier, and an external capacitor to cancel the dc offset. The ac offset is cancelled by sending a calibration signal to the other auxiliary input. The sensed signal is a narrow-band signal modulated at the chopping frequency. After amplification, the signal is demodulated by a passive demodulator into the baseband. The output signal bandwidth is 2 kHz.

The square-wave modulation signals and the bias reset signal are generated on-chip by MOS switches. The fully differential modulation is realized by switching between two dc reference voltages. The reference voltages are bypassed by large external capacitors to ensure the modulation signals contain very low noise at the chopping frequency. The sensing electrodes are reset to a dc voltage every 16 modulation clock cycles. As in the SC sensing circuit, by releasing charge periodically from the high-impedance electrodes, this switching bias method suppresses the undesirable charging and eliminates the bias voltage drift caused by charging. Unlike the SC circuit, by resetting every 16 clock cycles, the noise folding is reduced by a factor of 16 because the reset frequency is 1/16 of the modulation frequency. The generator circuit and timing diagram of the modulation and bias reset signals are shown in Fig. 5. The modulation is turned off during the reset. Otherwise, a signal-dependent offset will be present. Minimum-sized PMOS transistors are used as the reset switches to minimize both the
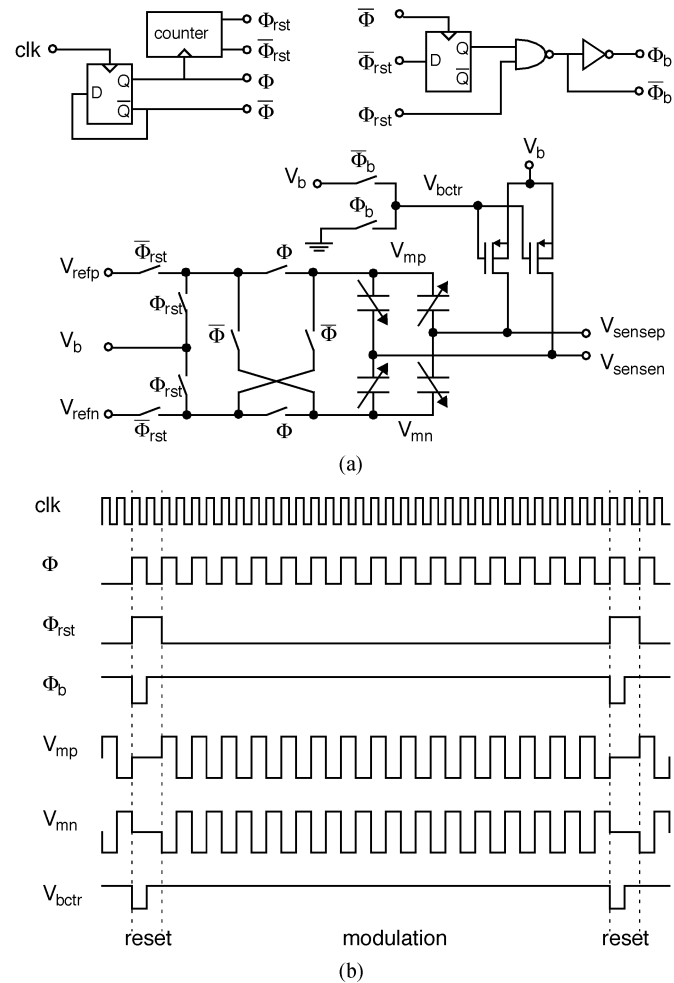

Fig. 5.   (a) Generator and (b) timing diagram of the modulation and bias reset signals.

leakage current and the parasitic capacitance. The ac impedance of the bias circuit is determined by the off-resistance of the PMOS reset switch which is above the GΩ level. The parasitic capacitance of the bias circuit is the drain junction capacitance
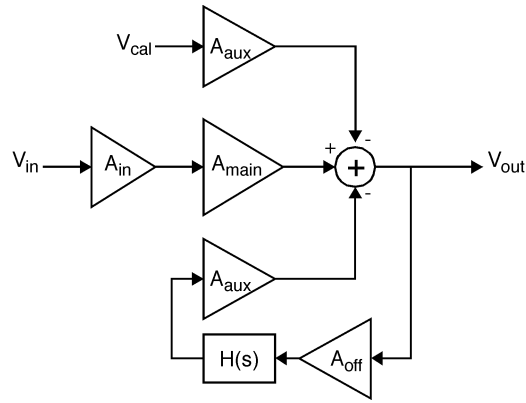
Fig. 6. Cancellation of circuit dc offset and sensor ac offset.

Fig. 7. Two-stage wide-band differential difference amplifier with offset cancellation.

of the minimum-sized PMOS switch which is smaller than 10 fF. Compared to other biasing methods, this switching bias scheme effectively achieves low-impedance dc path, ultra-high ac impedance, and ultra-small parasitic capacitance at the same time, without the penalty of noise folding.

Fig. 6 shows a signal flow diagram of the two-stage three-input DDA. The input signal can be partitioned as

$$V_{\text{in}} = V_{\text{sig}} + V_{\text{dc}} + V_{\text{ac}}, \qquad (12)$$

where V_{sig}, V_{dc}, and V_{ac} represent the signal, the input-referred dc offset, and the input-referred ac offset, respectively. The output voltage of the DDA is then given by

$$
\begin{aligned}
V_{\text{out}} &= \frac{A_{\text{in}} A_{\text{main}} V_{\text{in}} - A_{\text{aux}} V_{\text{cal}}}{1 + A_{\text{off}} A_{\text{aux}} H(f)} \\
&\approx A_{\text{in}} A_{\text{main}} V_{\text{sig}} + \frac{A_{\text{in}} A_{\text{main}} V_{\text{dc}}}{1 + A_{\text{off}} A_{\text{aux}}} \\
&\quad + \left(A_{\text{in}} A_{\text{main}} V_{\text{ac}} - A_{\text{aux}} V_{\text{cal}} \right)
\end{aligned}
\qquad (13)
$$

where $H(f)$ is the low-pass transfer function of the dc feedback path. Due to the dc feedback, the sensing amplifier has a band-pass frequency response which attenuates the output dc offset by the open-loop gain of the dc feedback loop. The low frequency corner is set at 10 kHz such that both the signal and the ac offset are not affected. In a dc accelerometer, the sensor offset appears as an ac offset modulated at the same frequency as the signal, and must be removed by calibration. After the sensor calibration, a calibration signal V_{cal} is sent to the other auxiliary input of the DDA to remove the ac offset by forcing the last term in (13) to zero.

The transistor-level schematic of the two-stage three-input amplifier is shown in Fig. 7. Because the circuit is implemented by a standard digital CMOS process which does not provide high-performance resistors and capacitors, the use of on-chip passive components is avoided. The input buffer is a NMOS differential low-gain stage with diode-connected NMOS transistor load. The NMOS implementation is chosen because simulations show it gives lower input-referred noise floor above 500 kHz than using PMOS input transistors. The size of the input transistors is determined to be 80 μm/0.5 μm based on capacitance matching equation (7) at 1 MHz. The width and length of the load transistors are chosen so that both the thermal noise and the $1/f$ noise are dominated by the input transistors. The second stage is an operational transconductance amplifier (OTA) with
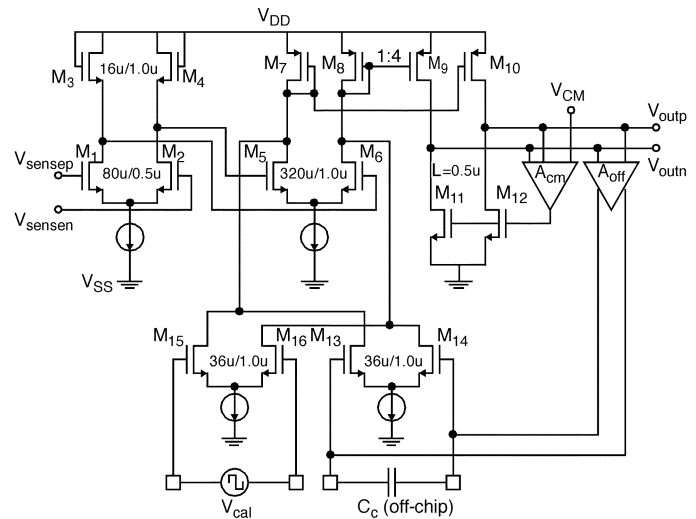
three input differential pairs to realize the DDA function. One key design consideration is that the transistors used in the two auxiliary inputs have smaller size, hence smaller transconductance, than the main input transistors. This reduces the noise contribution of the auxiliary inputs. The common-mode feedback loop employs a high-bandwidth common-mode amplifier that stabilizes the output common-mode voltage of the high-gain second stage. A high-gain low-bandwidth offset amplifier forms the dc feedback loop with a large external capacitor that provides the band-pass closed-loop frequency response to cancel the dc offset. The overall amplifier has a 3-dB high-frequency corner at 3 MHz that is limited by the second-stage bandwidth, and a 3-dB low-frequency corner at 10 kHz which is set by the dc feedback loop.

IV. EXPERIMENTAL RESULTS

A monolithic CMOS MEMS accelerometer with the above capacitive sensing amplifier has been fabricated in Agilent's three-metal one-poly 0.5-μm CMOS technology followed by post-CMOS surface micromachining [17]. In the post-CMOS processing, the top metal layer is used as the mask for etching SiO_2 and Si. Thus, the circuit is implemented with two metal layers and is covered by the top metal layer for protection. Fig. 8 shows the die micrograph. The circuit area is under the top metal cover and could not be seen in the micrograph. The scanning electron micrograph (SEM) of a released accelerometer is shown in Fig. 9.

The acceleration measurements are made on a vibration table which generates a single-frequency acceleration signal. A reference accelerometer with 1-V/g sensitivity is mounted on the vibration table so that the sensitivity and the input-referred noise floor of the prototype accelerometer can be calculated by comparing to the reference. An off-chip low-noise instrumentation amplifier converts the differential output signals from the accelerometer chip into a single-ended signal and provides an additional gain up to 25. The single-ended measurement takes place at the output of the instrumentation amplifier. Fig. 10 shows the measured output signal and the reference signal in
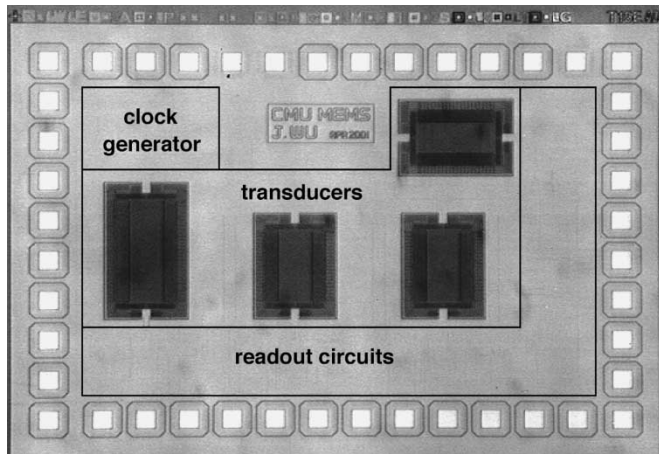
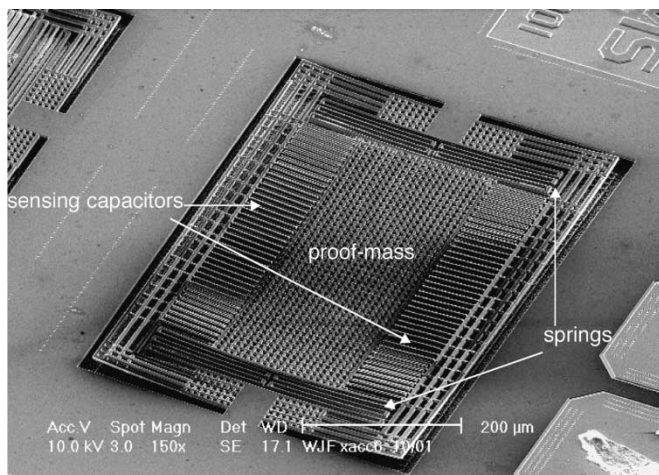Fig. 8.   Die micrograph with circuit covered by top metal layer.

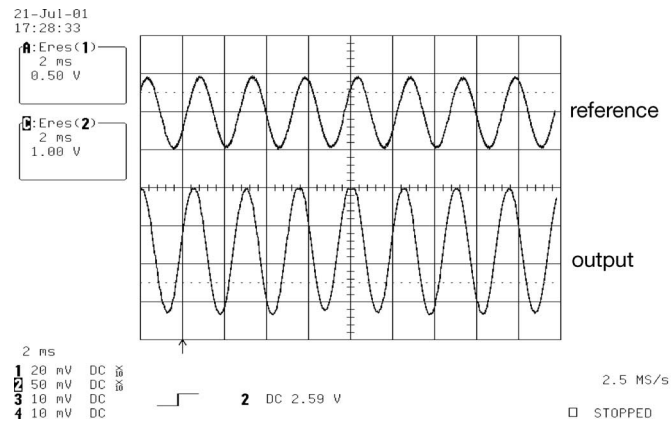Fig. 9.   SEM of a released CMOS MEMS accelerometer.

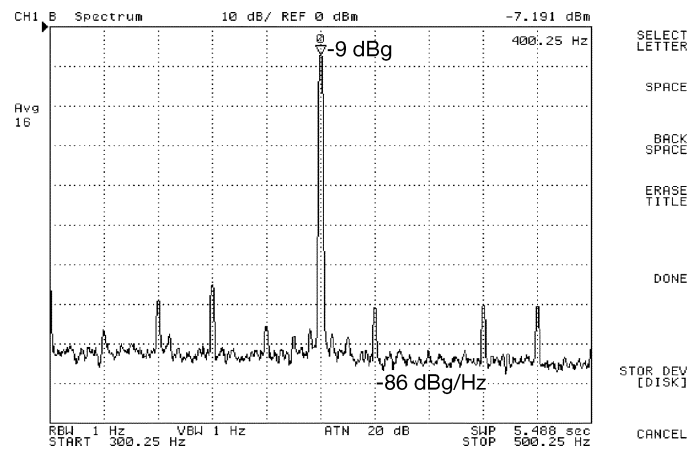Fig. 10.   Output and reference waveforms with 0.5-g 400-Hz sinusoidal acceleration.

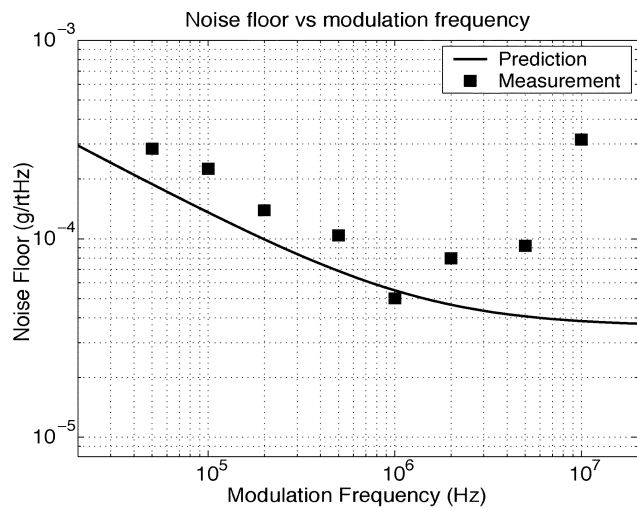Fig. 11.   Output spectrum with 0.5-g 400-Hz sinusoidal acceleration.

Fig. 12.   Accelerometer input-referred noise floor versus modulation frequency.

response to a 400-Hz 0.5-g sinusoidal acceleration. The combined sensitivity of the test chip and the off-chip amplifier is 3.2 V/g. Thus, the sensitivity of this integrated accelerometer is 130 mV/g. The mechanical resonant frequency of the accelerometer is 5.8 kHz. The total harmonic distortion (THD) measured with the 0.5-g sinusoidal acceleration is lower than −60 dB, or 0.1%. The distortion increases to −20 dB, or 10%, at 6 g. The linear range is mainly limited by the output saturation of the high-gain readout circuit in the open-loop accelerometer. Significant improvement of the sensor linear range is expected if the accelerometer is enclosed in a force-balanced feedback loop [19].

Fig. 11 shows the output spectrum with a 400-Hz 0.5-g sinusoidal input acceleration at a modulation frequency of 1 MHz. Defining the power of 1-g-rms acceleration as 0 dBg, the power of the 0.5-g amplitude sinusoidal acceleration is −9 dBg. As shown in Fig. 11, the output noise power spectral density is −77 dB below the signal level at −86 dBg/Hz, which corresponds to an input-referred noise floor of 50 $\mu g/\sqrt{Hz}$. The equivalent noise floors in capacitance and displacement are 0.02 $aF/\sqrt{Hz}$ and 500 $fm/\sqrt{Hz}$, respectively. The calculated Brownian noise of the transducer is 30 $\mu g/\sqrt{Hz}$. Therefore, the circuit noise level is close to the Brownian noise limit. Fig. 11 also shows spurs smaller than −70 dBg at 340, 360, 420, 460,

and 480 Hz. These are the harmonics of the 60-Hz power line interference and the intermodulation products of the power line interference with the 400-Hz signal from the single-ended measurement setup.

The accelerometer noise is measured with the modulation frequency varying from 50 kHz to 10 MHz. Fig. 12 compares
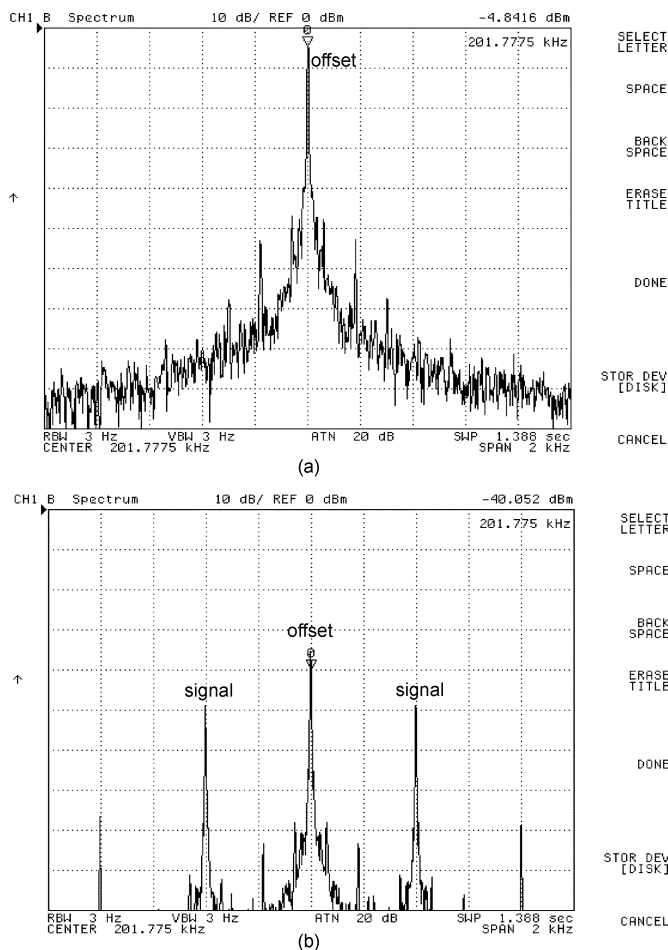
Fig. 13. Signal spectrums prior to demodulation: (a) the signal is blocked by the ac sensor offset; (b) the signal emerges after the sensor offset is reduced.
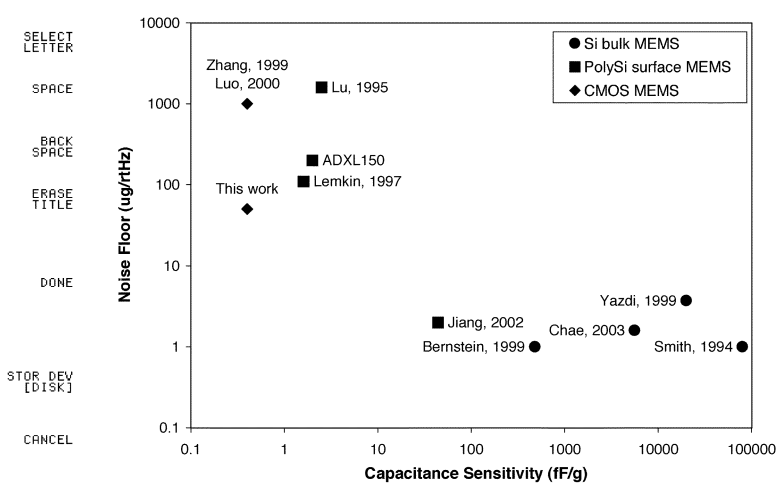

Fig. 14. Comparison of noise floor versus capacitance sensitivity of recently reported MEMS accelerometers.

the measured noise floor versus modulation frequency with the values calculated by (3). The model prediction shows reasonable agreement with the measured results. The noise decreases with frequency from 50 kHz to 1 MHz due to the significant $1/f$ noise in the MOS input transistors. Above 1 MHz, the noise no longer decreases as the Brownian noise starts to dominate. In fact, the input-referred noise increases because the signal is attenuated by incomplete settling due to the bandwidth limit in the second stage amplifier. The minimum noise floor is achieved at 1 MHz.

The dc offset voltage measured at the output of the offset amplifier is 0.1 V and the equivalent input-referred dc offset voltage is $10\,\mu V$. The cancellation of the ac sensor offset is done by adjusting the calibration signal generated on the test board. Fig. 13 shows the single-ended spectrums of the signal prior to the demodulation with and without the offset calibration at 200-kHz modulation frequency. They demonstrate that greater than 40 dB of sensor offset reduction can be achieved by calibration. As shown in Fig. 13(a), without offset cancellation, the signal is completely blocked by the offset due to the saturation within the amplifier. In Fig. 13(b), with offset greatly reduced, the signal components emerge. Because of the singled-ended measurement, significant offset and even-order spurs appear in Fig. 13(b). The actual offset and even-order distortions are much smaller in the differential signal and the demodulated output.

TABLE I
SUMMARY OF ACCELEROMETER CHARACTERISTICS

Parameters	Measured values
Sensitivity	130 mV/g
Noise floor	50 μg/$\sqrt{\text{Hz}}$ @ 400 Hz (1 MHz modulation)
Linear range	+/- 6 g
Sensor offset reduction	> 40 dB
Circuit dc offset	10 μV
Sensing capacitance	4 x 20 fF
Capacitance sensitivity	0.4 fF/g
Capacitance noise floor	0.02 aF/$\sqrt{\text{Hz}}$
Resonant frequency	5.8 KHz
Sensor bandwidth	2 KHz
Modulation frequency	50 KHz - 2 MHz
Supply voltage	5 V
Current consumption	6 mA
Chip area	3.5 mm x 2.5 mm
Sensor area	600 μm x 450 μm
Technology	0.5 μm 3M1P CMOS + CMOS-MEMS

V. CONCLUSION

The characteristics of the monolithic CMOS MEMS accelerometer are summarized in Table I. By employing the low-noise low-offset capacitive sensing amplifier described in this paper, it achieves 50 μg/$\sqrt{\text{Hz}}$ and 0.02 aF/$\sqrt{\text{Hz}}$ noise floor and >40-dB reduction of sensor offset with total sensing capacitance smaller than 100 fF and capacitance sensitivity around 0.4 fF/g.

Fig. 14 compares the noise floor versus capacitance sensitivity in recent published MEMS accelerometers. By exploiting low-noise circuit design techniques for sensing ultra-small capacitance changes, including capacitance matching, chopper

stabilization and low-duty-cycle periodic reset biasing, this work achieves very good relative noise performance.

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