Micromachined High-Q Inductors in a 0.18-μm Copper Interconnect Low-K Dielectric CMOS Process

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Abstract—On-chip spiral micromachined inductors fabricated in a 0.18-μm digital CMOS process with 6-level copper interconnect and low-K dielectric are described. A post-CMOS maskless micromachining process compatible with the CMOS materials and design rules has been developed to create inductors suspended above the substrate with the inter-turn dielectric removed. Such inductors have higher quality factors as substrate losses are eliminated by silicon removal and increased self-resonant frequency due to reduction of inter-turn and substrate parasitic capacitances. Quality factors up to 12 were obtained for a 3.2-nH micromachined inductor at 7.5 GHz. Improvements of up to 180% in maximum quality factor, along with 40%–70% increase in self-resonant frequency were seen over conventional inductors. The effects of micromachining on inductor performance was modeled using a physics-based model with predictive capability. The model was verified by measurements at various stages of the post-CMOS processing. Micromachined inductor quality factor is limited by series resistance up to a predicted metal thickness of between 6–10 μm.

Index Terms—CMOS micromachining, modeling, monolithic inductors, quality factor, RFIC, self-resonance, silicon integrated circuit technology, substrate loss.

I. INTRODUCTION

ADVANCES in silicon technology, with decreasing feature sizes and application of novel materials, are pushing circuit performance to higher frequencies. The new digital 0.18-μm interconnect CMOS process with high f_t transistors is highly attractive for RF design for mass produced wireless communication products [1]. Interconnect resistance traditionally has not received attention in a digital CMOS process, but as modern digital designs have begun to be limited by interconnect delays, more interest has been seen [2]. Copper interconnect has been introduced to lower the interconnect resistance to reduce interconnect delay. This is an advantageous trend for RF circuit designers as better quality on-chip passives [3] can be designed with lower series resistance. High-Q inductors can lead to improved power or figure of merit in low noise amplifiers (LNA), lower insertion loss in bandpass filters, and better phase noise and power in voltage controlled oscillators (VCO) [4].

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Inductors are intended to store magnetic energy, however, the finite coil resistance and the substrate losses in silicon contribute to energy losses and hence reduce the quality factor Q. Energy losses in the silicon substrate result from I^2R losses due to the currents flowing through the metal to substrate capacitance and those generated due to magnetic field induced by the inductor. These losses can be eliminated by either shorting the substrate or making it open.

Solid ground shields that help to reduce the substrate resistance induce opposite flowing loop currents due to Lenz's law. These currents produce a negative mutual coupling that reduces the magnetic field and decreases the overall inductance. One approach suggested by Yue and Wong [5] is the use of patterned ground shield that reduces the induced loop current by insertion of slots in the shield. The main drawback of this technique is that the parasitic capacitance to substrate is significantly increased. Patterned ground shields are effective for lower frequency applications where the parasitic capacitance can be absorbed in the LC tank. Increasing the substrate resistance is another approach that is useful for reducing substrate losses. The use of high resistivity silicon [6] and sapphire substrates have been used by researchers to demonstrate high-Q planar inductors, achieving quality factors of 40 at 5.8 GHz for an 1.4-nH inductor [7]. However, the use of high resistivity material is not common in a digital logic CMOS process, and many submicron CMOS technologies use epitaxial silicon wafers. Substrate removal is a method of choice for large area inductors in which improvement in self-resonant frequency extends the usable frequency range. Chang *et al.* [8] proposed elimination of substrate losses in large area inductors by removing the underlying silicon using front-side etching of silicon in a post-processing step. The post-processing step either removed the silicon by wet etching or by using gaseous dry etching [9]. These techniques have inherent limitations as to how far circuits can be placed from the inductor, introducing I^2R losses in the interconnect resistance. The distance of the transistors from the inductor is determined by the dimensions of the inductor and the time of the etch. Other approaches to eliminate silicon from below the inductor have used back-side etching techniques [10]. Research has also aimed to integrate micromachined inductors using custom fabrication techniques on the bottom of the CMOS chip [11] and on GaAs substrates [12].

In this paper, we present an approach to improve the performance of inductors fabricated in a digital logic process with copper interconnect and low-K dielectric by use of maskless post-processing steps [13]. Removal of the underlying silicon
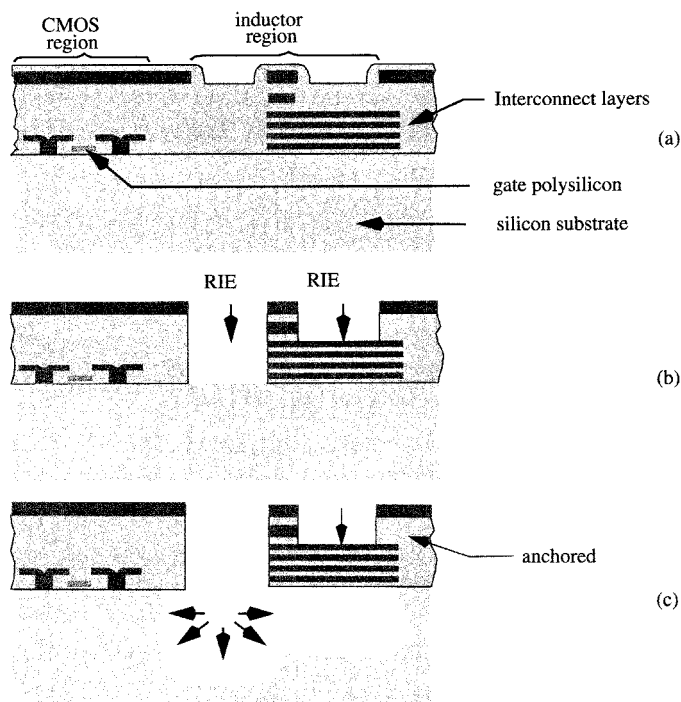
Fig. 1. Cross-section of the post process steps in the fabrication process. (a) The conventional CMOS die from the foundry. (b) After removal of sidewall oxide. (c) After silicon substrate removal due and anisotropic and an isotropic etch.

Fig. 2. Scanning electron micrograph of a single side anchored micromachined inductor.

and the inter-turn sidewall oxide helps reduce the substrate losses that dominate at higher frequencies, increase the self-resonant frequency, and also reduce substrate noise coupling into the inductor. This technique leverages the ever-increasing number of interconnect layers used in modern processes for passive designs [14] for lower series resistance without severe high-frequency performance penalties. Section II describes the processing steps and their impact on circuit design and layout. The mechanical stability of a suspended inductor to external shock and temperature changes has been investigated using finite element modeling. Section III describes a physical model of the inductors that was developed to understand the performance gains due to micromachining. Measurement results compare the performance of the micromachined inductor to conventional on-chip inductors, with and without the sidewall oxide. Section IV presents a discussion of the results and Section V draws some conclusions based on this work.

II. DESIGN CONSIDERATIONS

A 0.18-μm minimum feature size CMOS process with copper interconnect and low-K dielectrics was used to fabricate the inductors. The process flow, shown in Fig. 1, enables fabrication of micromachined structures in CMOS. The conventional CMOS processing [Fig. 1(a)] is followed by anisotropic reactive ion etching (RIE) with CHF_3 and O_2 to remove oxide not covered by any of the metal layers, resulting in high-aspect-ratio vertical sidewalls [Fig. 1(b)]. The following anisotropic and isotropic silicon etch [Fig. 1(c)] removes the underlying silicon to release the microstructure. The anisotropic etch is used to obtain the desired spacing between the inductor and the substrate. The subsequent isotropic etch undercuts the silicon be-
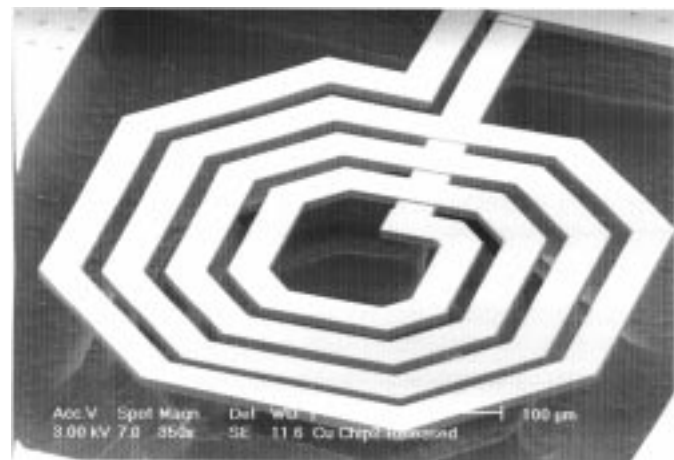
neath the inductor. The details of the process are described in [15] and [16].

Circuits can be placed about 30 μm away from the edge of the silicon pit, and this design rule is independent of the depth of the silicon pit. The circuits are protected by the top metal of the CMOS process. This is a disadvantage as top metal cannot be used for arbitrary interconnect and is grounded. The maximum width of a metal-masked feature is about 30 μm. The smallest width is limited by the processing conditions to about 1.5 μm.

The electrical performance of the circuits is not affected by the etching steps. Inverter test structures were tested before and after the micromachining process. A 2.2-GHz single *LC* tank oscillator was tested to verify the operation of the transistors after the post-process step. The oscillator used a 3-nH single suspended inductor. The circuit consumed 10.2 mA with a supply voltage of 1.7 V.

A. Inductor Structure

A scanning electron microscope image of a suspended inductor with single sided connection is shown in Fig. 2. The inductor coil is designed with four 20-μm-wide turns using metal-5 and metal-6 layers, which are the thickest (0.5 μm) layers available in the process. The two layers are shunted together to reduce the series resistance of the coil. The return conductor consists of the metal 4,3,2,1 layers shunted together. Inductor geometries were optimized using FASTHENRY [17] with a parametric inductor layout and input deck generator.

B. Mechanical Stability of the Suspended Inductor

One concern in design of mechanical suspended inductors is that external shocks and mechanical deformations of the inductor structure change the inductance and hence affect the circuit performance. Residual stress differences in various films used in the interconnect fabrication cause the inductors to curl out of plane, such that the highest point of the inductor is above the plane of the chip. This out-of-plane curl is a function of the dimensions of the inductor and temperature. The variation of inductor performance with temperature has been studied by researchers [18] for conventional on-chip inductors. Additional mechanical effects occur in suspended inductors that should be

TABLE I
SUMMARY OF MECHANICAL EFFECTS IN SUSPENDED INDUCTORS

Simulation result	Single anchored inductor	Double anchored inductor
Nominal Inductance (nH)	4.824	4.918
Inductor dimensions	400μm by 400μm	400μm by 400μm
Maximum out of plane curl (μm)	25.10	15.94
% Inductance change due to curl	-0.0070	-0.1036
1st Mechanical mode (kHz)	8.71	9.31
2nd Mechanical mode (kHz)	16.27	21.71
3rd Mechanical mode (kHz)	22.07	22.22
Temperature coefficient of inductance (ppm/°C)	0.757	11.139
% Inductance change due to 100G shock	-0.0162	-0.0173
Maximum deflection due to 100G shock (μm)	0.5011	0.4543

taken into account. Finite element simulations were carried out to verify the mechanical stability of the suspended inductors and curling due to residual stress and temperature. To the first order, the change of out-of-plane curl (Δz) of such structures is proportional to the temperature increase (ΔT), cube of the total thickness of the interconnect stack (t_s), and square of the distance from the anchor (l). The proportionality constant K_0 is a function of material properties of the interconnect stack [19].

$$\Delta z = \frac{K_0 l^2}{t_s^3} \Delta T. \qquad (1)$$

Two square (400 μm by 400 μm) inductors with single-sided and double-sided suspension and five turns were analyzed. Thermomechanical simulations [20] were followed by FAS-THENRY [17] simulations to compute the inductance after deformation. External shock to the inductor was simulated by subjecting the inductor structure to a static acceleration of 9810 m/s^2 (100 G) and calculating the inductance change. Motion due to external shock is very small ($\sim$0.5 μm) due to the extremely small mass of the inductor, on the order of 1 μg. The natural mechanical frequencies, which potentially can amplify the displacement from a shock, and can frequency modulate the center frequency of a VCO, were simulated. The first three mechanical vibration modes of the device are low frequency (8–23 kHz), and the effect of these modes can be compensated in the design of the phase-locked loop (PLL) by a large loop gain. The higher frequency mechanical modes are difficult to excite in a packaged inductor due to the mechanical damping of the package. These resonances can be moved to higher frequencies by increasing the number of anchors. Table I summarizes the results of the mechanical simulation. The suspended inductors have a low mechanical dependence on inductance with temperature change because the relative displacement between adjacent turns is very small compared to the dimensions of the structure. The relative displacement between the turns is smaller in a single-suspended cantilever inductor, compared to the double-suspended inductor, even though the former has larger overall curl. This results in a lower inductance reduction for the single-sided inductor after release.
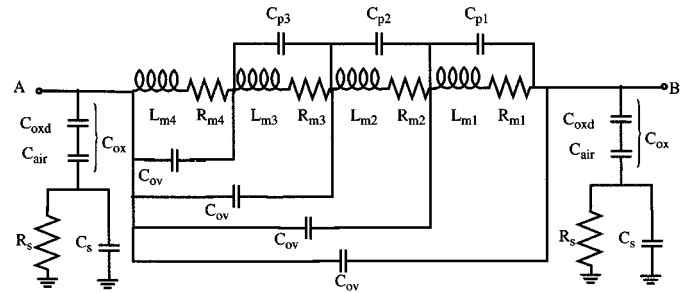

Fig. 3. Lumped parameter equivalent circuit for the inductor, which includes parasitic sidewall capacitance and substrate loss.

III. DEVICE MODELING AND CHARACTERIZATION

To understand the improvement due to substrate and the sidewall oxide removal, an equivalent circuit model based on physical principles is proposed. The schematic of the model for a four-turn inductor is shown in Fig. 3 and is an extension of models proposed earlier in the literature [21]. Each turn of the inductor has been modeled as a separate *LCR* segment to account for the contribution of inter-turn capacitances to the resonant frequency. Contribution of the inter-turn capacitance has been considered insignificant in the modeling of nonmicromachined inductors.

A. Inductor Model

To accommodate the effects of inter-turn capacitance, the inductance (L_{mn}) and the series (R_{mn}) resistance due to each turn are modeled separately [22] and are expressed as

$$L_{mn} = L_m \left(\frac{l_n}{l_m} \right)$$
$$R_{mn}(f) = R_m(f) \left(\frac{l_n}{l_m} \right) \qquad (2)$$

where L_{mn} is the inductance of the nth turn of the inductor, L_m is the total inductance, l_m is the total length of conductors, l_n is the length of the nth turn, and $R_m(f)$ is the series

resistance of the inductor. The total inductance value was estimated from finite element simulations using FASTHENRY. A constant inductance per unit length was assumed for all the spirals.

At dc, the resistance can be computed from the dimensions of the coil and conductivity of the interconnect material. However, at higher frequencies the series resistance of the inductor is dependent on frequency due to skin effects, and current crowding issues due to magnetic effects [23]. The situation is further complicated by the use of two parallel conductors that are electrically shunted together to form the inductor spiral. The application of analytical expressions derived in [21] and [24], and has been used to model the series resistance. The series resistance of each segment is modeled as

$$R_m(f) = R_{dc}\left(\frac{l_n}{l_m}\right)\frac{\frac{t_c}{\delta}}{1 - e^{-(t_c/\delta)}}$$

$$= R_{dc}\left(\frac{l_n}{l_m}\right)\left(\frac{\sqrt{\frac{f}{f_c}}}{1 - e^{-\sqrt{f/f_c}}}\right) \quad (3)$$

where f_c models the frequency at which skin effect begins to dominate in copper for the thickness of the conductor used in the design, t_c is the combined thickness of the copper conductors used in the spiral, and ρ is the resistivity of copper. The skin depth δ at any frequency [25] and the critical frequency f_c are given by

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} \quad (4)$$

$$f_c = \frac{\rho^2}{\pi^2\mu^2 t_c^2}. \quad (5)$$

The above expression indicates that the use of thicker metals in the spiral will reduce the frequency at which skin effects begin to dominate. Improvements in Q factor at higher frequencies reduce with increasing coil thickness.

The capacitance due to the crossover of the return conductor under the coil is denoted by C_{pov}. This is computed as the parallel plate capacitance between the spiral and the return conductor.

$$C_{pov} = \frac{\varepsilon_d w^2}{d_s} \quad (6)$$

where ε_d is the permittivity of the low-K dielectric material, w is the width of the inductor turn, and d_s is the dielectric thickness between the spiral and the return path.

The sidewall inter-turn capacitor has been neglected in the modeling of non-micromachined inductors. The inclusion of this term is important to understand the effects of sidewall oxide removal on the performance of the micromachined inductors. The sidewall term consists of two parts, namely the parallel plate component (C_{p1n}) directly between the conductors and the fringing fields between the two conductors (C_{p2n}). The fringing field between the inductor turns is a function of the ratio of in-
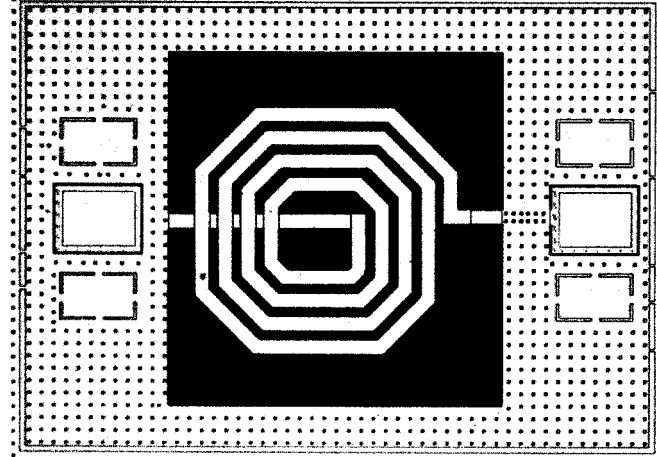

Fig. 4. Microphotograph of a micromachined inductor test structure showing the mask metal layer surrounding the double-side anchored inductor along with two-port test pads. The dimensions of the cavity are 400 μm by 450 μm.

ductor turn width and the gap between the turns and can be expressed as [26]

$$C_{pn} = C_{p1n} + C_{p2n}$$
$$C_{pn} = \frac{(l_{n+1} + l_n)}{2}\left(\frac{\varepsilon_{\text{gap}}t}{P - w} + \frac{\varepsilon_{\text{gap}}}{2\pi}\ln\left(\left(\frac{w}{P - w} + 1\right)^2 - 1\right)\right.$$
$$\left.\cdot\left(1 + 2\left(\frac{P - w}{w}\right)\right)^{(1+(w/(P-w)))}\right) \quad (7)$$

where ε_{gap} is the electrical permittivity of the medium between the turns (air or dielectric), and P is the pitch of the spiral. The fringing capacitance due to the sidewalls can only be neglected for narrow conductors with large spacing between them. The fringe term expression assumes that the conductors are in a medium with the same dielectric constant. The effect of the silicon under the coil has been neglected.

The substrate losses are modeled using the model proposed in [21] and [6]. The capacitance between the inductor and the substrate, C_{ox} is expressed as

$$\frac{1}{C_{ox}} = \frac{1}{C_{oxd}} + \frac{1}{C_{air}} = \frac{2\,d_{\text{sub}}}{\varepsilon_d w l_m} + \frac{2\,d_{\text{etch}}}{\varepsilon_o w l_m} \quad (8)$$

where C_{oxd} is the capacitance between the bottom metal of the spiral and the silicon substrate, that is separated by a distance d_{sub}, C_{air} is the capacitance between the bottom of the oxide to the etched silicon, d_{etch} is the etch depth of the silicon pit. The value of d_{sub} for the inductor in this process is 3.2 μm. The slight asymmetry between the two ports due to the presence of the return conductor has been neglected. The expression has been corrected for fringing using the expression in [27].

The dissipative mechanisms in the inductor include losses in the silicon substrate below the inductor and in the surrounding metal frame. Due to processing constraints, the top metal layer is used as a mask and it defines the etch pit around the inductor. A fill pattern is also introduced by the foundry to control metal density for more uniform thickness during the chemical mechanical polishing of the metal. The empty area in the hollow and around the
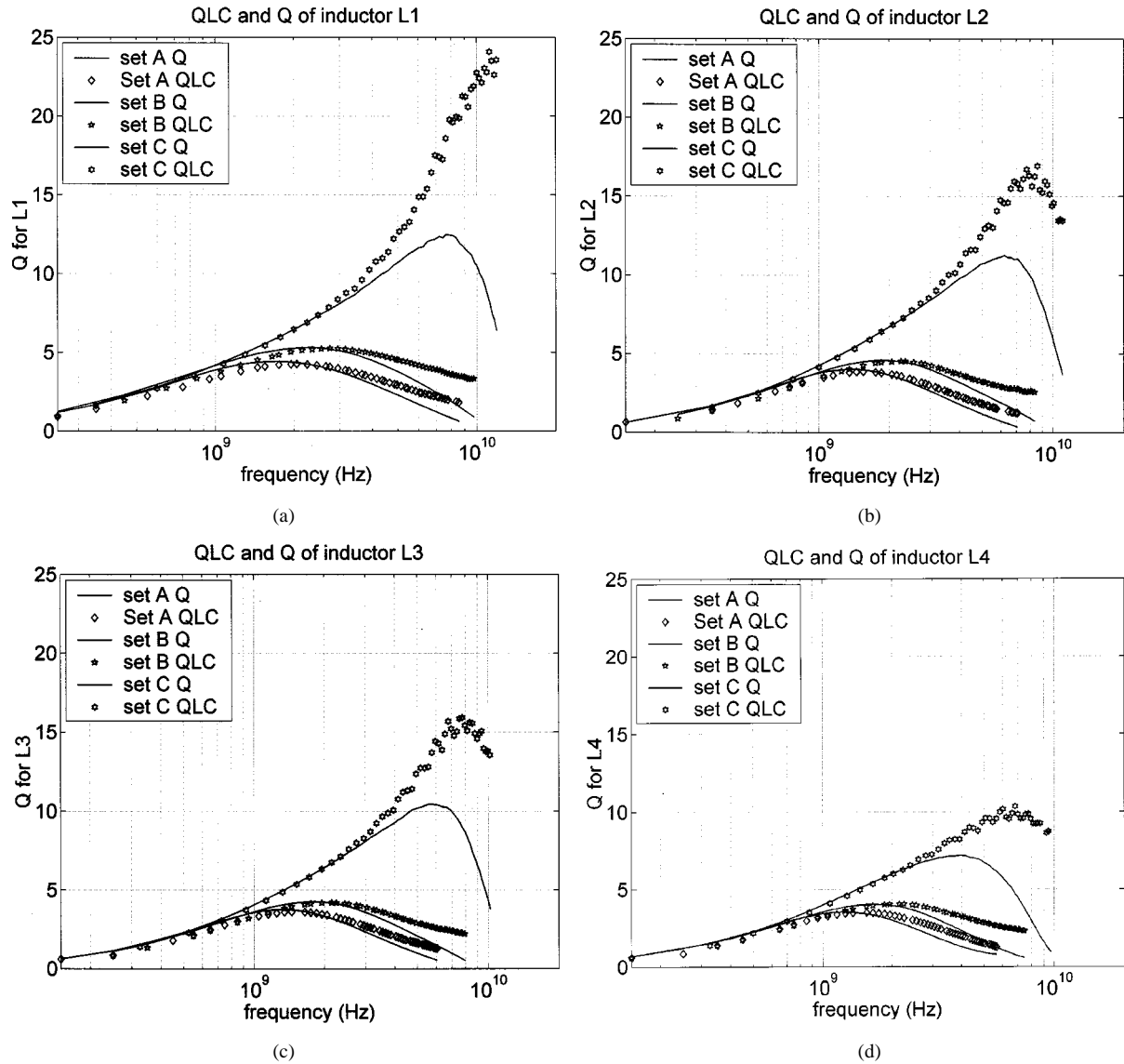
Fig. 5. (a)–(d) Comparison of the measured quality factor of the inductors from Set A (conventional), Set B (oxide removal), and Set C (micromachined) measured by conventional (Q) and LC tank definitions (Q_{LC}) of Q for inductors L1–L4.

inductor and in the lower unused metal layer is an exception to the metal fill rule. The eddy currents produced in the silicon dominate the substrate losses in the non-micromachined inductor case. However, the effects from the surrounding metal frame dominate the losses in the micromachined inductor. A lumped R_s–C_s substrate model accounts for these dissipative mechanisms.

$$C_s = \frac{wl_m}{2} C_{\text{sub}} \qquad (9)$$

$$R_s = \frac{2}{wl_m G_{\text{sub}}} \qquad (10)$$

where C_{sub} is the capacitance and G_{sub} is the conductance per unit area of the substrate. The values of G_{sub} and C_{sub} are extracted from measured results and are function of the inductor geometry. The etch depth of the silicon directly below is a function of the metal mask geometry due to a mass-flow limited etch process. Small openings in the metal mask experience etch lag, d_{etch} is thus a function of the geometry and the layout. Considering these difficulties, d_{etch} is extracted from experimental data.

This model accounts for the changes in inductor performance due to the post process. The effects of oxide removal can be explained by reduction of the C_{pn} term to increase the self-resonant frequency of the inductor. The increase in d_{etch} due to silicon etch lowers the substrate capacitance C_{ox}, thus reducing substrate losses.

B. Definition of Quality Factor

Several definitions of Q have been used to define the quality factor of inductors in the literature [14], [5], [28], depending on their intended applications. The quality factor defined for inductors used in on-chip planar inductor applications and in this paper is defined as

$$Q(f) = \frac{X_m(f)}{R_m(f)}. \qquad (11)$$

For application of the inductor in an LC tank circuit, the quality factor definition at the resonant frequency is important. The Q at resonance of an LC tank (Q_{LC}) is calculated by

TABLE II
SUMMARY OF INDUCTOR MEASUREMENT DATA

Property	L1			L2			L3			L4		
	set A	set B	set C	set A	set B	set C	set A	set B	set C	set A	set B	set C
L_m (nH)	3.16	3.32	3.19	3.89	3.95	3.91	4.12	4.20	4.15	4.61	4.71	4.69
Q_{max} conv.	4.39	5.32	12.5	4.02	4.60	11.2	3.76	4.25	10.46	3.64	4.09	7.61
@ f (GHz)	1.75	2.25	7.75	1.45	1.85	6.50	1.35	1.75	5.72	1.25	1.75	4.75
R_{dc} (ohms)	3.45	3.27	3.32	4.26	4.39	4.16	4.70	4.89	4.65	5.28	5.52	5.21
Q_{max} LC	4.43	5.28	25.7	3.87	4.52	17.0	3.52	4.19	16.0	3.50	4.04	10.3
@ f (GHz)	2.05	2.65	13.7	2.15	2.25	8.62	1.55	2.15	7.65	1.45	2.15	6.80
f_{res} (GHz)	10.1	11.5	14.0	8.35	9.85	12.9	7.15	9.45	12.0	6.65	8.85	11.38
diameter(μm)	300			336			350			365		
width(μm)	20			20			20			20		
turns	4			4			4			4		
pitch (μm)	30			30			30			30		

assuming that the capacitive contribution to the impedance is equal to the inductive contribution and is expressed as

$$Q_{LC} = \frac{f}{2R_m(f)} \frac{d}{df} (X_m(f)) \Big|_{f=f_{res}}$$
$$f_{res} = f|_{X_m=0} \qquad (12)$$

where f is the frequency of the *LC* tank, and $R_m(f)$ is the real part and $X_m(f)$ is the imaginary part of the inductor impedance. This expression is evaluated at the resonant frequency of the *LC* tank, f_{res}, which is defined as the frequency at which the imaginary part of the impedance is zero. This method defines Q at only the resonant frequency. Niknejad *et al.* [28] proposed a Q calculation at any frequency by addition of a perfect capacitor to bring the resonance to that frequency. This definition of Q measurement leads to much higher values for micromachined inductors.

C. Experiment Design and Measurements

Four octagonal inductors with different sizes, L1–4, and values ranging from 3.0 to 4.5 nH were designed. The metal mask around the inductor was 400 μm × 450 μm. Inductor L1 along with the two-port probe pads are shown in Fig. 4. The surrounding mask metal has been grounded and is tied to the substrate. To investigate the effect of the micromachining on the performance of the inductors, measurements were made on unprocessed inductors, after the first step of sidewall oxide removal and after the complete processing. All these chips were from the same wafer batch and were post-processed at the same time. This set of measurement helps to quantify the improvement due to micromachining, including oxide removal and silicon etching.

The inductors were measured by making two-port measurements by on-chip probing using 100-μm pitch ground–signal–ground (GSG) microwave probes connected to an HP8510C network analyzer with frequencies ranging from 50 MHz to 20 GHz. Probe calibration was done using a Cascade CS-5 calibration substrate. The probe pads were de-embedded by making

measurements on dummy open and short test structures connected to test pad structures.

The performance of four inductors L1–4 was compared with measurements made on three chips. The three sets of measurements are as follows.

- Set A: Conventional inductors without micromachining were obtained from the foundry.
- Set B: Low-K sidewall oxide removed in areas not covered metal. [Fig. 1(b)].
- Set C: The inductors were processed as in Set B followed by silicon removal [Fig. 1(c)] in all regions not covered by metal.

A comparison of the Q of the micromachined inductors calculated by the conventional method and by the *LC* tank definition is shown in Fig. 5. Table II summarizes the measurement results obtained from the inductors. All the values of Q were measured by grounding port 2. The change in quality factor after the sidewall oxide removal is not significant, however, an increase of 14%–33% in the self-resonant frequency can be seen. The reduction of the sidewall oxide capacitance is larger for the bigger inductor, causing a greater increase in self-resonant frequency. A small increase in the maximum Q was also observed due to the increase in the self-resonance frequency.

The silicon removal process step increases the maximum Q by about 100%–180%. A smaller increase is observed in L4, the largest inductor, due to the smaller distance of the inductor from the surrounding mask and the fill metal. This suggests that the separation distance from the sidewall to the inductor should be made large enough to minimize eddy current losses in the mask metal. The self-resonance frequency increased by about 38%–70% over set A, depending on the size of the inductor. The larger inductors have a larger increase due to a greater reduction in capacitance to substrate (C_{ox}). The frequency at which maximum Q occurs is moved to the 5–8-GHz range from the 1–2 GHz range in the case of set A inductors, an increase of 280%–350%. Inductor L1 in set C achieves a maximum Q
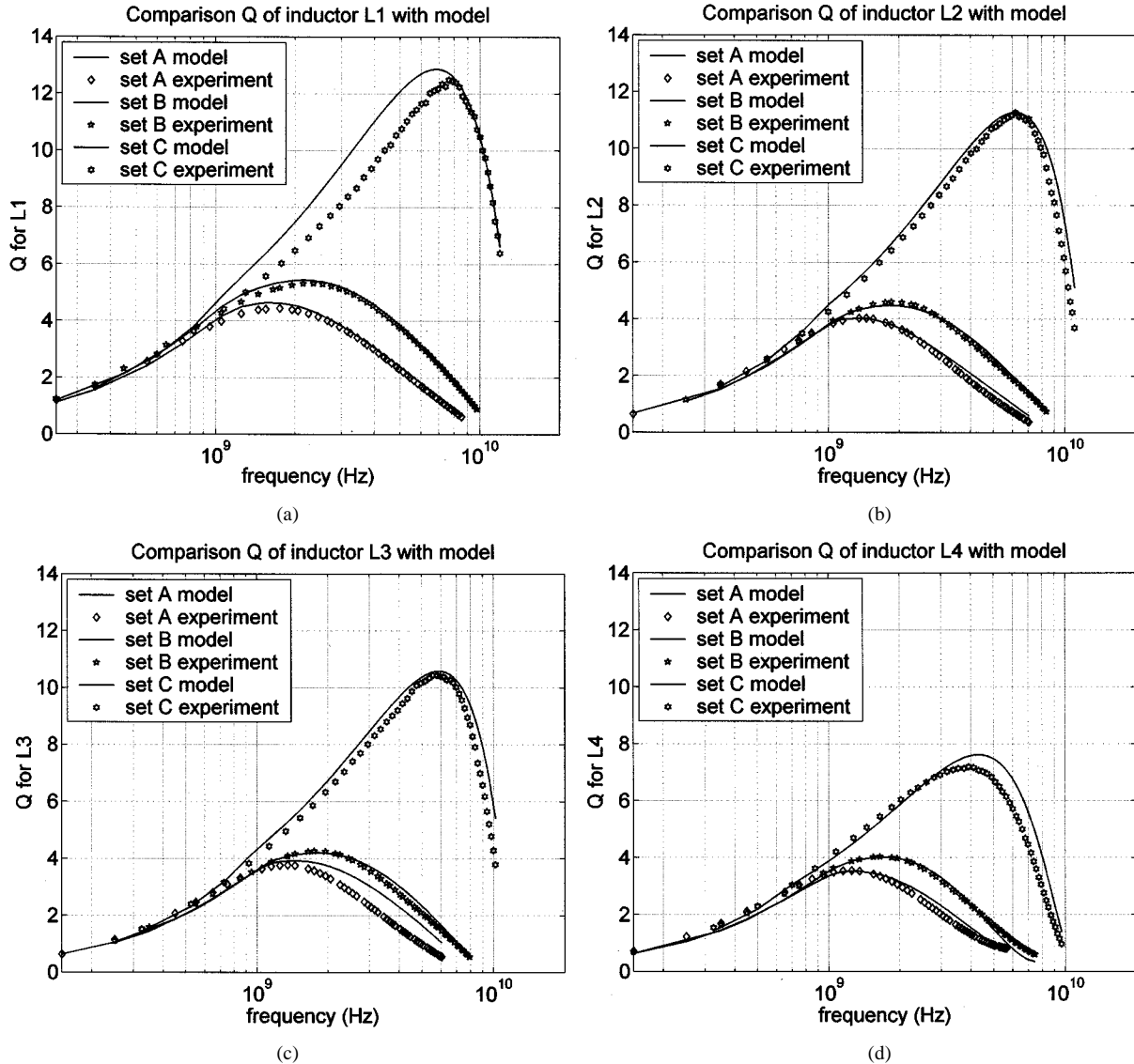
Fig. 6. (a)–(d) Comparison of the measured quality factor of the inductors from Set A (conventional), Set B (oxide removal), and Set C (micromachined) with the model predictions for inductors L1–L4.

of 12.5 at 7.8 GHz, a 14-fold increase compared to set A. At 5.5 GHz, a five-fold improvement can be seen.

The measured quality factors are compared to the model, described previously, in Fig. 6. The differences in set A and set B result from a reduction in the sidewall capacitance and a slight increase in G_{sub} due to the overetching of the silicon during the etching of the oxide. The model for set C is accounted for by the increase in the effective etch depth d_{etch} and the increased substrate conductivity G_{sub}.

IV. DISCUSSION

At lower frequencies, the quality factor of the inductors is not significantly improved by micromachining, as the series resistance losses dominate the energy loss mechanism. However, at higher frequencies, substrate losses begin to dominate and an improvement in Q is observed. The inductor design was made in the standard digital logic process and the total thickness of the inductor metal was 1 μm, and yet quality factors of greater than 10 have been achieved.

Post-CMOS micromachining represents a solution that reduces both the capacitance to substrate and the inter-turn capacitance. The addition of closely spaced copper layers with interleaved low-K dielectric offers a high mutual inductance between the parallel layers [29]. This means that use of multilevel layers with CMOS micromachining will reduce series resistance without significant reduction in inductance, improving overall performance.

Design of high-quality passives for circuits in the 5–6 GHz band [30] is possible with micromachining on a standard CMOS process. The model developed for micromachined inductor can be used to evaluate the improvement in Q factor obtained by increasing the metal thickness. For example, Fig. 7 shows the improvement in Q by increasing metal thickness with and without micromachining for the L1 inductor. Without micromachining, the change is significant at 1 GHz, but at 5.5 GHz no improvement is gained, as substrate losses dominate the Q degradation. However, with the additional micromachining, the Q does improve at both frequencies. The

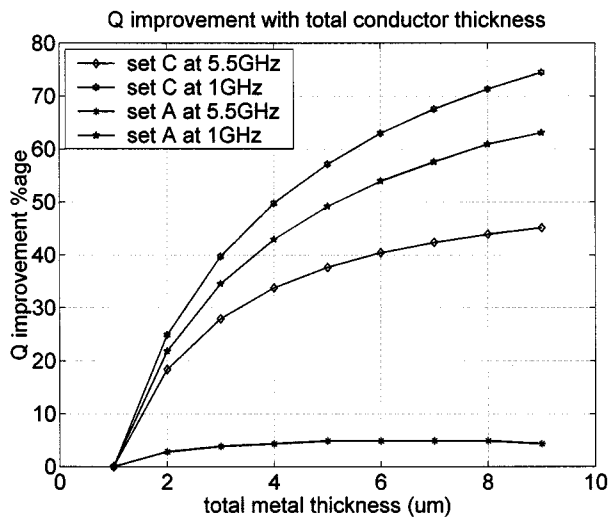## Q improvement with total conductor thickness

Fig. 7. Percentage improvement in *Q* factor with increase in metal thickness at 1 GHz and 5.5 GHz for inductor L1, with and without post-process micromachining.

improvement in *Q* at 5.5 GHz is lower than that at 1 GHz, as the skin depth limits the improvement of *Q* with increasing frequency. The quality factor of the micromachined inductor is predicted to be limited by the dc series resistance for metal thicknesses below 6 μm. Above this thickness, the inductance change with thickness must be included for best accuracy. Qualitatively, for thicker metal layers, the series resistance becomes limited by skin effects, the inter-turn capacitance increases and the self-resonance is lowered. All of these effects conspire to limit the *Q*. From Fig. 7, the thickness limit is estimated at about 10 μm, and conservatively at 6 μm.

Substrate coupling is an important consideration in design of RF analog circuits placed close to digital circuits. Design of deep trenches in the silicon separating the analog block from the digital block is an interesting application of this technology to reduce substrate coupling. This is easily implemented by designing a moat around critical circuit blocks. The removal of substrate also improves the performance of metal–insulator–metal (MIM) capacitors as the parasitic capacitance to substrate is reduced. The use of multiple metal layers shunted together can help reduce the resistance of the MIM structure.

The use of top metal as a mask is not very convenient as this layer cannot be used freely for circuit interconnect. The top metal also introduces increased interconnect parasitics. An extra noncritical masking step to protect the circuits from post-CMOS micromachining can be included to free the top metal for interconnects, however, this step was not feasible to implement on the die-level prototype.

V. Conclusions

Post-CMOS micromachining improves the performance of CMOS inductors, as validated through experimental measurements. A physics-based model based on earlier literature predicts the improvement in performance obtained by micromachining. The *Q* factor of conventional on-chip inductors at higher frequencies is limited by substrate losses and removal of silicon reduces these losses by 100% to 180%. Reduction of the inter-turn capacitance through dielectric removal and of

the capacitance to substrate through silicon undercut increases the self-resonance by 40%–70%. Micromachined inductor *Q* is limited by series resistance up to thicknesses of about 6 μm. Post-CMOS micromachining is an option to leverage the ever-increasing performance of active components with high-quality passives in higher frequency wireless communications.

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