# Post-CMOS Processing for High-Aspect-Ratio Integrated Silicon Microstructures

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***Abstract*—We present a new fabrication sequence for integrated-silicon microstructures designed and manufactured in a conventional complentary metal–oxide–semiconductor (CMOS) process. The sequence employs a post-CMOS deep silicon backside etch, which allows fabrication of high aspect ratio (25:1) and flat (greater than 10 mm radius of curvature) MEMS devices with integrated circuitry. A comb-drive resonator, a cantilever beam array and a $z$-axis accelerometer were fabricated using this process sequence. Electrical isolation of single-crystal silicon was realized by using the undercut of the reactive ion etch (RIE) process. Measured out-of-plane curling across a 120-$\mu$m-wide 25-$\mu$m-thick silicon released plate was 0.15 $\mu$m, which is about ten times smaller than curl of the identical design as a thin-film CMOS microstructure. The $z$-axis DRIE accelerometer structure is 0.4 mm by 0.5 mm in size and has a 25-$\mu$m-thick single-crystal silicon proof mass. The measured noise floor is 1 mG/$\sqrt{\text{Hz}}$, limited by electronic noise. A vertical electrostatic spring "hardening" effect was theoretically predicted and experimentally verified. [687]**

***Index Terms*—Complentary metal–oxide–semiconductor (CMOS) MEMS, deep reactive ion etch (DRIE), electrostatic spring, inertial sensors.**

## I. INTRODUCTION

MICROMACHINED devices fabricated by complentary metal–oxide–semiconductor (CMOS)-compatible fabrication processes are attractive because of the possibility to integrate high-performance on-chip signal conditioning circuits with digital readouts, expected multivendor accessibility and short design cycle times. Currently, most CMOS-compatible micromachining processes are polysilicon or polysilicon-germanium surface micromachining processes that use silicon oxide as the sacrificial material and typically involve a wet etch for releasing micromechanical structures [1], [2]. Even though HF vapor is often used [3], protection of integrated circuits and sticking problems during release are still major concerns [4]. Wiring on a single polysilicon microstructure is constrained to one conductor, limiting the design flexibility for electrostatic actuators and capacitive sensors. Moreover, the relatively large parasitic capacitance in many polysilicon processes degrades performance of capacitive sensor designs. For example, a 50-finger comb drive with 30 $\mu$m overlap in the MUMP's polysilicon process has 27 fF of sensing capacitance. The parasitic capacitance is 13 fF due to the fingers alone, 14 aF/$\mu$m from interconnect and 1.1 pF for a standard 78 $\mu$m by 78 $\mu$m square bond pad [5]. Bond-wire or solder-bump connection to external electronics contributes additional parasitic capacitance.

The process flow described here builds on prior work, in which a post-CMOS surface micromachining process uses composite microstructures made from combinations of aluminum, silicon oxide, and silicon nitride thin films [6]. For that process, the silicon substrate acts as the sacrificial material and is undercut for release (see Fig. 1). The resultant integrated multiconductor microstructures provide wiring flexibility and low parasitic capacitance to interface electronics, when compared to polysilicon microstructures. For example, a 50-finger comb drive with 30 $\mu$m overlap has 89 fF of sensing capacitance, assuming a CMOS microstructure with 5-$\mu$m-high comb fingers and a 1.5-$\mu$m gap. The comb parasitic capacitance is only 1.2 fF because of the large 30-$\mu$m-deep cavity underneath the fingers [7]. Both lateral and vertical CMOS accelerometers [7], [8] with fully differential capacitive interface circuits have been fabricated by using this post-CMOS micromachining process. A triaxial microstage has also been realized [9].

However, all of the microstructures discussed above are made of thin films, either homogeneous or multilayer. The multilayer thin-film structures made from the prior post-CMOS micromachining process usually have large residual stress gradients which cause curling. This limits the maximum layout size of microstructures, which is critical for providing large proof mass in inertial sensors. Moreover, release holes and unwanted curvature of microstructures degrade their application in the optical domain.

Deep RIE (DRIE) technologies have advanced significantly in recent years. By alternating passivation and etching cycles, the Bosch advanced silicon etch (ASE) process [10] can typically achieve high aspect ratios between 20:1 to 30:1. For example, a bulk silicon comb-drive actuator with 100-$\mu$m-deep comb fingers and 15-$\mu$m gap spacing has been fabricated by using the SCREAM process [11]. Microstructures have also been released by through-wafer etching [12], made feasible by the high silicon etch rate of the ASE process ($\sim$3 $\mu$m/min). However, given a typical wafer thickness ($\sim$500 $\mu$m), a minimum gap spacing of 20 $\mu$m would be needed to conform to the

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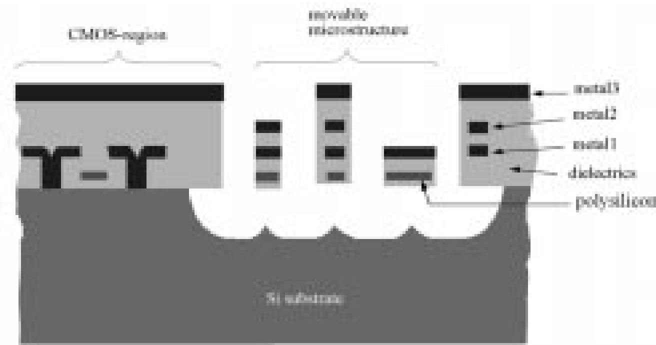


Fig. 1. Cross-sectional view of the thin-film post-CMOS microstructures.

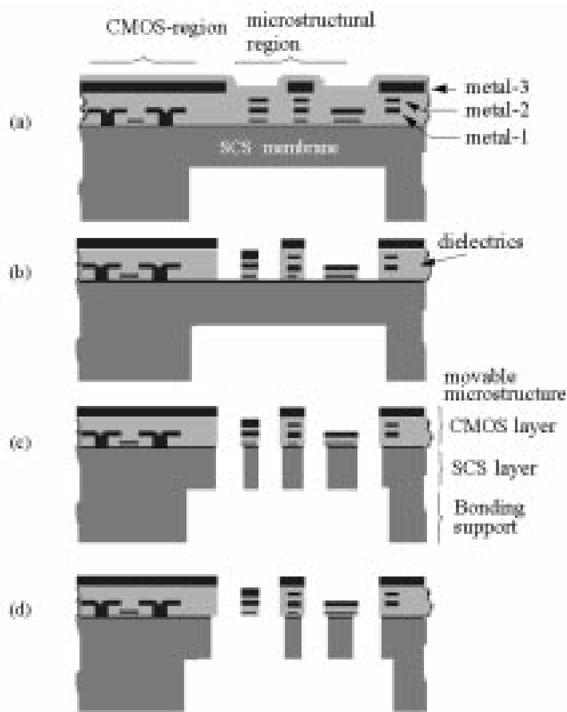


Fig. 2. The process-flow for DRIE CMOS micromachining. (a) CMOS-chip with backside etch. (b) Anisotropic dielectric etch. (c) Anisotropic silicon etch for release. (d) An optional, short isotropic silicon etch for undercut control.

etch aspect ratio. Such a spacing requires large silicon area for either sensing or actuation.

Our solution is to combine the maskless post-CMOS micromachining process [6], ASE and backside etch. The backside etch is used to control the thickness of the final, released, microstructures, which allows optimization of the process for a particular design. The new process sequence (Fig. 2) provides high-aspect-ratio and very flat microstructures. It incorporates all the advantages of CMOS composite microstructures with the excellent mechanical properties of single-crystal silicon (SCS), including fine-gap lateral electrodes micromachined from the CMOS interconnect stack. A timed lateral silicon undercut etch at the end of the process allows a combination of the CMOS thin-film structures along with DRIE SCS structures designed within the same device. In the following sections, the new DRIE post-CMOS micromachining process is described and the characterization results of a few example devices fabricated in the new process are reported.

## II. CMOS Micromachining Processes

### A. CMOS Surface Micromachining Process

The previous post-CMOS micromachining process [6] consists of an anisotropic dielectric etch for defining the microstructures and an isotropic silicon etch for release. Fig.1 shows the cross-sectional view after the process is completed. As the etching masks are interconnect metals from preceding CMOS processing, no post-CMOS photolithography is required. An aspect ratio as high as 4:1 can be achieved, limited by metal mask erosion. The microstructures consist of the metal interconnect layers that are electrically isolated by dielectrics, which enables a variety of wiring configurations [7]–[9]. An issue with this CMOS-MEMS process is the residual stress and thermal coefficient mismatch in the embedded layers of a composite beam that cause curling or bending [14]. Vertical curling can be compensated to first order through a curl matching frame, at the price of significantly increased design complexity [7].

### B. CMOS Backside Micromachining Process

In order to overcome some of the drawbacks of thin-film microstructures without losing the advantages of the multiconductor structures, we propose a new process sequence building on the previous post-CMOS micromachining process. The basic idea is to introduce a single-crystal silicon (SCS) layer underneath the CMOS multilayer structures in such a way that the mechanical properties are dominated by the SCS layer and electrical connections are provided by the CMOS microstructure layer [15].

A diagram of the process flow is shown in Fig. 2. We start with a deep anisotropic backside etch leaving a 10-$\mu$m to 100-$\mu$m-thick SCS membrane [see Fig. 2(a)]. This backside etch step is used to control the thickness of microstructures. The cavity formed by the backside etch allows the completed die to be bonded directly to a package without interference from the released microstructures. Next, an anisotropic dielectric etch is performed from the front side [see Fig. 2(b)]. Then, in contrast to the prior work on post-CMOS processing, an anisotropic instead of an isotropic silicon etch is used for

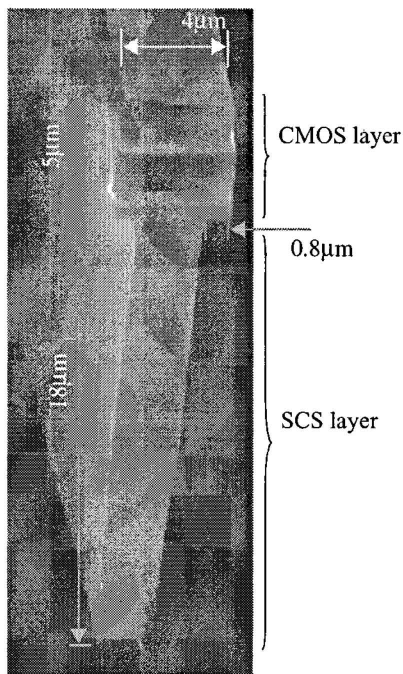


Fig. 3. SEM side view of a beam end: The optional isotropic etch [see Fig. 2(d)] was used to attain the large undercut.

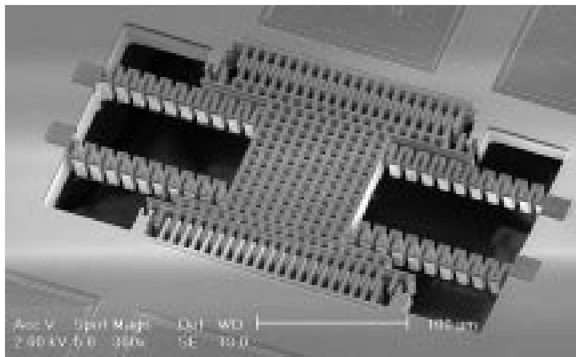

Fig. 4. SEM of a comb-drive resonator fabricated in the DRIE CMOS process.

release [see Fig. 2(c)]. A thick, stiff, SCS layer remains underneath the CMOS layer, resulting in a relatively flat released microstructure, especially when compared with multilayer thin-film CMOS-MEMS structures. As a final step, an optional timed isotropic Si etch may be performed [see Fig. 2(d)]. This step provides a specific undercut of bulk Si to create compliant structures to achieve electrical isolation of single-crystal silicon.

A scanning electron micrograph (SEM) of a beam fabricated by this process is shown in Fig. 3. The silicon beam end is tapered, appearing tilted as an artifact of the viewing angle in the SEM. The 0.8-$\mu$m undercut resulted from the isotropic silicon etch step. No curling compensation is needed and a microstructure can be designed to an arbitrary shape and orientation in the $x$-$y$ plane. Furthermore, the proof mass and comb-finger capacitance for CMOS-MEMS based inertial sensors is significantly increased. The SEM of a comb-drive resonator fabricated by using the new process is shown in Fig. 4. In a later section, we will discuss the electromechanical characterization of this device in detail.

### C. Design Considerations

Since there are no fixed electrodes underneath the microstructures, this technology is mainly suitable for sidewall capacitive sensing and actuation. Suppose there are two side-by-side beams, e.g., a pair of comb fingers, as shown in Fig. 5(a). A comb drive can be constructed from an array of these comb fingers, as shown in Fig. 5(b). The sidewall capacitance change versus displacement in the longitudinal, transverse and vertical directions have the following relationships:

$$\frac{\partial C}{\partial x} \propto \frac{h}{g} \cdot \frac{L-g}{g+w} \quad \frac{\partial C}{\partial y} \propto \frac{h}{g} \cdot \frac{l}{g} \cdot \frac{L-g}{g+w}$$
$$\frac{\partial C}{\partial z} \propto \frac{l}{g} \cdot \frac{L-g}{g+w} \tag{1}$$

where $l, g, h$ and $w$ are the engaged length, gap, height and width of the comb fingers, respectively, and $L$ is the total length of the comb-finger array. The total number of gaps between stator and rotor comb fingers is $((L-g)/(g+w))$. The gap aspect-ratio is $h/g$, which is fixed for the ASE process. If a fixed area is assumed, i.e., $L$ is fixed, then the smaller the gap, the larger the capacitance change in all three directions. The height of the comb fingers is then best set by the minimum possible gap. Thicker comb fingers would require a larger gap and result in a reduction in capacitive sensitivity. However, there is a minimum SCS layer thickness that eliminates the stress-induced curling below values of surface roughness. Note that this minimum thickness value depends on the size of the designed microstructure as well as the thickness control accuracy of the deep Si RIE process. For inertial sensors, mass is a critical parameter that dictates resolution. The SCS layer should be as thick as possible and there is a tradeoff between the gap spacing and the structural thickness.

An electrically isolated SCS block is shown in Fig. 6, where the beam width is 1.5 $\mu$m and the CMOS bridge provides mechanical support as well as electrical wiring. The SCS layer underneath beams smaller than two times the deep Si RIE undercut of 0.4 $\mu$m are undercut. However, an additional isotropic silicon etch must be performed to undercut wider beams, as illustrated in Fig. 2(d). Through complete undercut of the silicon on supporting thin-film beams, released areas of bulk silicon can be electrically isolated. In addition, soft springs can be obtained by using the same principle. To further guarantee the electrical isolation, the to-be-undercut silicon region is implanted as $n$-well (for $p$-silicon substrate) to form a $p$-$n$-$p$ junction in case there is still a remaining thin layer of silicon underneath the beam, as shown in Fig. 7.

### D. Fabrication

Single-chip processing was used to demonstrate the DRIE release sequence. The square CMOS chips (2 mm by 2 mm) are made in the Hewlett Packard 0.5-$\mu$m three-metal $n$-well process available through MOSIS.

The chips come with an unpolished backside. Prior to the deep etching process the backside was patterned in a

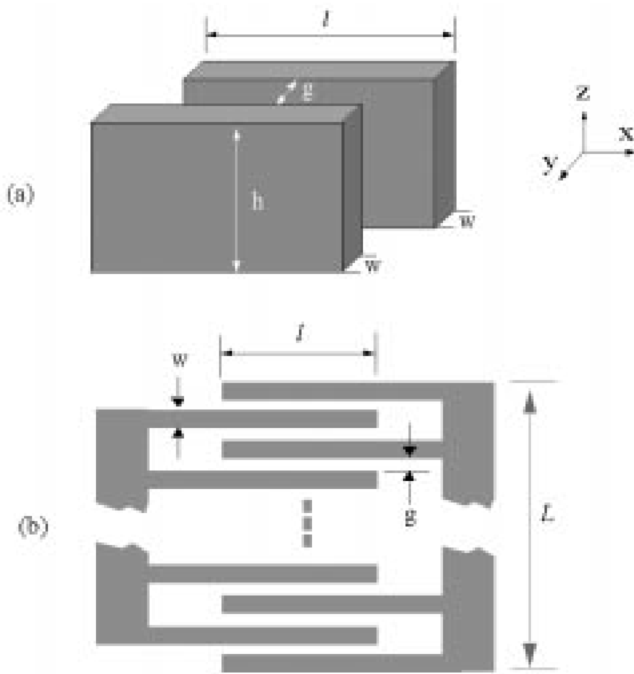


Fig. 5. Schematic of a comb drive. (a) Side view of a pair of comb fingers. (b) Top view of the comb-finger array.

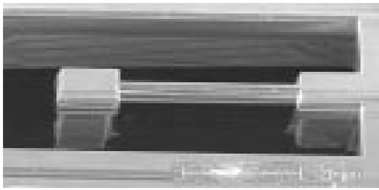

Fig. 6. SEM of an electrically isolated SCS block.

photolithography step with a backside release mask using a 10-$\mu$m layer of a high viscosity photoresist (Shipley AZ 4620). The exposure was performed with a Karl-Suss MA 56 mask aligner. The backside-frontside alignment accuracy needs to only be around 50 $\mu$m to allow for the full wafer thickness of silicon under the bond pads on the periphery of the chip. The patterning guaranteed that a sufficient silicon frame for mechanical support of the silicon membrane remains after the deep etch. The chips were mounted on a 4″ silicon wafer covered with photoresist. The backside ASE etch for defining the silicon membrane was performed in a Surface Technology Systems (STS) ICP (inductively coupled plasma) etcher. The etching-process employed was a typical ASE process [10] with an etching rate of 2.9 $\mu$m/min for a small silicon load. The main plasma parameters for the etching part of the cycle were 600 W coil power, 12 W platen power, 130 sccm $SF_6$ flow, and 23 mT chamber pressure. The fluorocarbon polymer passivation cycle was performed at 600 W coil power, 12 mT chamber pressure, 85 sccm flow of $C_4F_8$ and no platen power. The duration was 12 s in the etching cycle and 8 s in the passivation cycle. After removal of the chips from the carrier wafer and an oxygen plasma clean of the chip frontside, the oxide RIE etch of the CMOS-micromachining process [see Fig. 2(b)] was performed in a Plasma-Therm 790 reactor.

The major demands for the Si etching process are good stability of the etching rate, low surface roughness and a sufficiently uniform structural thickness. A polishing of the chip backside prior to the backside deep etch improves the smoothness of the resulting silicon membrane surface but is not necessary. The backside etch step defines the thickness of the remaining silicon membrane and high accuracy measurements of the thickness of the chips and the etch depth are necessary. The typical backside etch step of around 450 $\mu$m is beyond the measurable range of the profilometer in our lab. We employed an optical microscope to perform these measurements. By using a 50× microscope objective, accuracies of $\pm 3$ $\mu$m can be achieved.

For performing the anisotropic silicon release step [see Fig. 2(c)] in the STS ICP etcher, the chips were mounted on a 4″ photoresist-covered silicon wafer. The top metal of the CMOS layers served as the mask. We observed no degradation of the top metal layer even for etching durations of several hours. We could not detect any performance decrease of the ICP etcher due to use of the Al mask. Only die-sized samples were processed, which limited the amount of aluminum exposed in the chamber. The final optional silicon etch step [see Fig. 2(d)] is also performed in the STS etch chamber. The isotropic etch is achieved by turning off the platen RF power and leaving on only the coil power.

Due to well-known microloading effects of the ASE process [16], the trenches with a larger width are etched faster. Therefore, the large open areas are etched through to the backside first, before the narrow gaps. The exposure to plasma through the openings results in polymer deposition on the remaining silicon backside during the passivation steps of the ASE.

A close-up of the backside of a comb-drive actuator after performing the anisotropic etch step is shown in Fig. 8(a). The polymer deposited on the backside of the SCS layer due to the relatively early etch-through of the wider gaps forms a residual structural layer that cannot be etched by continuing the ASE process. The polymer layer is removed by using a zero-bias oxygen plasma clean at the end of the process flow after the narrow gaps are etched through to the polymer film. The SEM in Fig. 8(b) shows the backside of a clean device after an oxygen plasma step is used at the end of the release procedure. The 1.2-$\mu$m gaps are released. The bottom surface is rough due to the 450-$\mu$m-deep Si etch that is performed on the unpolished backside of the die. The ASE undercut is smaller in corners of structures, therefore the square release holes appear as round holes on the backside.

## III. Characterization

### *A. Cantilever Beams*

In order to investigate the mechanical properties of the composite microstructures with stacked CMOS and SCS layers, an array of 110-$\mu$m-long and 3-$\mu$m-wide cantilever beams was designed. Fig. 9 shows two of the released beams. The minimum gap is 2.1 $\mu$m, which limits beam thickness to a maximum of 55 $\mu$m for an aspect-ratio of 25. The fabricated beam thickness is 45 $\mu$m. The undercut of a beam or any other structure strongly depends on its separation to the surrounding struc-

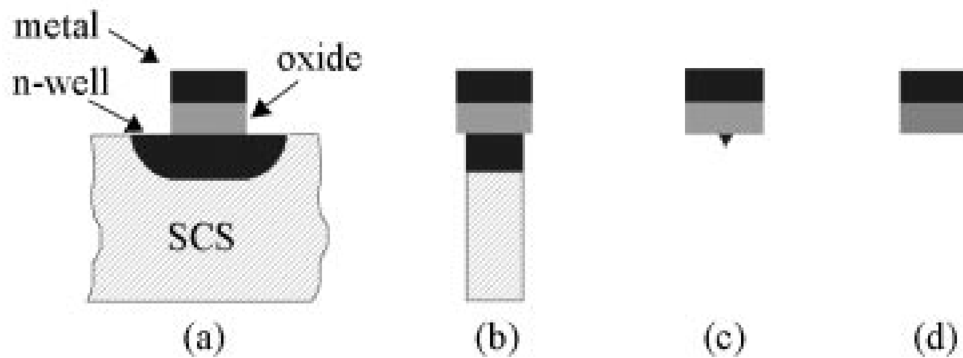


Fig. 7. Electrical isolation of silicon. (a)Metal–oxide beam after the dielectric micromachining process step with a $n$-well underneath. (b) Deep Si etch with a small undercut. (c) Isotropic Si etch with left-over silicon. (d) Isotropic Si etch for completely undercutting.

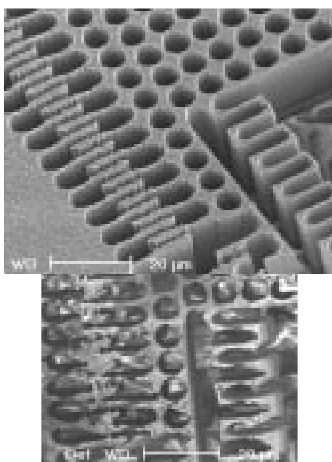

Fig. 8. SEMs of the backside of the comb-drive actuator. (a) After the ASE, prior to oxygen plasma cleaning. (b) After oxygen plasma cleaning.

Fig. 9. SEM of DRIE CMOS cantilever beam resonators.

tures. Larger gaps will generate larger undercut. In the figure, the typical scallops of the ASE process are present along with an undercut of about 0.4 $\mu$m at the edges adjacent to large etch pits. The measured resonant frequency is 254 kHz, which is in good agreement with the finite element simulation of 249 kHz. The Young's modulus of the SCS layer in the lateral direction aligned to the Si wafer flat (i.e., $\langle 110 \rangle$) is 168 GPa [17] and the CMOS layer has an effective Young's modulus of 63 GPa [14].

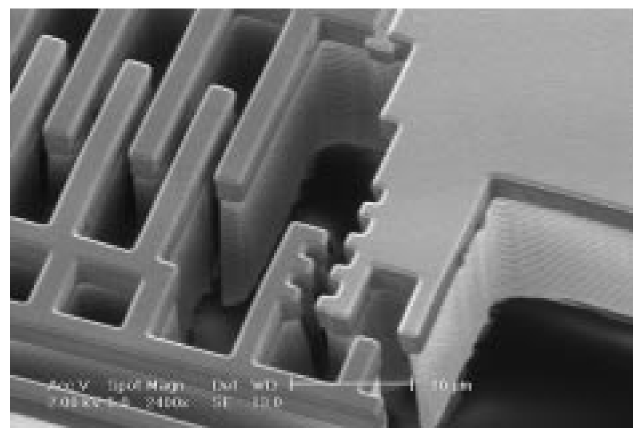

Fig. 10. Close-up of one corner of the comb-drive actuator (see Fig. 4).

### *B. Comb-Drive Resonator*

Fig. 10 is a close-up of one corner of the comb-drive resonator shown in Fig. 4. The gap of the comb fingers is 1.2 $\mu$m and thus the underlying SCS layer has been thinned down to a 30-$\mu$m thickness for an aspect-ratio of 25. The underlying SCS beam width is 0.8 $\mu$m narrower than the CMOS layers due to the 0.4-$\mu$m Si undercut. The underlying SCS is not electrically isolated from the silicon substrate in this comb-drive actuator. For comparison, another comb-drive resonator having the same layout was released by using the thin-film micromachining process. Experimental measurement of displacement amplitude at resonance shows that the stiffness of the serpentine-spring suspension is increased by a factor of four (12% error) by including the underlying thick SCS layer.

To evaluate the topography of the released structures, we employed a Linnik-type Michelson interferometer with LED illumination ($\lambda = 610$ nm). The topography is calculated from a series of fringe patterns using a phase unwrapping technique [19]. We achieved a measurement accuracy of better than 40 nm for the $z$-curling. The measured topography of a comb-drive actuator with no underlying SCS layer is shown in Fig. 11(a). The peak-to-valley curling measured across the 120-$\mu$m-wide device is 1.2 $\mu$m. For a device with underlying 20-$\mu$m-thick SCS, the curling is 0.15 $\mu$m, nearly an order of magnitude reduction, as shown in Fig. 11(b). The corresponding radius of curvature for the SCS CMOS-MEMS structure is 12 mm.

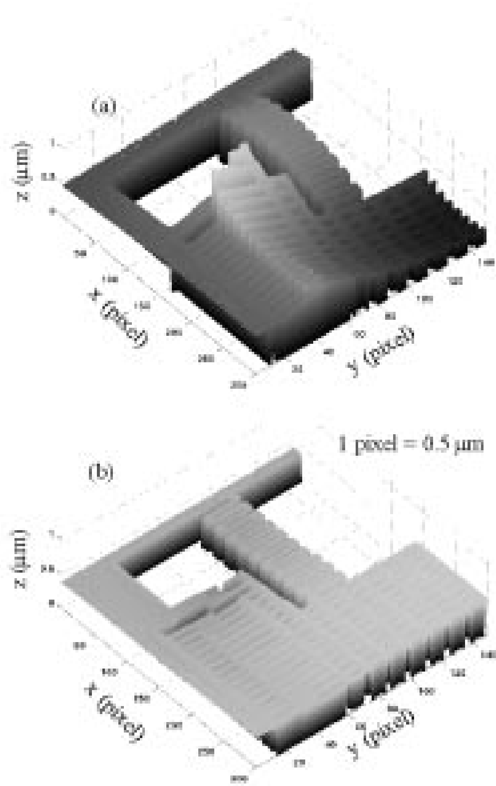


Fig. 11. The topography of the released comb-drive actuator (see Fig. 4) (only one quarter is shown) obtained by using phase shifting interferometry. (a) Conventional release. (b) Backside release.

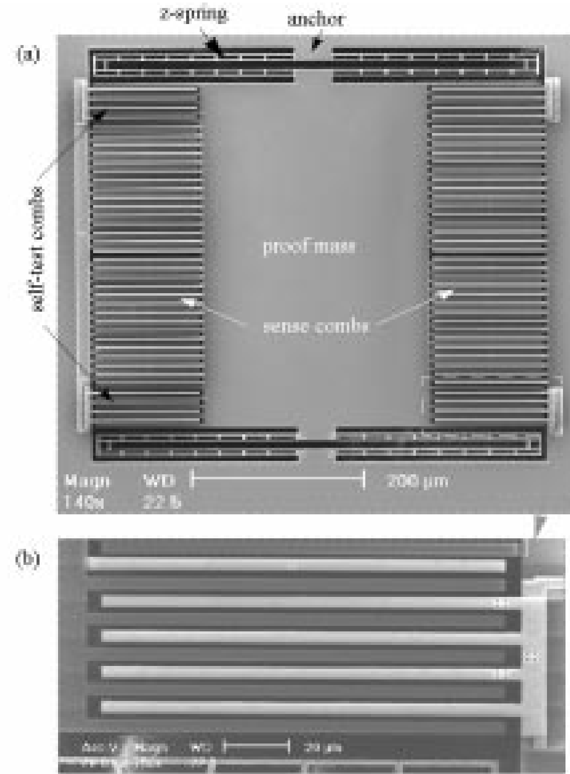


Fig. 12. SEM of a DRIE $z$-axis accelerometer. (a) Full view. (b) Close-up of self-test comb fingers.

### C. DRIE $z$-Axis Accelerometer

The SEM is shown in Fig. 12 of a released $z$-axis accelerometer consisting of $z$-compliant springs, a proof mass, comb fingers for $z$-axis motion sensing, and $z$-axis self-test comb-drive actuators. The principle of the $z$-axis motion sensing and actuation is described previously for the thin-film CMOS devices in [8] and [9] respectively. The $z$-compliant springs constitute only the CMOS interconnect layers where the underlying silicon is removed away by the undercut of the DRIE etching.

A Brüel and Kjær shaker table and an HP4395A spectrum analyzer were used to characterize the micromechanical frequency response. The motional response measured at the output of the on-chip preamplifier is shown in Fig. 13(a). Vibration was excited by applying a 1-V peak-to-peak ac voltage to the integrated self-test $z$-axis actuators. The $z$-axis out-of-plane vibration mode, which is the primary mode, has a resonant frequency of 4.1 kHz and a mechanical quality-factor of 21. The quality factor is close to one order of magnitude higher than that observed from the thin-film $z$-axis accelerometers [8]. This is because the DRIE $z$-axis accelerometer has a larger mass, and has no substrate under the microstructure and therefore has no appreciable squeeze-film air damping. The out-of-plane torsional mode has a resonance frequency of 7.8 kHz. In order to verify the electrical measurement, the $z$-displacement of the proof mass was also measured optically by using an MIT microvision system [18]. The result is shown in Fig. 13(b) where a 1 V peak-to-peak ac voltage was applied. The $z$-axis and torsional modes have optically measured resonance frequencies of 3.9 kHz and 7.4 kHz, respectively. The design of the $z$-compliant spring sets the resonance frequency of the $y$-mode at three times the $z$-mode (12.3 kHz). In-plane modes were not observed by using the $z$-axis self-test actuator for excitation frequencies up to 10 kHz.

Both $z$-axis and torsional modes in the optical measurement have slightly lower resonance frequencies than those in the electrical measurement. This is caused by the electrical stiffness "hardening" effect of the $z$-axis comb drive. The cross-section of a pair of the $z$-axis comb-drive fingers is shown in Fig. 14(a). Three interconnect layers in the rotor finger are electrically connected together, as are the three layers in the stator finger. The interconnect layers in the rotor are also electrically connected to the silicon substrate. Thus, a sidewall capacitor $C$ is formed. If a voltage $V$ is applied, a vertical force equal to $1/2(dC/dz)V^2$ will be generated. Values of $C$ and $(dC/dz)$ as a function of $z$ are extracted from finite-element analysis [20] and are given in Fig. 14(b) and (c). Near $z = 0$

$$\frac{dC}{dz} = 7.48 \times 10^{-9} - 4.05 \times 10^{-3} z. \qquad (2)$$

This value was calculated for 18 drive comb fingers, which is half of the total on the accelerometer. The spring stiffening force is included in the mechanical system response, i.e.,

$$m\ddot{z} + b\dot{z} + (k + 4.05 \times 10^{-3} V^2) z = 7.48 \times 10^{-9} V^2 \qquad (3)$$

where $m$ is the mass, $b$ is the damping, and $k$ is the mechanical spring constant of the system. Therefore, the resonant frequency

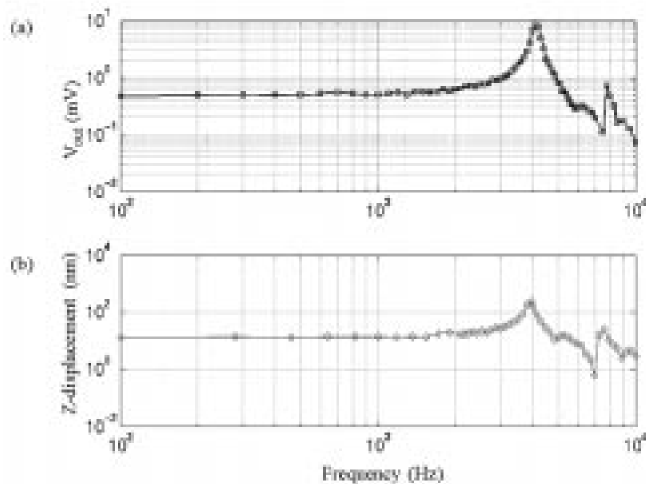


Fig. 13. Frequency response of the DRIE $z$-axis accelerometer. (a) Frequency response measured at the output of the on-chip circuit. The vibration is excited by using the integrated self-test actuators. (b) Frequency response of the $z$-displacement, measured by using an MIT microvision system [18].

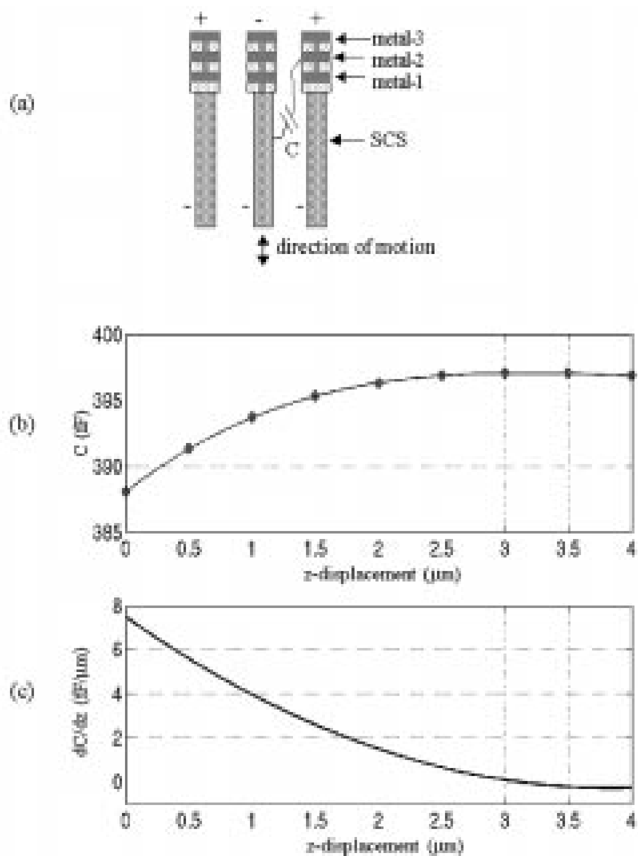


Fig. 14. Simulation of the sidewall capacitance of the $z$-axis comb-drive actuator. (a) Cross-section of comb fingers. (b) Capacitance versus $z$-displacement (c) Capacitance gradient versus $z$-displacement. Number of drive comb-fingers $= 16$; length of drive comb fingers $= 120$ $\mu$m.

of the system is equal to

$$\omega_r = \sqrt{\frac{k_{\text{eff}}}{m}} \cong \sqrt{\frac{k}{m}} \left(1 + \frac{2.03 \times 10^{-3}}{k} V^2\right) = \omega_{r0} \left(1 + \frac{2.03 \times 10^{-3}}{k} V^2\right) \quad (4)$$

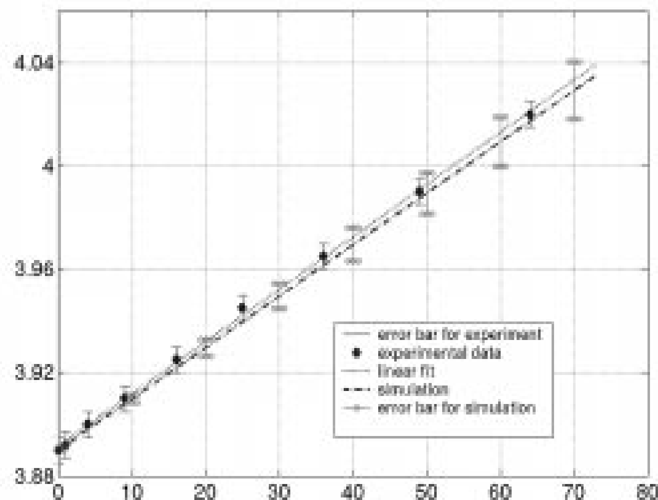


Fig. 15. Vertical electrostatic spring "hardening" effect.

where $\omega_{r0}$ is the purely mechanical resonant frequency of the system. The calculated and measured relationships between the resonant frequency and the dc bias voltage squared are shown in Fig. 15. The resonant frequency changes linearly with $V^2$, as predicted. The spring constant in (4) is calculated as $k = m\omega_{r0}^2$. The slight difference between the calculated and measured curves is attributed to measurement uncertainty in the volume of the silicon proof mass.

The spectrum of the output signal is shown in Fig. 16 with a 0.5-G, 100-Hz external acceleration. The noise floor is 1 mG/$\sqrt{\text{Hz}}$. Even though this noise floor is about five times lower than that measured in the thin-film $z$-axis accelerometers [8], it is still one-order of magnitude higher than the limit of the thermomechanical noise. The noise floor of the accelerometer will be greatly reduced after proper on-chip circuit design is achieved. No deterioration of the on-chip circuitry after the ASE etch was observed. Previous measurements of transistor threshold voltages in the related thin-film CMOS micromachining process showed no shift from the post-CMOS process

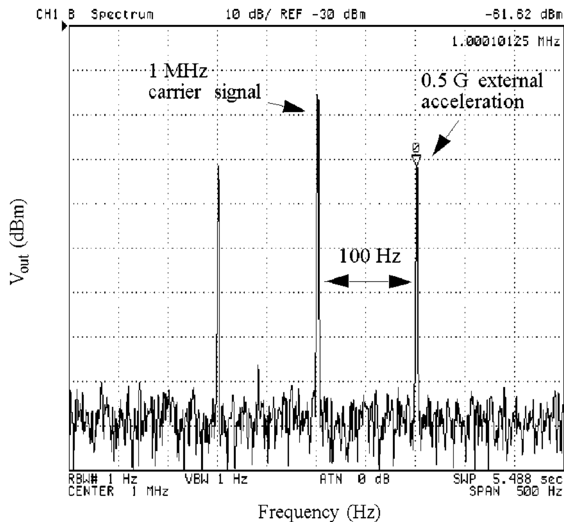


Fig. 16. Spectrum of the output signal of the DRIE $z$-axis accelerometer with a 100 Hz 0.5 G input.

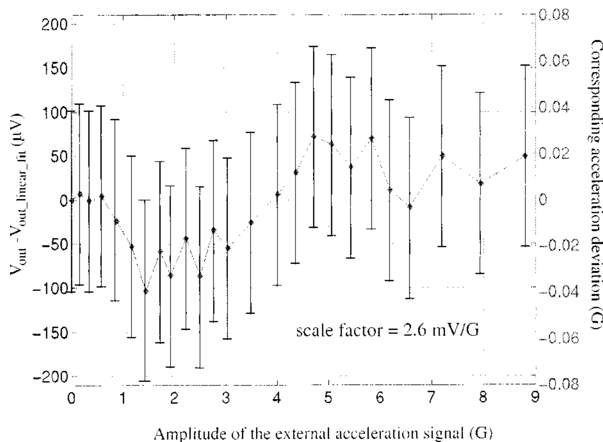


Fig. 17. Dynamic response of the DRIE $z$-axis accelerometer to 100 Hz sinusoidal excitation. Error bars indicate the measurement uncertainty.

steps [21]. Fig.17 shows the nonlinear deviation of the dynamic response curve, measured with an 100 Hz sinusoidal acceleration signal excited by a shaker table. The device has a sensitivity of 2.6 mV/G and a linear response range of at least ±8.8 G. Its linearity is within 0.5% of measured full scale (8.8 G).

## IV. Conclusion

The new DRIE post-CMOS micromachining process has been demonstrated by a beam resonator, a comb-drive actuator and a $z$-axis accelerometer. This process is CMOS compatible and can generate very flat and thick single-crystal silicon microstructures with tight gap spacing. The unique electrical isolation of the silicon and multiconductor features provide high expectations for capacitive sensing and actuation. The resultant large mass and increased comb-finger capacitance should result in high resolution and high sensitivity for inertial sensors as well as larger force microactuators. The out-of-plane actuation combined with the flat surface of resultant microstructures has broad applications in micro-optics such as scanning mirrors, all-optical switches and interferometric systems.

The microloading effect, which can be used to realize electrical isolation of silicon and soft springs, is crucial in this process and should be further characterized. The silicon membrane thickness control is another important issue which warrants further investigation.

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