MEMS DESIGN AND VERIFICATION

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Abstract

The long term impact of MEMS technology will be in its ability to integrate novel sensing and actuation functionality on traditional computing and communication devices enabling the ubiquitous digital computer to *interact* with the world around it. The design and verification of such integrated systems will occur at the system level, driven primarily by the application. Application-driven system-level design methodologies that ease the integration of the digital domain to the real world using mixed domain technologies are therefore needed. A hierarchical structured approach that is compatible with standard IC design is outlined. It starts with schematic capture of a design topology, followed by behavioral simulation, layout generation, parasitic extraction, and final verification.

Keywords: MEMS CAD, MEMS design methodology, modular design, composable design, integrated MEMS design.

1. Introduction

Monolithic integration of MEMS with standard CMOS processes is being driven by the ever-present need to lower cost and increase device sensitivity and reliability. Integration of digital control and digital interfaces increases actuator or sensor value, while the exploitation of the process integration and automation common in CMOS fabrication increases device yield. These combined benefits are underscored by the fact that recent high-volume product introductions have tended to be integrated such as: airbag accelerometers [1], digital light processors [2] and pressure sensors [3] (see Figure 1). In addition to increasing device integration, process integration of CMOS to a variety of MEMS processes including deep reactive-ion-etching of silicon (Si DRIE) [4], dissolved-wafer [5], polysilicon [6] and thick epi-polysilicon [7] technologies is under way.

Low-cost MEMS designs are targeted for high-volume applications such as the automotive accelerometers, gyroscopes and pressure sensors, or consumer ink-jet print heads. Smaller markets for MEMS sensors and actuators that need custom design are ignored due to the high non-recoverable cost of design. Today, custom MEMS design involves designers that need to be experts in MEMS processing, MEMS device design, system integration, as well as the final application domain. As in-depth expertise in each of these regions and breath across these domains is extremely difficult to acquire, few custom designs are attempted. Therefore MEMS continues to be dominated by high-volume markets.

Reducing these development costs requires an integrated MEMS design methodology that formalizes the communication between the process, device, system and application domains, and exploits the expertise in each domain. Such a methodology is required both because of the complexity of integrating MEMS design with CMOS design, as well as to enable the embedded systems design experts to include MEMS sensors if so desired. Once available, it will enable the successful design of *Application Specific Integrated Microsystems* (ASIMs) and advance the commercialization of MEMS in the various application areas where MEMS sensors are ideally suited.
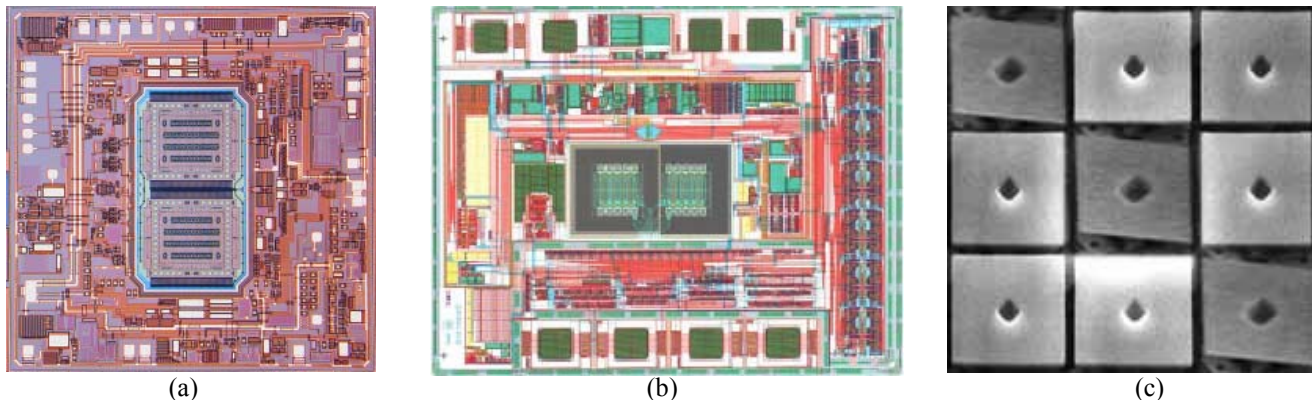

| (a) | (b) | (c) |

Figure 1: Integrated MEMS products (a) Analog Devices gyroscope (b) Motorola integrated tire pressure monitoring sensor and (c) Texas Instruments' digital mirror device.
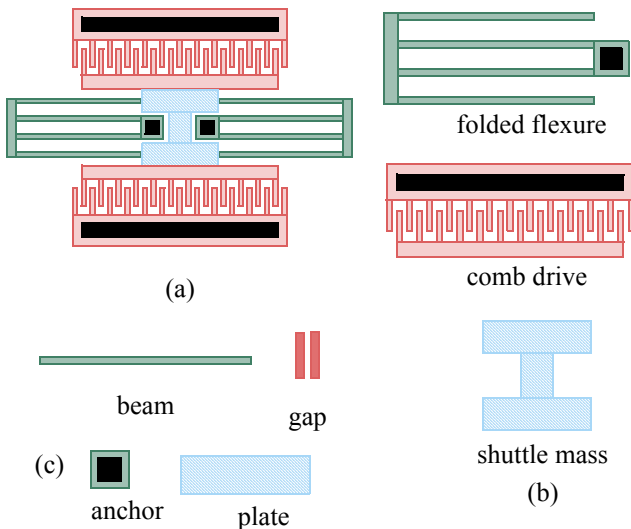
Figure 2: Decomposition of a folded-flexure resonator: (a) component-level folded-flexure resonator; (b) functional elements include comb drive and folded flexure; and (c) atomic elements include plates, beams, gaps and anchors.

To meet the needs of rapid design of low-volume custom MEMS, an integrated MEMS design methodology must: support a wide class of MEMS designs; be extensible to handling new MEMS design concepts; support a wide variety of MEMS fabrication techniques; fit into existing VLSI design flows; and, have the capability to evaluate integrated system designs. A modular approach to MEMS design which addresses these requirements is being developed at Carnegie Mellon [8][9] and elsewhere [10][11][12][13][14]. The approach described in this paper is based on a library of elements that enables modular design composition, similar to VLSI.

The modular design methodology focuses on suspended micromechanical systems. The class of suspended MEMS devices (including accelerometers, gyroscopes, and pressure sensors for automotive markets; micropositioners for data storage; resonators, RF filters, variable capacitors for communication systems; micromirrors for optical data processing systems; and acoustic and ultrasonic transducers) has significant application variety and complexity to motivate this focus. The decomposition of electrostatically-actuated suspended MEMS designs into perforated plates, beam springs of various topologies (*e.g.*, folded-flexure, crab-leg flexure), electrostatic air-gaps and anchors, is exemplified in Figure 2. The composition of complex topologies by interconnecting simple elements and the use of parameterized behavioral models for simulation are analogous and compatible with VLSI design. This enables the leveraging of design environments already in common use in VLSI design, and simulation of cross-domain effects arising from integration, leading to seamless insertion of MEMS into an application-specific design flow.

This modular methodology depends on a variety of abstractions and representations. Section 2 considers the design and process abstractions. Section 3 shows how behavioral simulation is used for design evaluation and iterative design improvement. Section 4 details the layout generation and verification approaches at the back end of the design flow. Finally, we consider the future of integrated MEMS design in the conclusions in Section 5.

2. Design and Process Abstractions

Design of complex integrated MEMS, like any other engineering design problem relies on two fundamental principles, *divide and conquer* to simplify the design problem, and *iteration* to optimize the design. Applying these principles to MEMS requires consideration of the relevant representations for MEMS.

2.1 Design Representations

The physical representations linking process sequences, material properties, mask layout into a 3D structural view for continuum prediction of behavior was formalized over 15 years ago [15]. The mask layout (or physical layout for device fabrication) and 3D structural views (with a mesh for continuum simulation) are the first two of the primary design representations in MEMS, as
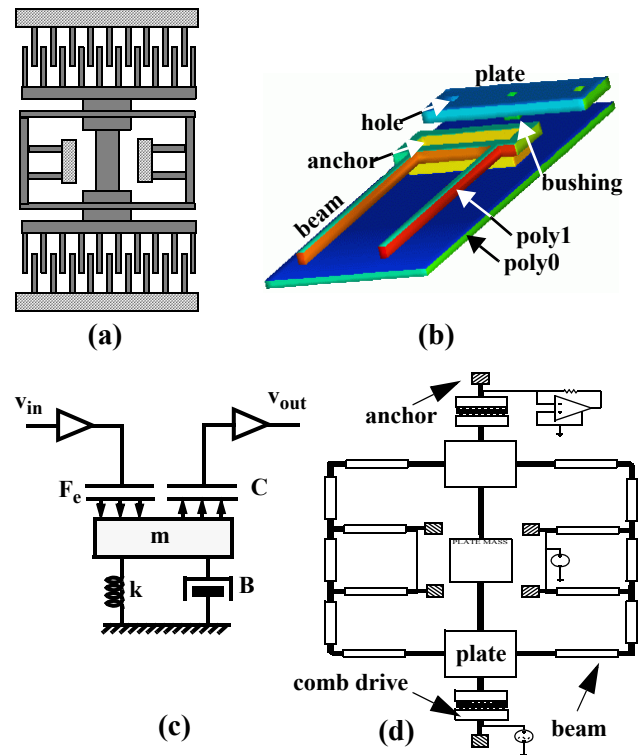

Figure 3: MEMS Design Representations of a micromechanical resonator filter with electromechanical transducer at input and output (a) layout, (b) 3D model (of portion of layout), (c) equation-based behavioral schematic, and (d) MEMS "circuit" schematic.

shown in Figure 3(a) and (b). For an entire decade, MEMS CAD research focused on methodologies based on these representations [16][17].

As MEMS research evolved from microstructure to microsystem design, a lumped-parameter representation (Figure 3(c)) [18] was imported from classical electromechanics [19]. This view, a behavioral schematic in Figure 3(c), is really a set of analytical equations that capture device performance as a function of device geometry.

The final, and most recently introduced representation is that of the MEMS "circuit" schematic of Figure 3(d) [11][13][20][21]. It is based on extending VLSI-style circuit simulation to MEMS, by identifying the commonly used MEMS circuit elements, parametrizing them by their geometric design variables and material properties, and developing models for them that are compatible with differential algebraic equation solvers within the circuit simulation tools.

2.2 Hierarchy

In addition to these representations, the iterative divide and conquer nature of design implies design hierarchy. Since the late '80s, the primary approach to traversing this hierarchy in MEMS was bottom-up [17], with the aim of encapsulating the MEMS transducer design as a fixed macromodel for system design (akin to hard-IP or discrete design). The limitation of bottom up design is the barrier to design optimization at the lowest levels of the hierarchy. In contrast, a top-down design approach provides a level of transparency to the entire design hierarchy allowing design customizations for application-specific needs.

In both top-down and bottom-up design, the primary language of communication between layers of a design hierarchy are the system (i.e., the level immediately above) and the sub-system (i.e., the current level) *design specifications*. As with analog electronics, there are two types of MEMS specifications: performance and defensive. Performance specifications allow comparison of device performance (such as transducer gain or accelerometer sensitivity). Defensive specifications ensure that the sub-system functions in the way assumed at the system (examples include cross-axis sensitivity in accelerometers if the system is assuming a primary sense direction). At the top-most level of the design hierarchy, the specifications tend to be defined by standards, such as the IEEE inertial navigation standard [22]. At the bottom-most level, the specifications set the geometry of the suspended MEMS atomic elements described in Figure 2(c).

2.3 Translators between Design Representations

In addition to translation up and down the design hierarchy, translation between the various design views described in Figure 3 (symbol, behavioral model, schematic, layout, and 3D) are needed. By using a parameterized element library as a foundation, support for translations between these representations are greatly simplified. This paper focuses on the translations described by the arrows in Figure 4, with the element library in the center enabling the parameterization needed for custom design. Schematics are constructed using the symbol representation. Behavioral models associated with the symbol capture the same electrostatic forces, mechanics, coupled electromechanics, and damping physics. The models and the schematic representation are used to evaluate the design performance through circuit-level simulation (as will be detailed in Section 3). The schematic captures both the interconnection of symbols (design topology), and the geometry parameters of each symbol (component sizing). The designer can alter design topology and element sizing and subsequently simulate the effect of these alterations using the behavioral models, thereby achieving the goal of iterative simulation-based design. Once design is complete, schematic-driven layout generation (Section 4.1) eliminates the tediousness of design entry directly at the layout representation. If the layout is manually generated or modified, layout verification is necessary, and is supported via layout extraction (Section 4.2). Finally, automatic mesh generation algorithms directly from schematic, or from layout can be used for generating the 3D solid model or mesh representations common in MEMS (Section 4.3). Although the 3D view can be used for design [17], for integrated MEMS, the 3D view is too complex for iterative design with numerical simulation, and tends to be used solely for detailed design verification; therefore translators from that representation to the alternative representations are unnecessary.

Classical bottom-up design methodologies tend to begin with a layout view that is transformed to a solid model or mesh view, or start directly from a solid model view of the MEMS device. Finite- and boundary-element modeling of the electrostatic forces, mechanics, coupled
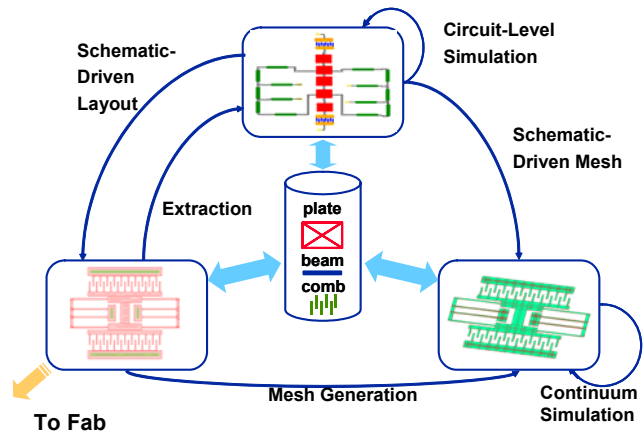

Figure 4: Integrated MEMS Design Methodology.

electromechanics and damping and numerical simulation are then used to construct reduced-order behavioral models [23][24] for system-level simulation. These reduced models are fixed for the given geometry and material properties. In contrast, the top-down schematic-based simulation relies on models parameterized by the design geometry and material properties. These physical parameterized models for each of the low-level elements such as beams that have adequate accuracy (< 10%) as compared to numerical simulation to support iterative design [20][25][26][27][28].

The design library can contain elements at several levels of the hierarchy. At the lowest level are the *atomic elements* such as beams, plates, gaps and anchors of Figure 2(c). These elements are chosen by three characteristics: they are often re-used (albeit sized by appropriate geometric parameters); they are modular (in the sense that they are decoupled from neighboring elements); and they can be accurately described by simple lumped parameter models. Additional higher-level elements can also satisfy these characteristics. In particular, the parameterized *functional elements* of Figure 2(b) are easily re-used because they capture a single function (generate electrostatic force, provide mechanical stiffness, *etc.*) and hence can be accurately represented by behavioral models [29]. While parameterized models at the *component-level* are still possible [13], the fixed topology of entire components such as in Figure 2(a) limits their potential for reuse. However, parameterized modeling at this level is very effective for design synthesis [30].

2.4 Process Abstractions

In addition to design representations and translations, process abstractions are needed for generalization across the variety of MEMS processes. As with CMOS foundries are needed to support application specific integrated MEMS designs. The number of MEMS start-ups offering unique processing capabilities has exploded in the last few years [31]. Although many of the foundries provide expertise in the development of custom processes for the product needs of the fabless MEMS design teams, the recent implosion in the optical MEMS applications is leading to their being re-targeted as standardized MEMS processes for a variety of other applications. The MUMPs family of standardized processes from MEMSCAP (of which Poly-MUMPs [32] has been in existence for a decade) is one such example. Analog Devices Inc.'s internal foundry, iMEMS^TM [33], has hosted a variety of accelerometer and gyroscope designs since 1991. Sandia's SAMPLES service provides access to 5 layers of polysilicon at 1 micron design rules [34]. The Carnegie Mellon CMOS-MEMS process [35] has been available in foundry format through DARPA support through the Application Specific Integrated MEMS Process Service [37].

As all processes are based on the same microfabrication deposition, patterning and etch fundamentals, a layered abstraction can be developed. Each process is defined by its layer definitions required for manufacturing as well as associated characterized material properties and geometric dimensions. In microelectronics, the layered process information is captured in a layout technology file, a layout design rule file, a layout parasitic extraction file and a device model file. The same four files can also be used in MEMS to map process information into the design flow. As in VLSI, the layout technology file identifies the layers available for layout (no MEMS specific changes are required).

The IC layout design rule file is supposed to be an abstraction of geometric design constraints to ensure robust manufacture. Beyond the standard microelectronics rules, MEMS design requires rules for the one unique MEMS process step: sacrificial etching for microstructure definition and device release. The undercut etch process for release in a foundry fabrication line can be characterized by the hole or gap size (related to quantity of etchant available for sacrificial etching) and the structure size (related to amount of sacrificial etching needed). High volume processes can alter etch time for optimal release of a given product. Low volume or foundry processes can only offer a constant-time release etch. For such processes the relationship between the hole/gap size and structure size required for release can be encapsulated in maximum structure width and minimum hole or gap size (i.e., a single number for each parameter), or by a non-linear function [38].

The parameterized values of the undesired resistances and capacitances are encoded in the IC layout parasitic extraction file. For integrated MEMS, the electrical parasitic parameters in the MEMS region are different than the electronics region. Additional parameters for mechanical parasitics (such as the joint between beams) are also needed [39]. The modeling of these parasitics is related to the lumped parameter modeling of the beams, and will be detailed in Section 4.2.

The success of application-specific integrated MEMS design requires both low design and fabrication cost as well as a fast time to market. Preventing fabrication iterations is therefore highly desired, and can only be attained if the device model parameters are well characterized. Although characterization approaches based on automated all-electrical testing have been proposed [41][42], many parameters such as residual stress gradients can still only be obtained by time-consuming manual methods.

Through the use of the above process abstractions, the library-based design methodology in Figure 4 can be used for single structural layer design in polysilicon technologies such as Analog Devices iMEMS^TM, MEMSCAP's PolyMUMPS and Sandia's SAMPLES as well as the Carn-

egie Mellon CMOS-MEMS process. Extensions to other MEMS processes that have which have been integrated with CMOS including deep reactive-ion-etching of silicon (Si DRIE) and thick epi-polysilicon are trivial. Structures in these processes are simply thicker versions of the polysilicon processes. Extensions to other side-wall geometries (such as the dissolved wafer process) requires additional models.

3. MEMS Circuit Simulation

Simulation of an integrated MEMS circuit schematic is needed to evaluate design performance. It uses behavioral models of physical system dynamics, and can be accomplished through signal-flow or network (circuit) representations. Recent approaches [21][28][43] have focused on the circuit representation due to interoperability with electronic circuits.

The development of a circuit representation requires identification of the physical disciplines of quantities at the terminals of a "circuit" element, as well as the relationship between these quantities within the element. The voltage at the terminal (across variable), and the current into the terminal (through variable) are commonly used abstractions in the electrical domain. Equivalently, force and torque and linear and rotational displacements as the through and across variables, respectively, in the linear and rotational mechanical domain. Once the terminal natures are defined, the physics can be modeled by relating the flow through the terminals to the potential across the terminals. This model is often called a *constitutive relationship* in network theory. In addition, as the initial position and orientation of the beam in the chip layout are important for modeling mechanics, the coordinates of the element center relative to the layout origin and the element rotation angle of the beam relative to the *X*-axis in the chip frame are included in the schematic representation. As these initial layout positions are static values which do not change during dynamic simulation, they are represented as parameters. A topological connectivity analysis algorithm calculates the layout coordinate values based on the topology and the element sizes in the schematic.

By using the same terminal natures at all levels of the design hierarchy, a composable design representation for mixed-level simulation is possible. This is particularly important as simulation of entire MEMS systems at the atomic level, though possible, may involve unnecessary long simulation times. A library consisting of commonly used atomic and functional elements therefore supports both rapid simulation as well as the capability to represent a wide class of designs [28].

Physical system simulation capabilities that interoperate with electronics are a fundamental requirement for integrated MEMS design. These capabilities are possible

through the use of mixed-signal hardware description languages, such as Verilog-AMS [44] and VHDL-AMS [45]. The examples in this paper are based on models written in Verilog-A for the Spectre™ behavioral simulator in the Cadence design framework (Verilog-A is the analog portion of Verilog-AMS) [28].

The flexibility of this design methodology is shown by two design examples. The first example is a bandpass filter composed of three identical resonators, each resonating at 550 kHz, coupled by O-springs, based on [46]. The topology of the filter (Figure 5(a)) is captured in the schematic using the mechanical symbols from the element library in Figure 4 and electrical symbols for the interface circuitry. Each of the three resonators is composed of a center proof mass, crab-leg springs, and differential electrostatic comb drives (for actuating and sensing). The stator fingers are connected to the input voltage V_{in} with 0 V DC bias. The rotor fingers are differentially DC biased at V+ and V-. Therefore, the fingers should theoretically have no DC position offset. When a sinusoidal voltage is applied to the stator fingers, electrostatic forces actuate the suspended microresonators. In the CMOS-MEMS implementation, the comb fingers consist of a stack of three metal layers and a polysilicon layer. These layers are electrically connected to the same voltage to maximize the active sidewall area of capacitance, therefore, the electrostatic force. The "O" shaped coupling spring topology employed in this design is
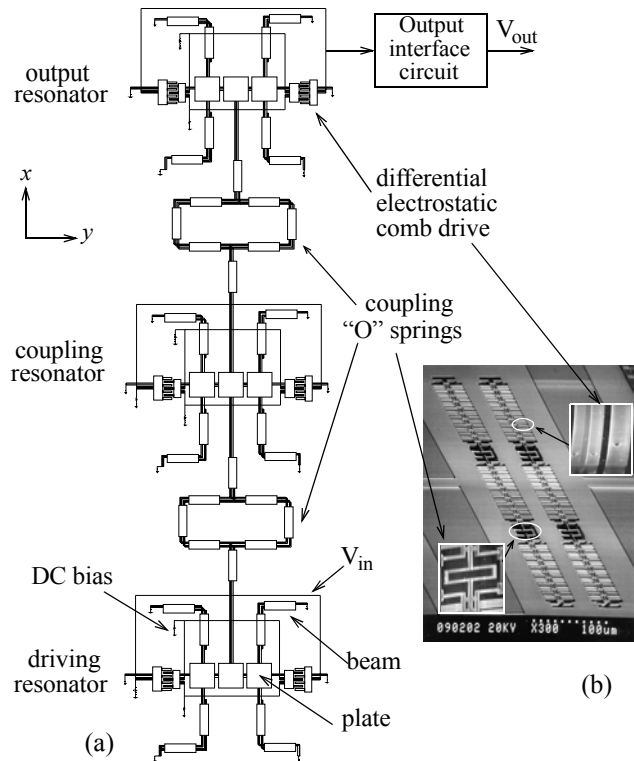

Figure 5: Schematic Representation of Crab-leg resonator filter; (b) SEM image of CMOS-MEMS implementation (two separate filters were fabricated side by side)

composed of beams with metal-2 and metal-1 only, in order to obtain softer springs, and therefore, narrower bandwidth. The three resonators resonate in *x*-direction, and are coupled at the center plates of each resonator. The SEM of two released filters and the close-ups of the differential comb drive and "O" coupling spring is shown in Figure 5(b). The device was tested in air, with the rotor fingers biased at +/-20V. Figure 6 shows the frequency response of the CMOS-MEMS bandpass filter (output voltage of interface circuit) with comparison to experimental data [47]. Simulations with a comb drive macromodel, in which the comb fingers are assumed to be rigid [29], is compared to simulation with gap and beam models, in which the compliance of comb fingers is considered [28]. The comparison shows that the simulations matches the experimental results to within 3%. With gap and beam models, the frequency reduction due to the compliance of comb fingers is captured.

The second example is a CMOS-MEMS accelerometer, whose schematic is shown in Figure 7(a). It is a fully differential common-centroid accelerometer using the topology described in [48]. Sensing nodes are located at stators instead of rotors to minimize parasitic capacitance. Differential modulation signals are routed through the serpentine spring by the two metal layers under the top metal layer of the CMOS metal stack. The simulations using the integrated MEMS design methodology were compared with experimentally measured results as in Figure 7(c). The resonant frequency and sensitivity simulated results are within 10% of the measured data. The noise simulation reported only considers Brownian noise and vastly underestimates the sensor noise.

4. Layout Generation & Verification

Once a MEMS schematic has been composed, and simulation results used to improve the design until the
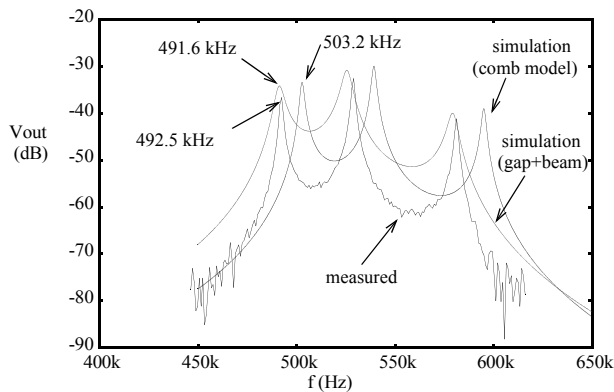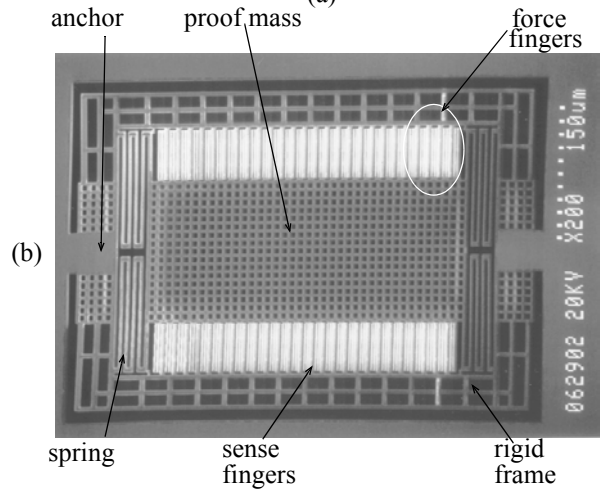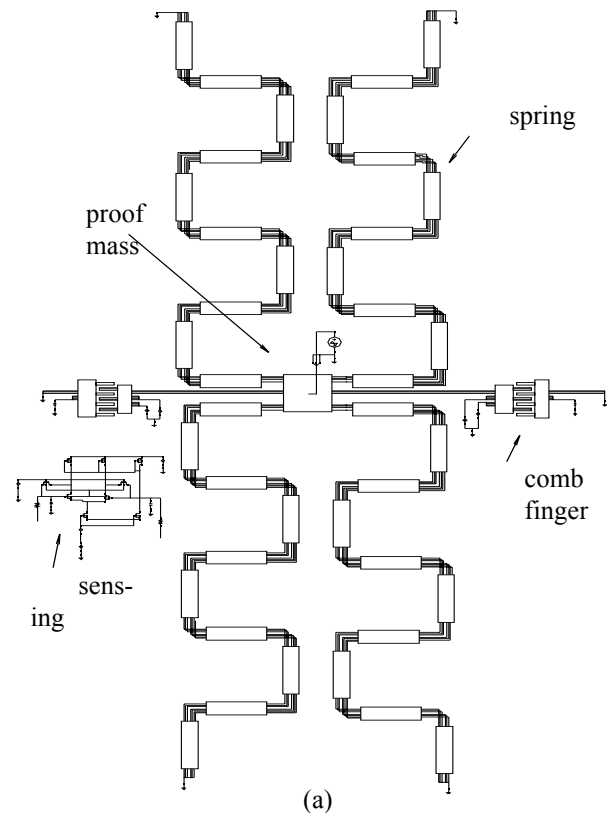

(a)

(b)

Figure 6: Measured output voltage of sensing interface circuit and output voltage from NODAS simulations with rigid combdrive macromodel and gap model.

	Simulated	Tested
Resonant frequency	5.9 kHz	6.1 kHz
Sensor sensitivity	0.6 mV/G	0.5 mV/G
Noise	$28\mu G/\sqrt{Hz}$ (Brownian only)	$1mG/\sqrt{Hz}$ (total)

(c)

Figure 7: (a) Schematic of CMOS-MEMS Accelerometer; (b) SEM image of (rotated) accelerometer; (c) Simulation vs. Measured results.

desired specifications are met, a layout needs to be generated.

4.1 Parametrized layout generation & DRC

As manual layout generation is cumbersome and error-prone, automated approaches are needed. Parametrized layout generation for commonly used MEMS functional elements from a text file [49] or library palette in the layout editor have been demonstrated [50]. These functional elements are then manually placed and connected by abutment. For fully-automated layout generation, element positions are needed. This can be computed using topological analysis of the schematic connectivity (and is also used for simulations in Section 3). Essentially this approach takes advantage of the one-to-one correspondence between the schematic and layout.

Following layout generation, verification involves design rule checking, electrical and mechanical rule checking and layout and parasitic extraction. Commercial design rule checking tools can be used for integrated MEMS by implementing a non-linear function between hole and gap size and undercut [38]. The design rules that need to be checked in the MEMS areas are different from those in the circuit areas. This can be accomplished with multiple rule checks runs with flags to enable or disable electronics or MEMS rule checking as desired by the designer.

4.2 Layout Extraction

Due to the lumped parameter modeling of the schematic elements, the joint between two beams in a flexure behaves as a mechanical parasitic. If one of the beams incident at the joint is significantly wider than the other beam, then the moment arms at the joint also need to be considered, necessitating the use of a rigid plate to model this joint [39].

Due to the sacrificial etch involved in releasing the MEMS, the interlayer parasitic per unit area capacitances in the MEMS portion will be different from those in the electronics portion. Integrated MEMS extraction therefore needs to partition the chip layout into the MEMS and electronics portion, and extract each portion separately for layout parasitics. The two portions can then be combined by linking the extracted MEMS and electronic schematics for the simulation. This integrated simulation of the extracted layout can capture the loss in sensitivity of the comb sensor (due to capacitance) and noise (due to series wiring resistance). These parasitics can also generate forces that can lead to undesirable mode coupling or device instability. Simply simulating the effect of the MEMS parasitics on the MEMS element and the electronics parasitics on the electronic elements ignores the potential interaction between these parasitics. For example, a closed-loop system's loop
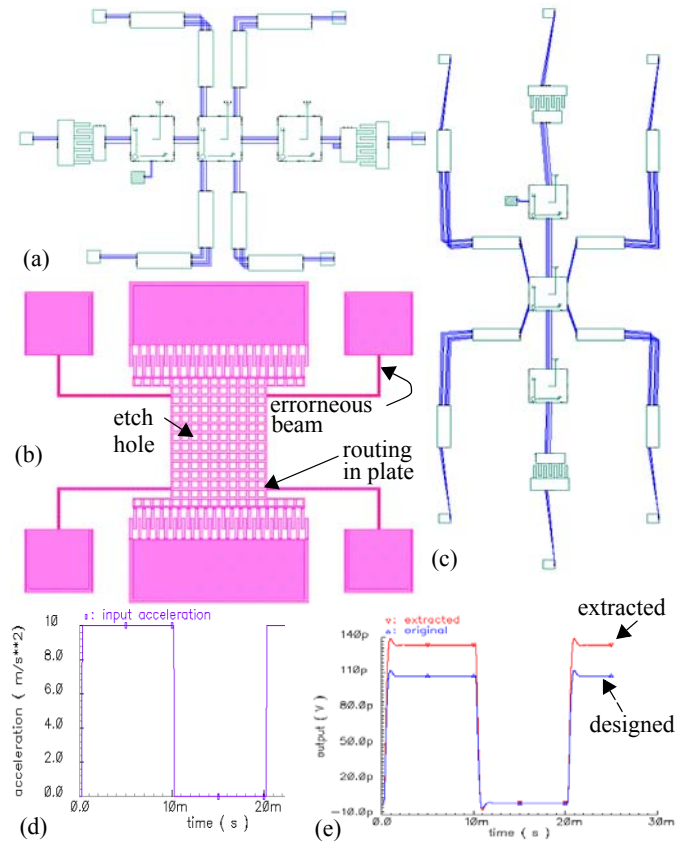

Figure 8: Crab-leg accelerometer. (a) designed schematic, (b) layout rotated by 90°, (c) extracted schematic, (d) input to the two schematics, (e) comparison of outputs from designed and extracted schematics

transmission, and hence stability, may be affected by the parasitics on both the MEMS and electronics side.

Extraction involves recognition of the atomic elements and the functional elements from the layout to construct a schematic with element parameters and parasitics. General feature recognition algorithms for surface micro-machined MEMS have been developed to identify the atomic elements [53]. Technology-specific information from other layers, like location of anchor cuts, is used to help in this phase. Additional identification of the functional elements based on electrical connectivity analyses for comb-drives and mechanical connectivity analysis for flexures and has also been developed [54]. LVS capabilities can be built on top of extraction to verify layout symmetry (which is important for achieving defensive specifications for many MEMS devices) [55].

Figure 8 shows an example of a crab-leg accelerometer which was verified using an extraction-based LVS methodology [55]. Figure 8(a) shows the designed schematic for the accelerometer from which the layout was automatically generated. The layout (Figure 8(b)) was rotated by 90°, for placement in the full system and routing for the comb

drives was added using lower metal layers in the plate region. The extracted schematic is shown in Figure 8(c). One of the beams (shown as erroneous beam in Figure 8(b)) was accidentally changed in width. When MEMS LVS was used to check the two schematics, the LVS failed and reported the path from the anchor attached to the erroneous beam to be faulty. Correcting the width of the beam resulted in a successful LVS even though the orientations of the two schematics were not the same. However, when the two schematics were simulated with an acceleration input as shown in Figure 8(d), the sensitivity of the extracted schematic and hence the actual layout was found to be better than that predicted by the design schematic (Figure 8(e)). This results from the additional mass contributed by the routing metal wires in the final layout. This example demonstrates the usefulness of the LVS methodology in catching layout errors and also proves the importance of mechanical parasitics in predicting the true behavior of the final design.

4.3 Meshing from Layout

As the post-extraction simulation uses lumped parameter models, the traditional solid-model and meshing approach for numerical simulation is desirable for final verification. Automatic meshing capabilities are now routine in commercial MEMS analysis tools from CFDRC [56], Coventor [57], Intellisense [58] and MEMSCAP [13]. An automatic technique for meshing multilayer CMOS micromachined structures for Finite Element Analysis (FEA) from device layout is described in [59]. The technique is based on a 3D canonical representation of the different CMOS layers and feature recognition of plate masses, springs, beams and comb drives within the surface micromachined MEMS device. Meshing heuristics derived from past experience and knowledge of structural features to improve mesh quality are encoded in a rules file and the extraction-based element recognizer. This approach results in a FEA mesh that is computationally more efficient that conventional automeshers that have no knowledge of the geometry. The resulting computation time is found to be an order of magnitude faster than uniform meshing, with less than 5% difference in accuracy.

5. Conclusions

MEMS design and verification requires the integration of several commercial and academic point tools into a design flow to enable rapid custom design of low volume MEMS. By reducing the time to a working design, this flow dramatically increases design productivity and enabling MEMS to become inexorably embedded into the information appliances of tomorrow.

By using a modular basis for the design flow, the primary design entry point is shifted from solid modeling and/ or layout to *schematic* entry. The use of an extendible library of elemental schematic symbols, behavioral simulation models and layout and mesh generators forms the core of the design methodology. The parameterized MEMS library is similar to a parameterized analog device library increasingly being available from semiconductor foundries as physical design kits. This MEMS library is process independent, and when coupled with process dependent technology abstractions, is able to support the coupling of custom-designed MEMS-enabled sensing and actuation with traditional electronics leading to application specific integrated microsystems.

6. Acknowledgement

7. References

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