MEMS FABRICATION

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ABSTRACT

This summary of selected microelectromechanical systems (MEMS) processes guides the reader through a wide variety of fabrication techniques used to make micromechanical structures. Process flows include wet bulk etching and wafer bonding, surface micromachining, deep trench silicon micromachining, CMOS MEMS, and micromolding.

1. Introduction

Microelectromechanical systems (MEMS) technology encompasses an enormous variety of applications, including sensors of almost any kind, imagers, ink jets, micropositioners, optical beam steering and filtering, microphones, RF tunable components and switches. Microfluidics is a specialty area that has grown out of merging MEMS technology with the physics of fluid dynamics, chemistry and increasingly the biological sciences. The common thread binding these disparate application themes is the ability to manufacture devices and systems using batch microfabrication processes. MEMS are made using the same standard process steps used in integrated circuit manufacturing, including photolithography, wet and dry etching, oxidation, diffusion, low-pressure chemical vapor deposition (LPCVD) and sputter deposition. Some unit processes, such as plating, molding and substrate bonding, are more common in MEMS than in mainstream IC manufacture.

Prior to around 1996, almost all MEMS process flows could be binned into two primary types: bulk (also called substrate) micromachining and surface micromachining. Bulk micromachining encompasses flows that exploit preferential etching of silicon, glass or other substrates to form micromechanical structures. It is most widely known commercially in production of membranes for pressure sensors and nozzles for inkjet printing. Surface micromachining flows create microstructures out of thin films on the substrate surface. Commercial examples of components made from surface micromachining include airbag accelerometers and micromirror projection arrays. Example structures arising from these two types of flows are given in Figure 1.

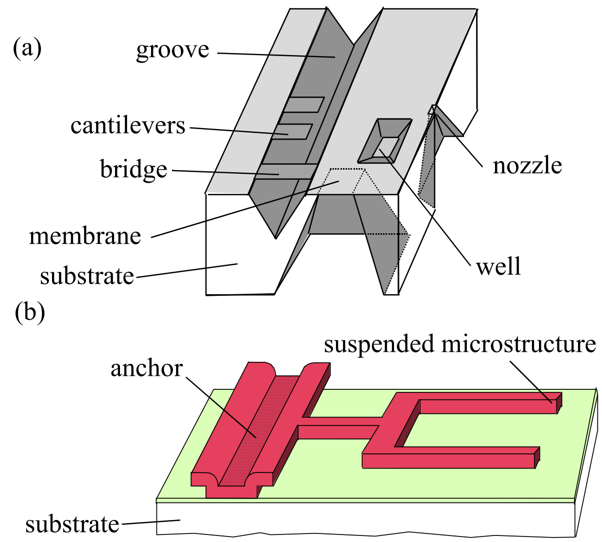

Figure 1. (a) Bulk micromachining. (b) Surface micromachining.

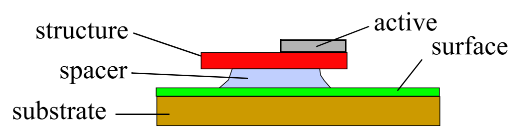

Figure 2. Categories of micromechanical materials. Shown is an example for surface micromachining.

2. MEMS Materials

Requirements of a MEMS process flow are inclusion of one or more mechanical materials, unit processes to shape (micromachine) these materials and, in most cases, unit processes to release parts of the structural material from other anchored materials. The choice of micromachining process usually starts with a specification of device dimensions and tolerances. Structures over 10 µm in thickness usually dictate bulk micromachining, while structures under 10 µm usually incorporate surface micromachining or hybrid bulk/surface micromachining.

There are five main categories of micromechanical materials, as shown in Figure 2. The structural material and substrate material, which may be one in the same, must be able to survive the various process steps. Structural material properties of interest include Young's modulus, yield strength, density, residual stress and stress gradients, electrical and thermal conductivity and long-term stability of these properties. Spacer materials are usually completely or partially etched away to release the microstructure, and are often called sacrificial materials because of this function. Spacer materials may also be used to make molds for structures. Surface materials may be used to protect the substrate or structural material from certain etching steps. Surface materials are also important for achieving electrical isolation.

Active materials are incorporated on structures to exploit their special physical transduction characteristics. Probably every possible transduction mechanism has been explored in MEMS. Common transduction effects are silicon piezoresistance to measure stress, the piezoelectric effect in ZnO, PZT, AlN for both stress sensing and actuation, temperature coefficient of resistance and thermoelectric properties of silicon, aluminum and other conductors to measure temperature, and various magnetic materials to couple mechanically to magnetic fields.

3. MEMS Process Flows

No single process flow can be used to fabricate all possible MEMS. However, a handful of canonical process flows cover the basic MEMS fabrication concepts and form a basis for many other derivatives. The canonical process flows covered in the following discussion are silicon wet etching and bonding, surface micromachining, deep reactive-ion etched silicon micromachining, CMOS MEMS, and microstructural molding processes.

Silicon wet etching and bonding

Silicon is a very useful micromechanical material with Young's modulus and high yield strength similar to stainless steel. For micromechanical applications, it is extremely robust and stable material. Several anisotropic silicon etchants exist (e.g., potassium hydroxide (KOH), ethylene diamene pyrocatechol (EDP) and tetramethyl ammonium hydroxide (TMAH)), which exhibit preferential etching along the <100> and <110> crystallographic directions and orders of magnitude smaller etch rate in the <111> direction. Silicon etch pit orientation in a <100> wafer is shown in Figure 3 for a timed etch. A long etch will terminate everywhere on {111} planes. The alkaline nature of these etchants rules out conventional photoresist masking. Instead. silicon oxide or silicon nitride masks must be used.

The etch rate is reduced by about 50 times for heavily boron doped silicon, which can serve as an etch stop. Alternatively, electrochemical etching in HF can be configured to stop on n-type silicon to form lightly-doped membranes. The membrane cross-section in Figure 3(c) illustrates the

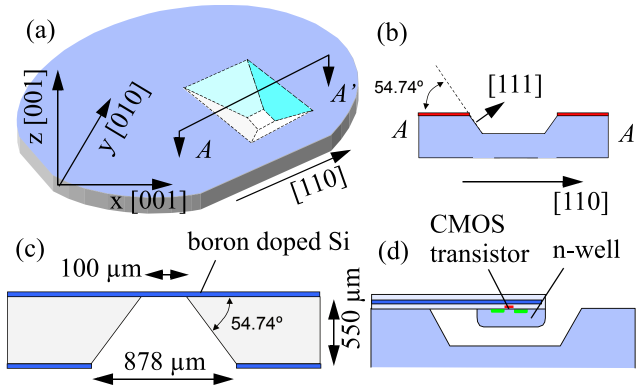

Figure 3. Bulk micromachining. (a) Anisotropically wet etched pit in <100> Si wafer. (b) Cross-section of pit. (c) Membrane formation using backside wet etch. (d) Electrochemical etch formation of a suspended n-well in CMOS.

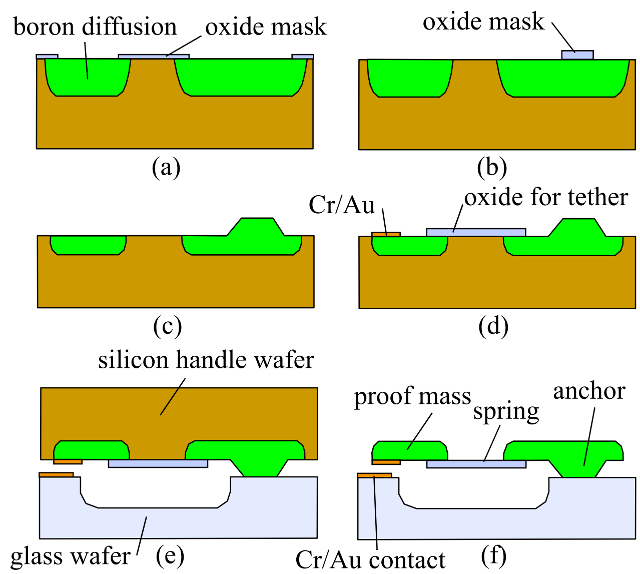

Figure 4. A dissolved wafer process. (a) Masked boron diffusion. (b) Silicon oxide deposition and patterning for silicon etch. (c) Silicon etch and mask strip. (d) Silicon oxide deposition and patterning; Chromium and gold deposition and patterning. (e) Anodic bonding. (f) Dissolve handle wafer for release.

expanded area required for the backside wet etch technique. Such membranes are the basis for silicon pressure sensors with diffused piezoresistors for membrane stress readout. Electrochemical etching can also be used to create suspended n-wells in CMOS, tethered by the CMOS interconnect layers as shown in Figure 3(d). Such microstructures have been used to make thermally isolated transistors [1].

The dissolved wafer process combines wet silicon etching and wafer bonding to form boron doped microstructures on a glass substrate [2]. A process flow is shown in Figure 4 for an inertial latch, which closes a gold contact when exposed to a threshold acceleration [3]. The "handle"

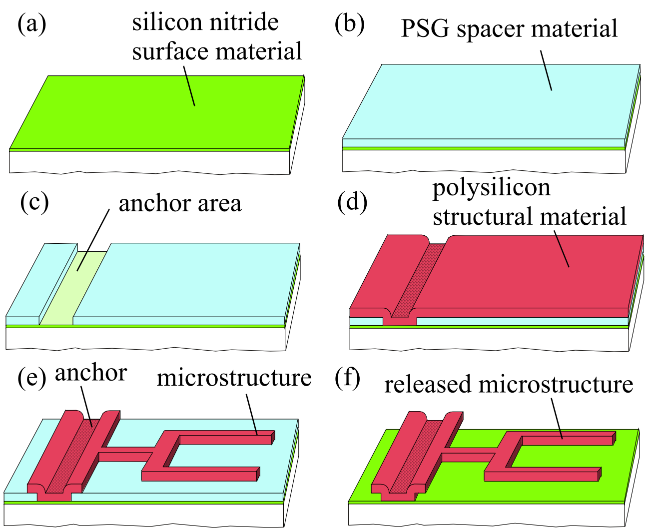

Figure 5. Process flow for single-layer polysilicon surface micromachining.

silicon wafer is a sacrificial mold for defining the height of the microstructures. Thin silicon oxide layers may be deposited to make electrically isolating springs as shown in Figure 4(d). The front side of silicon wafer with the patterned structural layers is anodically bonded to a glass substrate with gold interconnect. The glass substrate has excellent bond strength to silicon. For capacitive sensor applications, the glass eliminates capacitive parasitics that would be present if a conductive silicon substrate were used instead. The structures are released by etching the entire handle wafer in a wet silicon etchant.

Surface micromachining

Advantages of surface micromachining are a) structural and spacer features, especially thicknesses, can be smaller than 10 µm in size, b) the micromachined device footprint can often be much smaller than bulk wet-etched devices, c) it is easier to integrate electronics below surface microstructures, and d) surface microstructures generally have superior tolerance compared to bulk wet-etched devices. The primary disadvantage is the fragility of surface microstructures to handling, particulates and condensation during manufacturing.

Polysilicon (polycrystalline silicon) micromachining is arguably the most common form of surface micromachining. Polysilicon has mechanical properties similar to single-crystal silicon, which explains its popularity for MEMS. A basic process flow, shown in Figure 5, starts with low-pressure chemical vapor deposition (LPCVD) of a thin silicon nitride layer on top of a silicon substrate (a). This layer provides electrical isolation of subsequent structures from the substrate. Often, the layer is silicon-rich nitride, which can have much less tensile stress than stoichiometric Si_3N_4. and

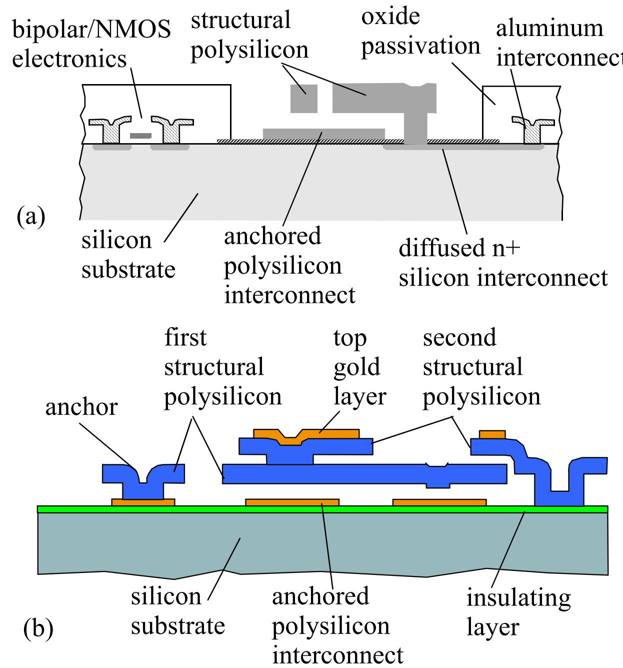

Figure 6. Cross sections of some commercial polysilicon micromachining processes. (a) ADI iMEMS. (b) MUMPs.

thus adheres well to the substrate. The spacer layer (b) is a 2 µm-thick layer of LPCVD phosphosilicate glass (PSG), which is patterned to form what will be structural anchors to the substrate (c). The next process step is LPCVD of phosphorous-doped polysilicon forming a 2 µm-thick structural layer (d). The polysilicon is dry etched to define the microstructures and to expose the underlying spacer layer (e). A hydrofluoric acid (HF) etch step removes the spacer layer around and under the structure, releasing it from the substrate (f). HF has a small but finite etch rate for polysilicon and silicon nitride, so the required etch time for release must be bounded. Large microstructures must have spaced-apart holes designed into them to allow the release etch to remove the underlying spacer. The microstructures are then rinsed in water and dried. Often, the surfaces are treated with a hydrophobic self-assembled monolayer prior to the drying step to prevent surface tension effects from causing structures to stick to the substrate or to each other. Alternatively, polymer pedestals, which are later removed by oxygen plasma ashing, may be employed as temporary spacers during wet etch release.

The iMEMS™ process, shown in Figure 6(a), from Analog Devices Inc. (ADI) integrates one structural polysilicon layer with BiMOS electronics and is used to make the company's line of inertial microsensors. The high-temperature polysilicon MEMS steps are performed after the BiMOS device fabrication but prior to aluminum metallization. After step (e) in Figure 5, more complicated multi-layer microstructures can be formed by repeating the spacer and structural material depositions and patterning steps (b) through (e). Two released structural layers are provided in the popular MUMPs process [4] depicted in Figure 6(b), while up to five polysilicon structural layers are provided in the Sandia SUMMiT-V process [5]. These extra layers allow more design freedom to create hinged structures, rotary gears and joints, and other articulated mechanisms. Improving bearing surfaces in these 3-D structures are a primary factor in increasing reliability.

Some other combinations of materials for surface micromachining are given in Table 1. Alternative processes follow the same order of surface material deposition, spacer material deposition, structural material deposition, and spacer etch for structural release. Common applications include silicon nitride structures for thermally isolated platforms, polyimide structures for shear stress sensors, aluminum structures for micromirrors, gold structures for RF switches and parylene microfluidic channels. The low deposition temperature of LPCVD polysilicon germanium (polySiGe) microstructures have made it a current research topic, motivated by the ability to micromachine the structures directly on top of foundry CMOS.

Table 1: Selected surface micromachining choices

Structural material	Spacer material	Surface material	Spacer etchant
polysilicon or polySiGe	silicon oxide	silicon nitride	hydrofluoric acid
polyimide	aluminum	silicon oxide	phosphoric/acetic/nitric (PAN)
aluminum or gold	polyimide	silicon oxide	oxygen plasma
parylene	photoresist	parylene	acetone

Microfluidic channels are often made by etching channels into polymers and then bonding a polymer or glass cover over the channels. Channels have been made in numerous polymer materials; no sacrificial material is needed. As one example, Epon SU-8 is an epoxy-based transparent ultraviolet (UV) sensitive negative photoresist, which has developed features with aspect ratios of greater than 10:1 and thicknesses of greater than 200 µm. More complex 3-D filter structure can be created in SU-8 by performing multiple exposures at different substrate tilt angles with respect to the UV source [7][8].

Microchannels may also be created through surface micromachining of any suitable structural material. The sacrificial material acts as a mold for the channel and is removed during the release etch. A process with two structural parylene layers has produced a variety of microfluidic channels, valves and pumps [6]. In this case, the sacrificial material is photoresist. In most of these processes, sealed cavities can be formed by depositing structural material across the cavity inlets after the release etch.

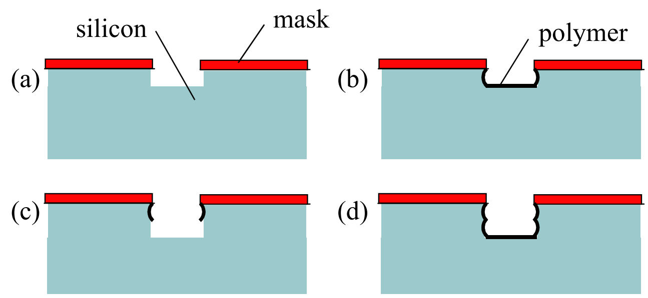

Figure 7. Sequence for the Advanced Silicon Etch (ASE) process.

DRIE silicon micromachining

In 1996, an Advanced Silicon Etch (ASE™) process was introduced that can make trenches in silicon with depth to width aspect ratios over 20:1 and with nearly vertical sidewalls [9][10][11]. The deep trench etch sequence is illustrated in Figure 7, and is also known as deep reactive-ion etching (DRIE). The mask is usually either photoresist or silicon oxide, however other mask materials can be used. In step (a), a high density inductively coupled SF_6 plasma etch achieves selectivity to the mask of around 100:1. The etch is normally run for about 8 to 12 s, which corresponds to around a 0.2 to 0.5 µm etch depth. The gas in the plasma chamber is then switched to C_4F_8 for around 8 s, which deposits a thin fluorocarbon polymer onto the wafer surface. The following etch step (c) uses physical ion assist to etch the polymer at the bottom of the trench, leaving some sidewall polymer. The polymer masks lateral etching and thereby maintains the vertical sidewall profile. The desired trench depth is obtained by cycling etch steps (a) and deposition step (b), with an effective etch rate of around 1 µm/min. The effective etch rate is a function of the trench aspect ratio, an effect known as aspect-ratio dependent etching (ARDE).

Silicon-on-insulator (SOI) MEMS and epitaxial MEMS process flows, illustrated in Figure 8, exploit the ASE process to create high-aspect-ratio silicon suspended microstructures. Thick SOI substrates are made by wafer to wafer bonding. Alternatively, silicon structural layers up to 10's of microns can be grown by epitaxy. Substrates for SOI electronics have top silicon thickness of much less than 0.1 µm and are not generally used for MEMS. Microstructures are defined with ASE, then the structures are released by a timed etch in HF of the underlying silicon oxide spacer layer. These processes have aspects of both bulk and surface micromachining. They are popular due to the process simplicity and the ability to make SCS microstructures with

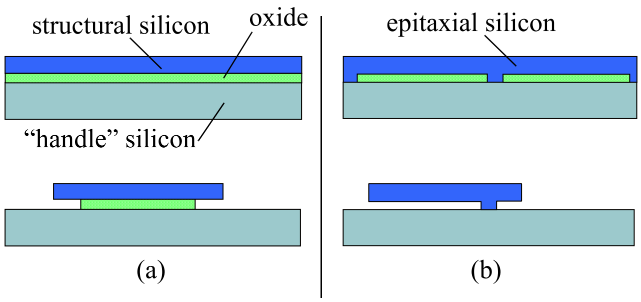

Figure 8. (a) SOI MEMS. (b) Epitaxial silicon micromachining.

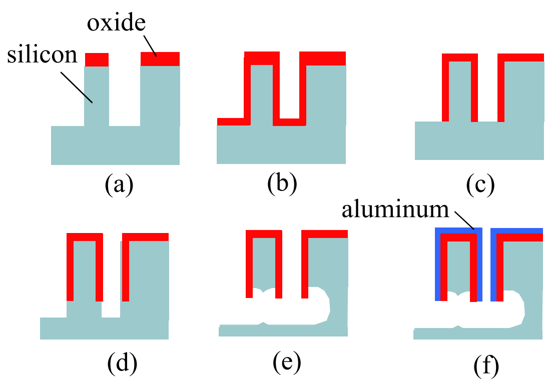

Figure 9. SCREAM MEMS. (a) Silicon DRIE. (b) Conformal oxide deposition. (c) Timed, directional oxide etch. (d) Silicon DRIE. (e) Isotropic silicon etch. (f) Metallization.

thicknesses typically ranging from 5 to 100 µm. Electrically insulating the SOI microstructures may be accomplished by forming the structures on pedestals of underlying oxide (as shown in Figure 8(a)), or by refilling thin trenches around the structural anchors with LPCVD or thermal oxide, which must then be protected from the subsequent HF release etch.

SCREAM (Single Crystal Reactive Etch and Metallization) is a process flow to make high-aspect-ratio silicon microstructures with metallized sidewalls [12]. The bulk silicon serves as both the structural and sacrificial material. The process, shown in Figure 9, begins with a silicon trench etch that sets the microstructure height (a). The silicon is then masked with a conformal plasma enhanced CVD (PECVD) silicon oxide layer (b). The oxide at the bottom of the trench is reactive-ion etched (RIE) away keeping oxide on the sidewall and on top of the substrate (c). Subsequent silicon RIE creates a deeper trench into the substrate (d). Then, switching to a timed isotropic silicon etch with SF_6 plasma or XeF_2 gas undercuts and releases the silicon microstructure (e). A final sputter deposition of metal coats the top and sidewalls of the structures to form highly conductive electrodes for electrostatic actuation or capacitive sensing (f). This process has potential to be integrated with foundry CMOS, as all micromachining steps can be low temperature.

CMOS MEMS

The term "CMOS MEMS" most often describes processes that create microstructures directly out of the metal/dielectric interconnect stack in foundry CMOS. The metallization and dielectric layers, normally used for electrical interconnect, now serve a dual function as structural layers. For example, the suspended n-well of Figure 3(d) is considered CMOS MEMS, since its beam suspension is made from the CMOS interconnect stack.

There is significant motivation for making MEMS out of CMOS. Leveraging foundry CMOS for MEMS is fast, reliable, repeatable, and economical. Electronics can be placed directly next to microstructures, enabling arrayed systems on chip. In CMOS MEMS, multiple conductors can be placed inside of the microstructures, which enables placement of multiple electrically isolated capacitive sensors and electrostatic actuators. The gate polysilicon can be embedded in the microstructures as heater resistors, piezoresistors, or thermocouples.

The first reported CMOS-MEMS processes produce microstructural sidewalls by stacking the drain/source contact cut and metal via cuts in the CMOS and removing the metallization layers above the cuts [13]. The substrate is exposed in the cut regions. A wet or dry isotropic silicon etch undercuts and releases the microstructures. Gaps between microstructures are limited to several microns because of artifacts in the etch pits from etching metal above the CMOS contacts. Such microstructures are commonly used to make thermally isolated and vertically actuated structures integrated with electronics.

A modification of the original CMOS-MEMS process is shown in Figure 10 [14]. The first post-CMOS micromachining step is a CHF_3:O_2 RIE (b). The top-most metal layer acts as a highly selective mask which defines the microstructures. The RIE etches any dielectric (*i.e.,* overglass, intermetal oxide/nitride, and field oxide) that is not covered with metal. Silicon DRIE then sets the spacing from the microstructures to the substrate (c). The final step is an isotropic silicon etch for structural release. The etch is usually timed to undercut structures around 20 µm wide. Larger structures must have etch holes for proper release. This process flow does not violate CMOS design rules and is readily implemented after advanced sub-0.5 µm CMOS, which has tungsten via plugs and chem-mechanically planarized (CMP) interconnect. Sub-micron gaps can be made between structures, enabling capacitive sensors and electrostatic actuators with high sensitivity.

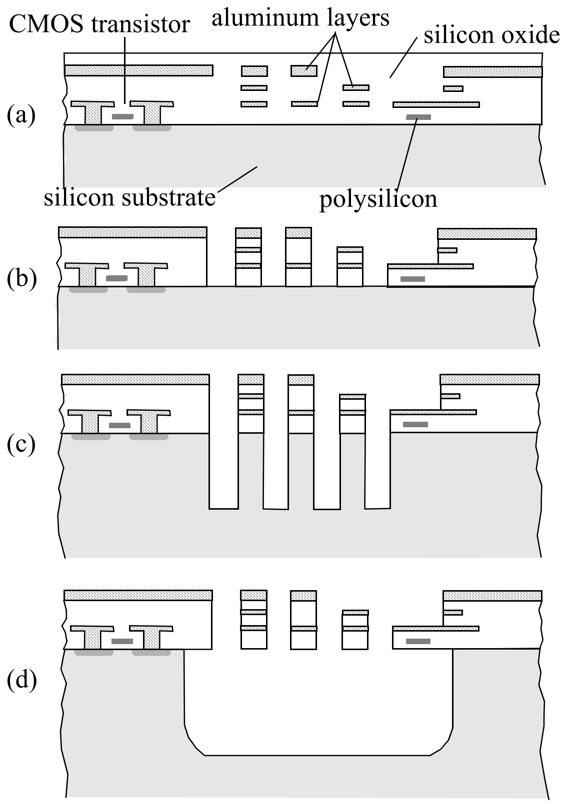

Figure 10. CMOS MEMS. (a) Foundry 3-metal CMOS. (b) Oxide RIE. (c) Silicon DRIE. (d) Isotropic silicon etch.

Microstructural molding processes

Polymer micromolding is a common way to make microchannels, because of the ease of processing, low cost, and bio-compatibility. Molds with micron-scale features may be made from photosensitive polymers (e.g., SU-8) or by DRIE silicon micromachining. Poly(dimethylsiloxane) (PDMS) is often chosen as the microstructural material [15]. PDMS is spin cast onto the mold, cured and peeled off. A short exposure in an oxygen plasma activates the PDMS surface and results in instant bonding to other PDMS or glass surfaces. Other polymers may be molded onto silicon masters through either hot embossing, casting, or injection molding.

Micromolding processes are also used to create microstructures from materials that are difficult to etch selectively, or to create very high-aspect-ratio structures. An example of the latter use is a process flow called HexSil, which forms vertical high-aspect-ratio (HAR) polysilicon structures [16]. The structure formation, as shown in Figure 11, exploits the extremely conformal deposition of LPCVD polysilicon. Trenches is a silicon substrate are first formed with DRIE (a). A conformal oxide is deposited on the silicon surface (b), followed by conformal LPCVD polysilicon to fill the trench (c). A CMP step removes the top layer of

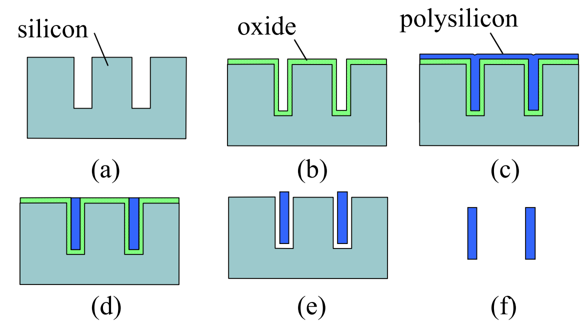

Figure 11. Basic HexSil process. (a) Silicon DRIE. (b) Oxide deposition. (c) LPCVD polysilicon. (d) CMP. (e) HF etch. (f) Release of substrate mold.

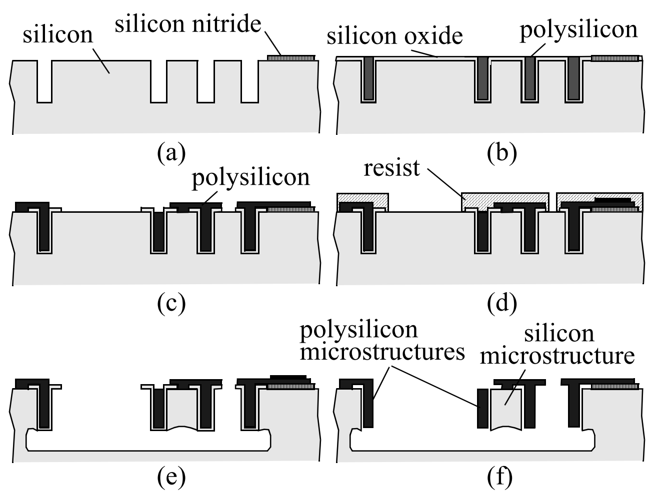

Figure 12. HARPSS process. (a) Deposit and pattern silicon nitride; DRIE silicon. (b) LPCVD silicon oxide; LPCVD polysilicon; CMP. (c) Pattern oxide; deposit and pattern polysilicon. (d) Deposit Cr/Au; Pattern resist for subsequent DRIE. (e) DRIE silicon; timed isotropic etch silicon for undercut. (f) HF etch for release.

polysilicon, and exposes the oxide trench liner. An HF etch with surfactant releases the HAR polysilicon rib structures. Plate structures can be made by forming a honeycomb pattern with the vertical ribs. By skipping the CMP step (d), polysilicon plates with vertical stiffening ribs can be made.

Variations on the polysilicon molding process may be used to make very narrow lateral gaps between microstructures. For example, the HARPSS (High Aspect Ratio Polysilicon-Silicon) process, shown in Figure 12, employs a similar molding concept as HexSil to form sub-micron gaps between released bulk silicon and polysilicon structures [17]. High-frequency silicon resonant structures with narrow gaps have also been formed with this process.

Silicon carbide (SiC) microstructures withstand extremely high temperatures and are corrosion resistant. However, silicon carbide is difficult to pattern with wet or dry etchants, because of poor mask selectivity. Instead, silicon dioxide or polysilicon molds may be used to define

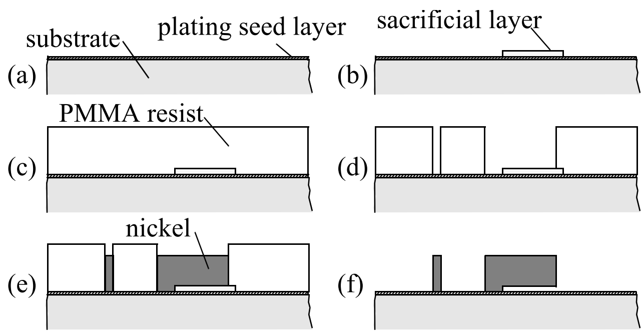

Figure 13. A basic LIGA process. (a) Metal deposition. (b) Sacrificial layer deposition and patterning. (c) Cast PMMA. (d) Expose to x-rays and develop. (e) Plate nickel. (f) Etch PMMA and sacrificial layer for release.

polycrystalline SiC microstructures [18]. SiC deposited by atmospheric pressure CVD at 1050 °C fills the molds. CMP is then performed to planarize the SiC layer to the level of the mold. This molding, SiC deposition, CMP sequence can be repeated several times, resulting in multilayer polysilicon carbide microstructures similar to the polysilicon surface micromachined counterpart [19].

LIGA is a German acronym for lithography, plating (galvanoformung) and molding (abformtechnik) [20]. A basic process flow to form moving structures is shown in Figure 13. One possible substrate is silicon covered with a metal seed layer for plating. An optional sacrificial layer of silicon dioxide, polyimide or other metal may be patterned on the substrate for subsequent release of the microstructures. Poly(methylmethacrylate) (PMMA) resist is cast onto the substrate and lithography is performed with x-ray synchrotron radiation. The x-ray radiation requires masks with over a 5 μm-thick metal absorbing layer. The developed PMMA has vertical sidewalls and can be millimeters thick. Nickel is electroplated in the PMMA mold, taking care not to plate up to the top of the trenches. The PMMA is then dissolved in solvent to release the nickel microstructures. The nickel structures may be used as a mold for subsequent plastic microparts, though this step is not shown in the figure.

Access to x-ray synchrotron radiation is limited. As a low cost alternative, the plating mold may be made from a UV-photosensitive polyimide or SU-8 resist. The trade-off is thickness limited to about 100 μm and a limited aspect ratio.

4. Conclusion

MEMS fabrication incorporates numerous materials within an enormous variety of different process flows. This short tutorial is not at all comprehensive. Several good books cover the area [21][22][23][24], though any book becomes dated as MEMS fabrication innovations continue to be reported. The interested reader is encouraged to browse through the major journals in the MEMS field, where virtually all of the fabrication concepts are published [25][26][27][28].

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