21.1 Tunable RF and Analog Circuits Using On-Chip MEMS Passive Components

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RF microelectromechanical systems (RF MEMS) are expected to address the lack of on-chip high-Q tunable passives for >5GHz transceivers [1]. Although MEMS filters [2] can potentially be integrated, insertion loss at GHz frequencies remain larger than 3dB that is obtainable using conventional off-chip components. Minimizing losses requires compact metal interconnect in the passive structures. Such metal MEMS may be embedded within custom CMOS redistribution layers for RF switches [3]. Post-foundry micromachining of the metal/dielectric interconnect stack and undercut of the silicon for release [4] is an alternative process previously applied for integrated sensors, but only recently to RF BiCMOS processes. This approach integrates RF electronics with suspended inductors and reconfigurable capacitors whose performance is enhanced by MEMS at GHz frequencies, as well as with resonant RF MEMS mixers that take advantage of ultra-high-Q MHz mechanical filtering. MEMS enhanced Q factor and wide tuning range has enabled entirely on-chip design of voltage-controlled oscillators (VCOs) with lower power and phase noise, passive RF filters with low insertion loss, and low-power low-area mixers, for potential use in multi-band applications.

A reconfigurable wideband receiver architecture that exploits all of the MEMS passives is shown in Fig. 21.1.1. The bandpass filter (BPF) and VCO simultaneously reconfigure to select 100MHz bands from the 100MHz to 10GHz spectrum. A low-noise amplifier (LNA) amplifies the output of the BPF and drives an array of MEMS mixer-filters. Each mixer in the array down-converts the received signal from GHz frequency band to a unique intermediate frequency (IF), set by the mechanical device resonance in the MHz range. Each array element also acts as a channel selection filter with a 100kHz bandwidth (centered around f_{r1} to f_{rN} in Fig. 21.1.1).

The first-generation RF MEMS BPF is a low-pass Butterworth network connected to ground-signal-ground (GSG) pads with dc blocking MEMS capacitors (C_{dc}) [5]. Fig. 21.1.2 shows the 0.09mm^2 6nH symmetrical spiral inductor surrounded by four 0.13mm^2 MEMS capacitors. Micromachining removes the dielectric between the 8μm-wide aluminum turns to increase self-resonance by 2x, and removes about 30μm of silicon under the turns to improve Q by 1.5x [6]. The BPF is the first integration of multiple MEMS capacitors [7] into a CMOS chip. Switching between 1.7 to 2.6GHz is expected from simulation. A 490MHz reconfiguration between 1.87GHz (f_{low}) to 2.36GHz (f_{high}) is measured (Fig. 21.1.3). Measured insertion loss as low as 7dB was achieved in this fully integrated passive LC filter. Although, off-chip ceramic, dielectric, or LC filters tend to have insertion loss in the 1.5 to 6dB range, with Qs exceeding 30 (fractional bandwidths less than 3%), they are not tunable. The highest frequency tuning range obtained on the RF MEMS LC filters so far is 850MHz (2.6GHz to 3.45GHz). Such wide tuning range filters are likely to become critical components for applications such as cognitive radio.

The variable MEMS capacitors use interdigitated beams to form sidewall parallel-plate electrodes. One set of beam electrodes moves laterally under electrothermal microactuation. The actuators with 40×200μm^2 layout area exhibit 25μm stroke with 127Hz maximum switching frequency using 7.5mW heater power. The advance in actuation area efficiency compared to electrostatic approaches is designed by offsetting the metal lines and vias within the actuation beams. Upon heating, the beams move due to the difference in temperature coefficient of expansion of the offset metal lines versus the surrounding dielectric. Although heater power is needed when switching, zero power is required to hold the capacitor through use of a friction clutch mechanism. The clutch is normally engaged by exploiting self-assembly from the lateral residual stress gradient designed into the actuator beams and is disengaged through electrothermal control. Further scaling of the CMOS interconnects will enable taller structures for larger capacitance per area, narrower actuation beams to increase both actuation efficiency and switching speed.

The differential cross-coupled oscillator (Fig. 21.1.4) uses SiGe BJTs to cancel the losses in a LC tank consisting of a 6.25nH symmetrical MEMS inductor and MEMS capacitors that switch between 0.18pF and 1pF [5]. Parasitic interconnect capacitance from 8μm-wide 400μm-long metal-4 interconnect between the L and each C is considered when selecting tank capacitance values. Emitter follower output buffers interface the differential tank to 50Ω GSG pads. Total area is 0.87mm^2. The measured phase noise is –122dBc/Hz at 1MHz offset from the 2.8GHz carrier at a core current of 1.1mA from a 2.5V supply (Fig. 21.1.5) leading to a figure of merit of 187dB. This VCO required 5x less power than other comparable VCOs in the literature due to the loss reduction in the integrated MEMS LC tank.

MEMS mixer filters exploit the V^2 nonlinearity of the electrostatic force. Mixing and IF filtering can be accomplished in 0.02mm^2 area with <1mW power, driving the potential for integrated filter arrays. The initial cantilever-based design in Fig. 21.1.6 have a measured resonant frequency of 2.29MHz and Q of 1620 at 100mTorr [8]. Manufacturing-variation-induced measured resonance difference is 0.5% between beams spaced 100μm apart, and is matched by DC electrostatic tuning. The square geometry at the head of the cantilever reduces feedthrough by distancing the RF and IF electrodes. Application of RF to the stationary electrode and LO to the cantilever generates an electrostatic force proportional to $(V_{RF} - V_{LO})^2$ that acts on the moving cantilever. The $V_{RF} \times V_{LO}$ force component has a frequency of $(f_{RF} - f_{LO})$. Vibration within the mechanical resonance of the canteliver is amplified by the mechanical Q and read out capacitively through the IF electrode. Successful mixing with these resonators has been observed up to 3.2GHz input frequencies and is currently limited by test-bed losses.

In this paper, multiple MEMS devices within each circuit is demonstrated, but further characterization on yield and reliability is warranted. Low-cost packaging remains a challenge, with wafer-level capping possibly required for high-volume applications.

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References:
[1] *International Technology Roadmap for Semiconductors*, public.itrs.net, 2003.
[2] C. T.-C. Nguyen, "Vibrating RF MEMS for Next Generation Wireless Applications," *CICC* , pp. 257-64, Oct., 2004.
[3] N. Hoivik et al, "RF MEMS Switches Using Copper-based CMOS Interconnect Manufacturing Technology," *Sens., Act., and Microsys. Workshop,* pp. 93-94, 2004.
[4] G. K. Fedder et al, "Laminated High-Aspect-Ratio Microstructures In A Conventional CMOS Process," *Sens. & Act. A*, pp. 103-110, March, 1997.
[5] D. Ramachandran et al, "MEMS-Enabled Reconfigurable VCO and RF Filter," *RFIC Symp.,* pp. 251-254, June, 2004.
[6] H. Lakdawala et al., "Micromachined High-Q Inductors in 0.18μm Cu Interconnect Low-K CMOS," *IEEE J. Solid-State Circuits,* vol. 37, no. 3, pp. 394-403, Mar., 2004.
[7] A. Oz et al., "CMOS-Compatible RF-MEMS Tunable Capacitors," *RFIC Symp.*, pp. 611-614, June, 2003.
[8] F. Chen et al., "CMOS-MEMS Resonant RF Mixer-Filters," *IEEE MEMS,* 2005.

 0-7803-8904-2/05/$20.00

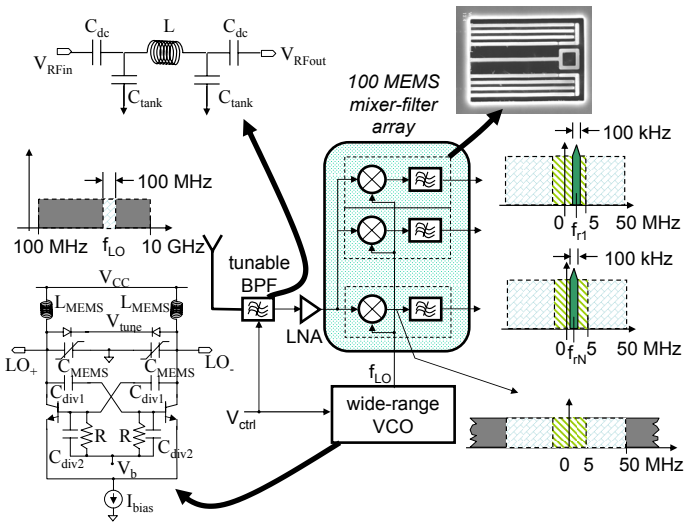

Figure 21.1.1: RF MEMS enhanced dual-hop wideband receiver.

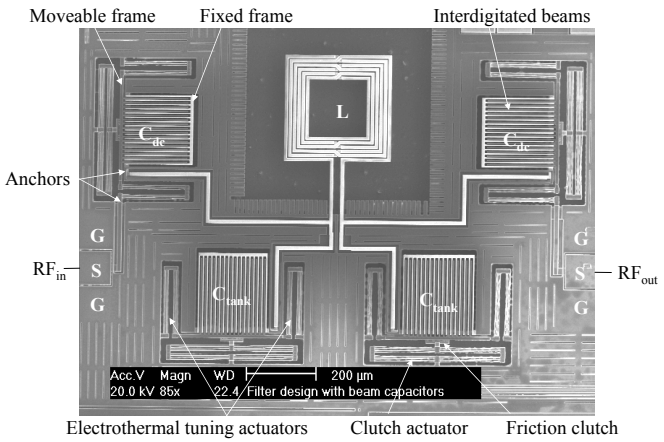

Figure 21.1.2: RF MEMS filter in the Jazz SiGe60 4-metal BiCMOS process. C_{dc} and C_{tank} switch from 550fF to 250fF and 800fF to 300fF, respectively.

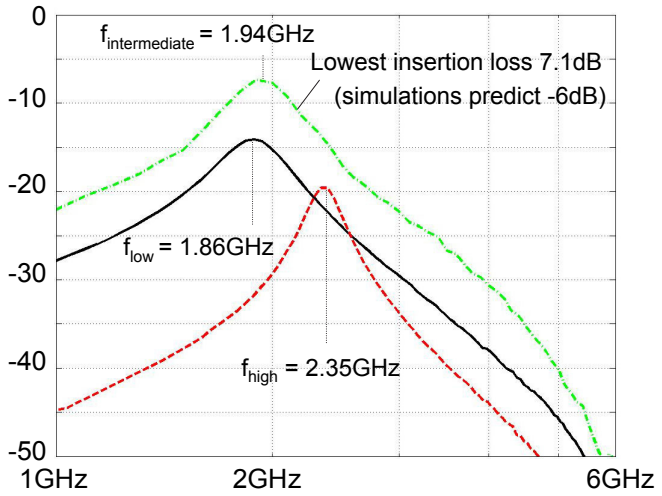

Figure 21.1.3: Measured transmission gain of RF MEMS filter.

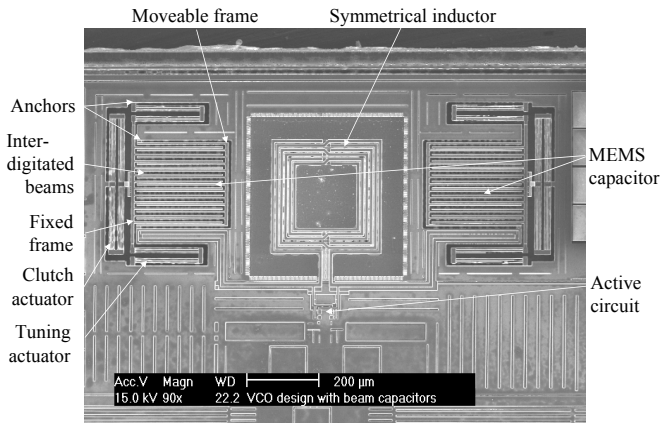

Figure 21.1.4: RF MEMS VCO in the Jazz SiGe60 4-metal BiCMOS process.

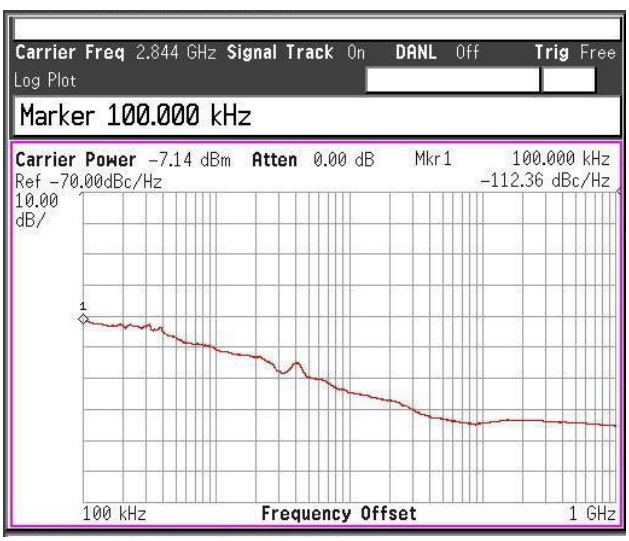

Figure 21.1.5: Phase noise spectrum of RF MEMS VCO.

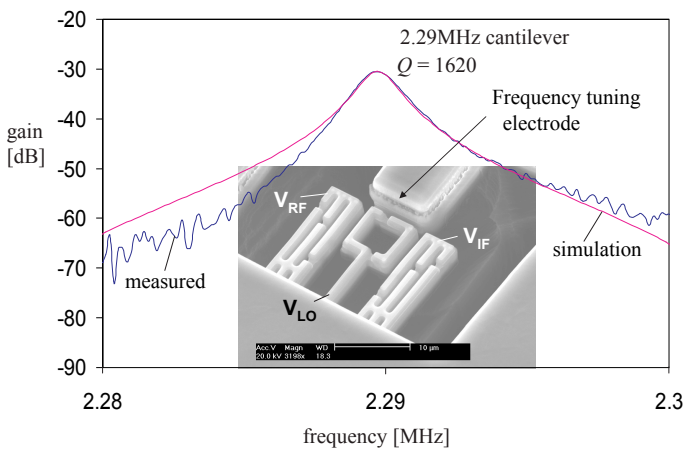

Figure 21.1.6: RF MEMS mixer filter in the Jazz SiGe60 4-metal BiCMOS process. Measured Q is a tuning parameter in the simulation.

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