26.2 A Low-Noise Low-Offset Chopper-Stabilized Capacitive-Readout Amplifier for CMOS MEMS Accelerometers

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A CMOS continuous-time chopper-stabilized amplifier reads out signals by sensing capacitance changes associated with the motion of on-chip MEMS structures. This design is applied to an accelerometer fabricated using a CMOS MEMS process [1]. The amplifier design uses transistor sizing based on capacitance matching between circuit and sensor to minimize sensor noise floor, making it possible to resolve the smallest possible motion from MEMS structures. It also establishes robust DC biasing at input sensing nodes by periodic reset and provides DC offset cancellation to prevent amplified DC offsets from saturating the amplifier outputs. Finally, because manufacturing mismatches can result in large position offsets, the amplifier design includes AC sensor offset cancellation. For example, the position offset in the prototype accelerometer, without AC offset cancellation, is sufficient to entirely swamp the operation of the amplifier.

The surface micromachined accelerometer prototype has particularly low sensing capacitance ~20fF and low sensitivity <1mV/g, making electronic noise dominant. In a CMOS interface circuit, the noise sources include MOSFET 1/f noise, thermal noise, and shot noise of bias leakage current. The noise floor of the accelerometer is given by:

$$\overline{a_n^2} = \frac{2kT\omega_r^4 x_0^2 (2C_s+C_p+C_g)^2}{3C_s^2 V_m^2 \sqrt{2\mu_n C_{ox} I_D (W/L)}} + \frac{\omega_r^4 x_0^2 (2C_s+C_p+C_g)^2}{8C_s^2 V_m^2 \mu_n C_{ox}^2 WLf} + \frac{\omega_r^4 x_0^2 q I_{leak}}{8C_s^2 V_m^2 f^2} \quad (1)$$

Sizing up the MOSFETs does not improve the signal-to-noise ratio (SNR) because it also reduces the sensitivity due to larger gate capacitance (C_g). The SNR is optimized by capacitance matching, which results in MOSFET width of 50μm to 100μm for a 0.5μm length.

There are three other major nonidealities: undesirable charging activity; circuit offset; and sensor offset. In continuous-time voltage readout, the sensing nodes have high impedance and are sensitive to charging. Due to low sensitivity, the circuit offset and the sensor offset caused by manufacturing mismatch are both large compared to the signal, equivalent to 100-1000g of acceleration. All of these nonidealities must be controlled for the device to function properly.

The architecture of the fully-differential chopper-stabilized amplifier is shown in Figure 26.2.1. Simulation shows that continuous-time voltage readout offers better noise performance over switched-capacitor circuit by avoiding noise folding [2,3]. Therefore, chopper stabilization is used to modulate signal to a high frequency to suppress offset and low-frequency noise in a continuous-time mode [4]. The DC bias voltages of input sensing nodes are established by resetting them to a DC voltage source every 16 clock cycles. By releasing charge periodically, the effect of undesirable charging is minimized. A two-stage wide-band differential difference amplifier (DDA) provides gain of 40-50dB in a 3MHz bandwidth. The input stage is optimized for noise and the second stage provides main amplification and offset cancellation. The circuit DC offset is cancelled by DC feedback employing a narrow-band offset amplifier and a large off-chip capacitor. The electronic compensation of sensor offset is realized by sending an AC correction signal into another DDA input. A passive mixer is used to demodulate the signal.

Figure 26.2.2 shows the generation of modulation and biasing signals. Square-wave modulation is used. They are generated on-chip with a single digital clock. To prevent charge injection error, the modulation is disabled during the bias reset, and the reset is turned off before the modulation is turned on again. Large CMOS transmission gates are used as the switches. Low-leakage pMOS diodes are used as the bias reset switches because in an n-well process the well is biased at the source potential.

The two-stage wide-band DDA is shown in Figure 26.2.3. The input stage has gain of 3.3 to attenuate the noise from following circuits. The input MOSFETs are sized to achieve optimum capacitance matching with the sensor to maximize the SNR. The load devices have 2x minimum channel length to minimize their 1/f noise contribution. The main input transistors of the second stage are large so their noise contribution is negligible. The two auxiliary compensation input ports use smaller transistors to minimize their noise contribution. A large portion of total current is supplied to the output stage to obtain high 3dB bandwidth. A common-mode feedback amplifier is used to stabilize the output common-mode voltage. And, a narrow-band offset amplifier is used for DC feedback. All current sources use cascode current mirrors to improve common-mode and power-supply noise rejection.

A prototype chip is fabricated in a 0.5μm CMOS process and the transducers are released by SiO_2/Si dry etching (Figure 26.2.4) [1]. In the test setup, the differential output signal is converted to single-end by an off-chip instrumentation amplifier with gain of 25. Figure 26.2.5 shows the system response to 0.5g 400Hz acceleration and the pre-demodulation differential signals. Figure 26.2.6 shows the accelerometer output spectrum with -9dBg input. The circuit input-referred noise floor is <40nV/√Hz, and the sensor noise floor is 50μg/√Hz. With the DC feedback, the offset amplifier output is 0.1V, which translates to input-referred offset ~10μV. The electronic offset compensation achieves >40dB sensor offset reduction. It has much larger compensation range than mechanical tuning and avoids the high voltage required by an electrostatic actuator.

The measured noise floor versus modulation frequency is plotted in Figure 26.2.7. This measurement proves that the noise decreases with modulation frequency and the 1/f noise dominates in a wide frequency range because the input transistors must be small to match the fF-range sensing capacitance. Beyond 2MHz, the input-referred noise goes up due to bandwidth limit. Even higher modulation frequency is needed for further reduction of electronic noise floor, which requires either faster process or higher power consumption.

Acknowledgements:
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References:

[1] G. Zhang et al., "A Lateral Capacitive CMOS Accelerometer with Structural Curl Compensation", Tech. Digest 12th IEEE Int. Conf. Micro Electro Mechanical System (MEMS '99), pp. 606-611, Orlando, FL, 1999.
[2] M. Lemkin, B.E. Boser, "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics", IEEE JSSC, vol. 34, no. 4, pp. 456-468, April, 1999.
[3] N. Yazdi, K. Najafi, "An interface IC for A Capacitive Silicon ug Accelerometer", ISSCC Digest of Technical Papers, pp. 132-133, Feb., 1999.
[4] C.C. Enz, G.C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", Proc. of the IEEE, vol. 84, no. 11, Nov., 1996.

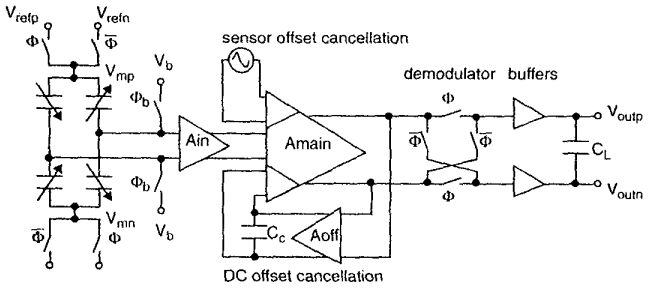

Figure 26.2.1: Architecture block diagram.

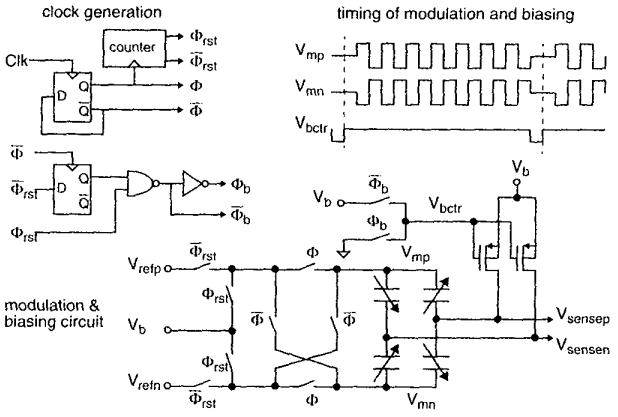

Figure 26.2.2: Modulation and input biasing.

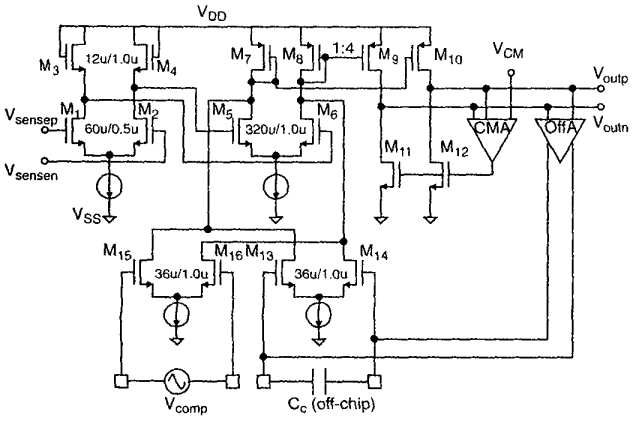

Figure 26.2.3: Schematic of the 2-stage 3-input DDA.

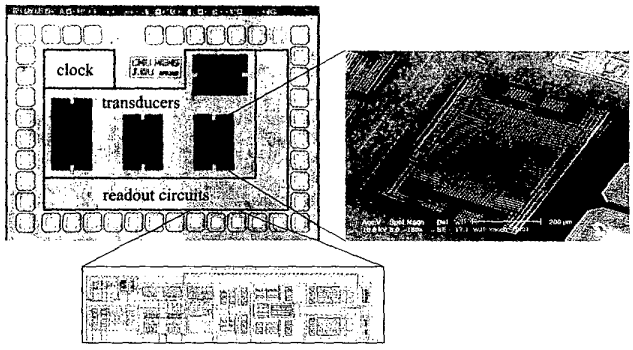

Figure 26.2.4: Chip micrograph, SEM of released transducer and circuit layout.

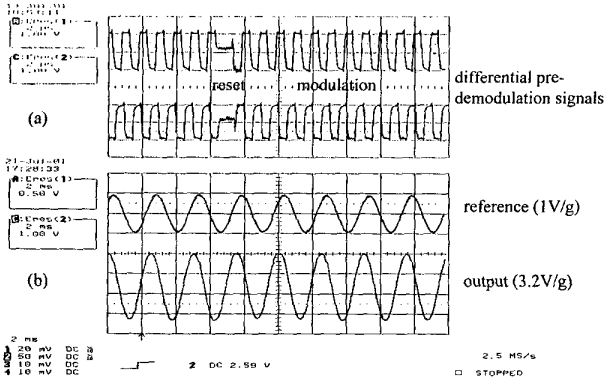

Figure 26.2.5: Measured waveforms of: (a) pre-demodulation signals; (b) output signal in response to 0.5g 400Hz acceleration.

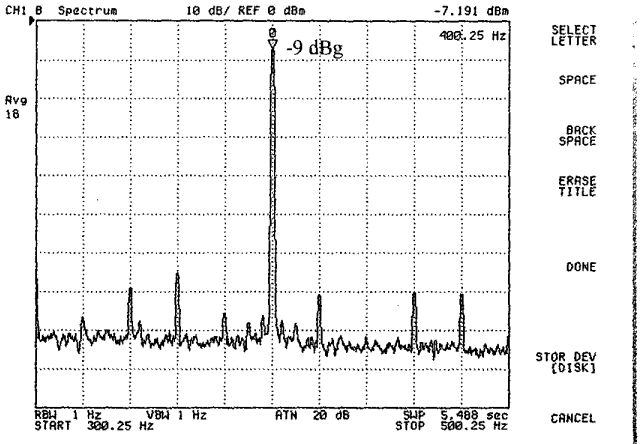

Figure 26.2.6: Measured output spectrum in response to -9dBg 400Hz acceleration.

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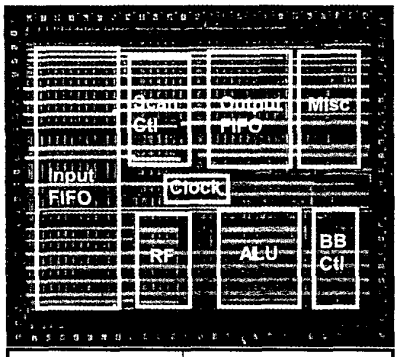


Die Size	1.61 x 1.44mm²
Process	130nm CMOS
Interconnect	1 poly, 6 metal
Transistors	160k
Maximum V_{CC}	1.5V

Figure 25.2.7: Die characteristics.

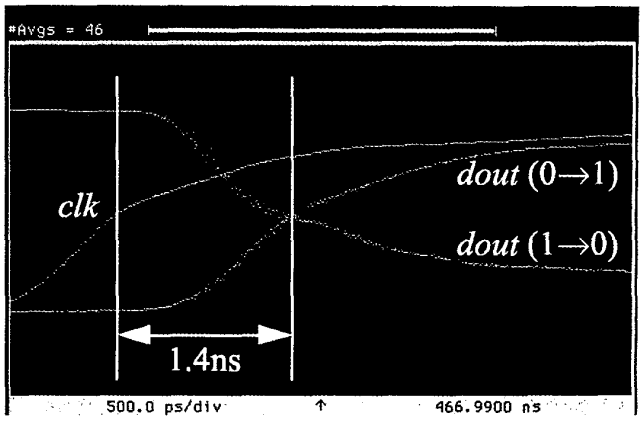


Figure 25.4.7: Oscilloscope waveform showing access time.

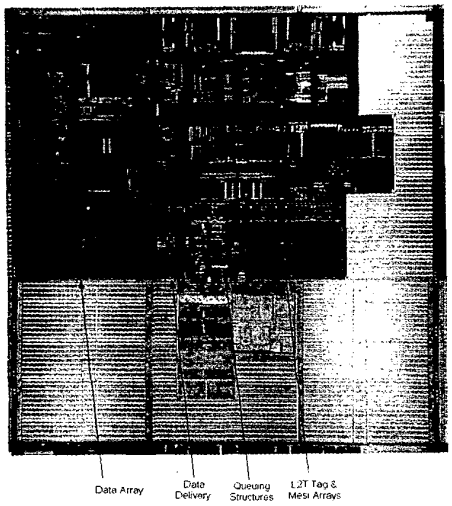


Figure 25.5.6: Die micrograph.

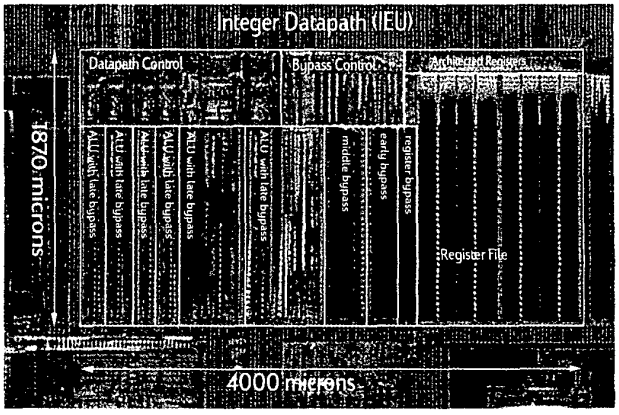
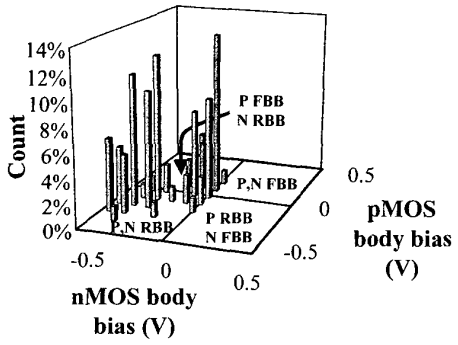


Figure 25.6.7: Die micrograph.



Bias resolution	Die-to-die ABB		Within-die ABB	
	dies, F > 1	σ/μ	dies, F > 1.075	σ/μ
0.5	79 %	2.87 %	2 %	1.89 %
0.3	100 %	1.47 %	66 %	0.50 %
0.1	100 %	0.58 %	97 %	0.25 %

Figure 25.7.7: (a) Histogram of applied bias voltage. (b) Impact of bias resolution on ABB effectiveness.

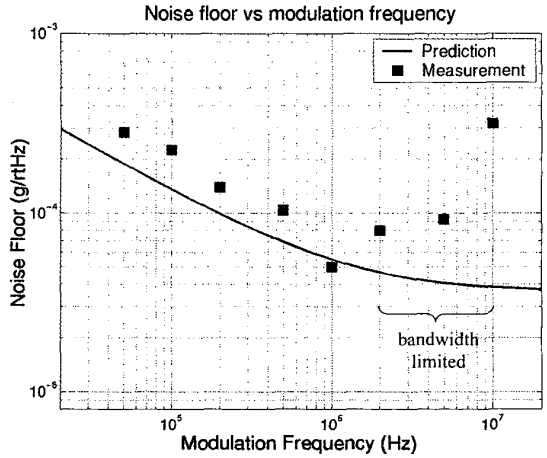


Figure 26.2.7: Measured and predicted noise floor versus modulation frequency.