Integrated RF Microsystems with CMOS-MEMS Components

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ABSTRACT

Future on-chip low-IF-conversion receiver architectures will benefit from advances in CMOS-MEMS capacitors and mixer-filter components. Single-chip reconfigurable LC filters and VCOs employ multiple MEMS capacitors working in concert. Resonant mixer-filters with 0 dB insertion loss and sub-mW power are achievable through formation of self-assembling gaps in the post-CMOS micromachining technology.

1. INTRODUCTION

The enormous cellular phone market, along with emerging wireless markets in modular USB port plug-ins, RF identification tags and sensor networks continue to motivate research to place ultra-low power RF transceivers completely on chip. Within our group, the wideband receiver front-end architecture in Figure 1 has been a primary system target driving RF CMOS MEMS device and circuit development. The reconfigurable bandpass filter is meant to switch between bands and be synchronized to the wide-range voltage controlled oscillator (VCO), which produces the local oscillator (LO). MEMS switches can be used for such modules. As an alternative, we are exploring use of reconfigurable MEMS capacitors (essentially capacitive switches) to implement filter and VCO blocks that currently switch center frequency by up to 800 MHz, but have potential for even larger range. These devices are made entirely in foundry CMOS and BiCMOS, and so can be readily transferred for commercial use.

The architecture in Figure 1 incorporates an array of MEMS resonant mixer-filters. Electromechanical mixing of RF and LO inputs and narrow-band filtering is performed in a single passive device. The filter center frequency is set by the micromechanical resonance and, for our recent research, is kept between 1 MHz to 10 MHz to exploit the relatively large motions attained through mechanical bending modes (when compared to motion from bulk or shear modes). An analog preamplifier is required to detect the motional displacement current of each resonator. The resulting MHz IF signal then can be converted to digital form. The potential advantage of using MEMS mixer-filters is their small footprint and low power, enabling an arrayed architecture, where the channel selection is performed by selecting between device outputs rather than having a tunable filter. An alternative, but similar, architecture employs a single electronic mixer feeding a bank of MEMS filters.

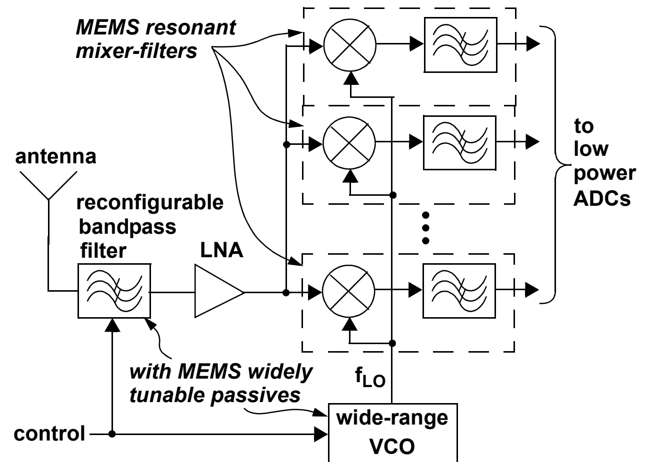


Figure 1. Wideband receiver front-end architecture driving RF CMOS MEMS research on devices and circuit modules.

This paper provides an overview of the research to date on CMOS RF MEMS devices and circuit modules. The discussion will cover the process flow and specific issues in achieving small gaps, the reconfigurable capacitor design and lateral electrothermal actuation, use of multiple MEMS capacitors in a filter and VCO, work on verifying CMOS-MEMS mixer-filter performance along with recent results to obtain sub-0.5 μm gaps, and some thoughts on future research exploiting this technology.

2. CMOS MEMS FABRICATION

The CMOS MEMS process developed at Carnegie Mellon [1] is illustrated in Figure 2, starting with a four metal CMOS chip shown in cross-section in (a). Most of the RF MEMS passives and circuit modules are made in the Jazz Semiconductor SiGe60 process, which supports 4-metal layers, 0.35 μm CMOS and SiGe bipolar transistors. The structures are micromachined after the foundry process is completed through a sequence of dry etch steps. The first post-CMOS micromachining step, shown in (b), is a CHF_3:O_2 reactive-ion etch (RIE) of the inter-metal dielectric stack [2]. The RIE etches any dielectric that is not covered with metal. The RIE is slowed by the first metal layer encountered and thus acts as the mask that defines the microstructural sidewalls. The top-most metal layer placed

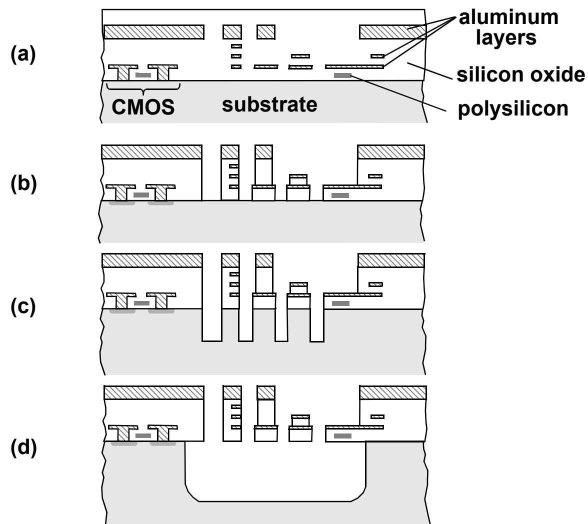


Figure 2. CMOS MEMS process. (a) Foundry 4-metal CMOS. (b) Oxide RIE. (c) Silicon DRIE. (d) Isotropic silicon etch.

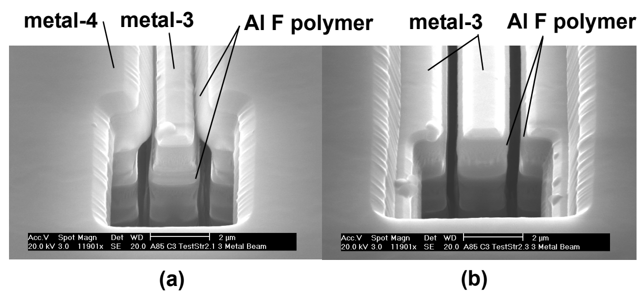
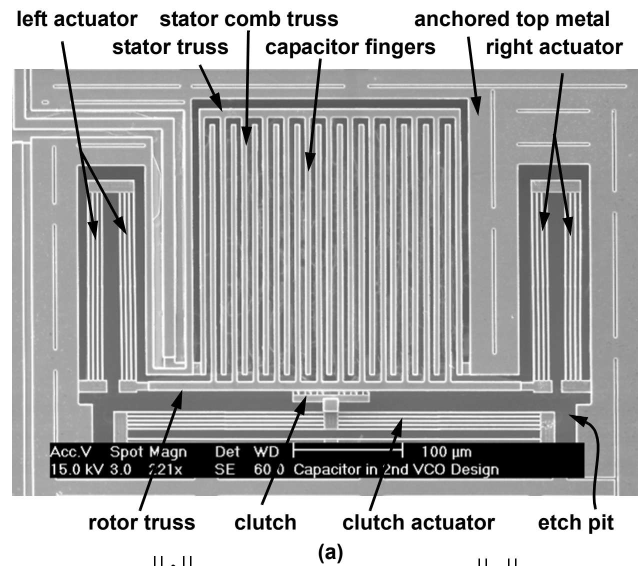


Figure 3. Test structures for assessing the design rules for gap etch. (a) Metal-4 layed out with its sidewall in line with metal 3, demonstrating metal-4 bloat and excessive polymerization. (b) Metal-4 layed out with 2 µm cut-in from metal-3 edge. The gap widths are 0.25 µm on the left side and 0.35 µm on the right side. After [10].

in a structure sets its thickness. The second post-CMOS micromachining step, shown in (c), is a timed directional etch of the exposed silicon substrate using the deep-RIE process. This step sets the spacing from the microstructures to the substrate. The final step is a timed isotropic silicon etch in an SF_6 plasma to undercut and release the structures as shown in (d) [3].

The minimum allowable gap is constrained by sidewall polymer buildup and by aspect-ratio dependent retardation of the etch. An aluminum fluoride polymer deposition of up to 0.2 µm occurs locally on sidewalls during the plasma oxide etch. Exposed aluminum from the chip is incorporated into the plasma. Micromechanical sidewalls and gaps formed with the top 2 µm-thick aluminum layer (metal-4) are particularly affected. An excessive amount of polymer is present on these sidewalls, as shown in Figure 3(a). The metal-4 layer also experiences a bloat of around 0.1 µm with respect to layout. A design solution to enable very narrow gaps is to enforce a cut-in of metal-4 with respect to



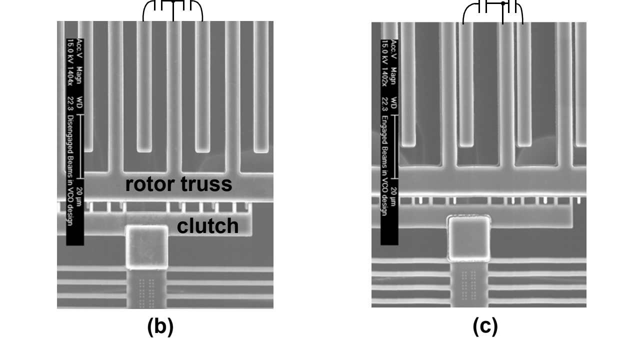


Figure 4. (a) Tunable capacitor in the Jazz SiGe60 process. (b) Rotor fingers latched into a low-capacitance state (400 fF), midway between stator fingers. (c) Rotor fingers latched in high-capacitance state (866 fF), mechanically contacting stator fingers. After [9].

the lower metal layers. For example, the test structure in Figure 3(b) has a metal-4 cut-in from metal-3 of 2 µm. Polymerization on the gap sidewalls is small enough to allow around 300 nm mechanical gaps to be formed. However, a penalty is paid as about 3.5 µm of electrode height is sacrificed by recessing the metal-4. Using a process solution, the sidewall polymer can be greatly reduced by masking the aluminum in the non-MEMS areas with photoresist.

3. TUNABLE CAPACITORS

Micromachined capacitors are able to provide larger capacitance ratios than varactor diodes and can achieve higher quality factor for applications above 5-10 GHz. Since there is only a single micromechanical layer available in CMOS MEMS, vertical parallel-plate capacitors are not possible without additional material depositions and micromachining above the CMOS.

Several topologies of laterally actuated CMOS-MEMS tunable capacitors have been designed, fabricated and

tested [4][5]. The capacitor topology shown in Figure 4(a) is the most robust topology to date [9]. The capacitor is made of 25 interdigitated comb fingers that form parallel-plate sidewall electrodes. The stator fingers are suspended from a micromachined frame that compensates for any out-of-plane curl that occurs along the finger trusses. The rotor fingers are connected to two folded-flexure electrothermal actuators located to the far right and left of the device. Heating the actuators moves the rotor fingers to the left into contact with the stator fingers, as shown in Figure 4(c). A lower temperature centers the comb fingers to produce the low-capacitance state, as shown in Figure 4(b).

The maximum capacitance is limited by the sidewall polymerization. The quality factor for these capacitors is around 20 up to 2.7 GHz, limited by series resistance. The RF signal must be routed through the actuator beams, whose interconnect resistance is the limiting factor.

A separate actuator is placed adjacent to the rotor truss to operate a clutch mechanism. When heated, the clutch actuator retracts from the rotor allowing it to move. Once the rotor is moved into the desired position, the clutch actuator is powered off and clamps onto the rotor due to a self-assembly displacement. Once latched, the rotor actuators may be powered off with the capacitor remaining in its desired position. This clutch sequencing provides capability to fix capacitance within a range with no continuous power.

4. ELECTROTHERMAL ACTUATION

The CMOS electrothermal microactuators can operate at low voltages, are area efficient, and can have very stiff suspensions to reduce acoustic vibrations in RF MEMS passives. The design concept for lateral electrothermal actuation is illustrated in Figure 5. The lower metal layers in the beams are offset with respect to the top metal layer of the beams [6]. The residual stress difference between the silicon oxide and the aluminum (Figure 5(b)) gives rise to a lateral displacement upon microstructural release (Figure 5(c)). By designing the metal offset to switch sides halfway down the beam length, the displacement mimics that of a guided-end beam. Upon heating, usually by passing current through an embedded polysilicon heater resistor, the aluminum expands about 20 times more than the silicon oxide and creates a bending moment opposite from the self-assembly direction (Figure 5(d) and (e)).

Electrothermal actuation of the folded-flexure actuators such as used in Figure 4, move up to 25 µm with under 10 mW of heating. The actuator can be designed to self-assemble and actuate in either direction, dependent on the ordering of the metal offset within the actuation beams.

The guided-end motion enables an arbitrary number of beams to be placed in parallel to achieve high stiffness in the actuation direction without lowering the displacement capability. For example, the folded-flexure actuators in Figure 4(a) have four parallel beams per actuator segment.

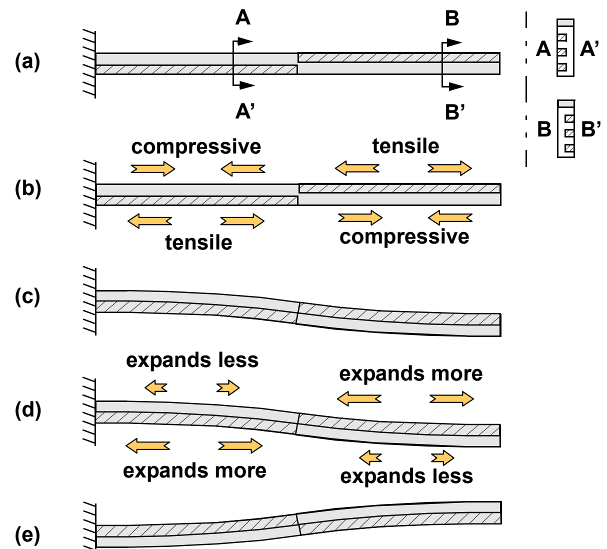


Figure 5. CMOS-MEMS lateral electrothermal actuator. (a) Cantilever in layout, illustrating embedded metal offset inside beam. (b) Residual stress distribution before release. (c) Displacement after release. (d) Strain distribution after heating. (e) Displacement after heating.

5. FILTER and VCO MODULES

The bandpass filter topology in Figure 6(a) and (b) incorporates four MEMS capacitors and a MEMS inductor with silicon undercut to improve Q [7]. The maximum shift in center frequency was from 1.87 GHz to 2.36 GHz. The change in Q and amplitude is partly due to the ganged design of the capacitor control. A minimum insertion loss of 7.1 dB at 1.95 GHz stems from the optimum ratio of the dc blocking and tank capacitors.

A wide-range voltage-controlled oscillator was implemented by using two MEMS capacitors for reconfiguration between 180 fF and 1 pF in parallel with varactor diodes for local tuning [8]. The phase noise was -122 dBc/Hz at a 1 MHz offset from the carrier. Power was 5 mW at 2.07 GHz and 2.75 mW at 2.84 GHz. This is the lowest power in a wide-range reconfigurable VCO at these frequencies.

6. RESONANT MIXER FILTERS

The dual cantilever resonant mixer-filter shown in Figure 8 was our first CMOS-MEMS topology to demonstrate the mixing function [10]. A differential signal was produced by setting a positive bias (+12.5 V) on one resonator and a negative bias (–6.5 V) on the other. These particular bias values tuned the resonators to achieve the single-peak output at the 435 KHz resonance. The Q limits at 1400 for pressure below 1 T. The mixer-filter response, shown in Figure 8(c), remains unchanged for LO and RF frequencies

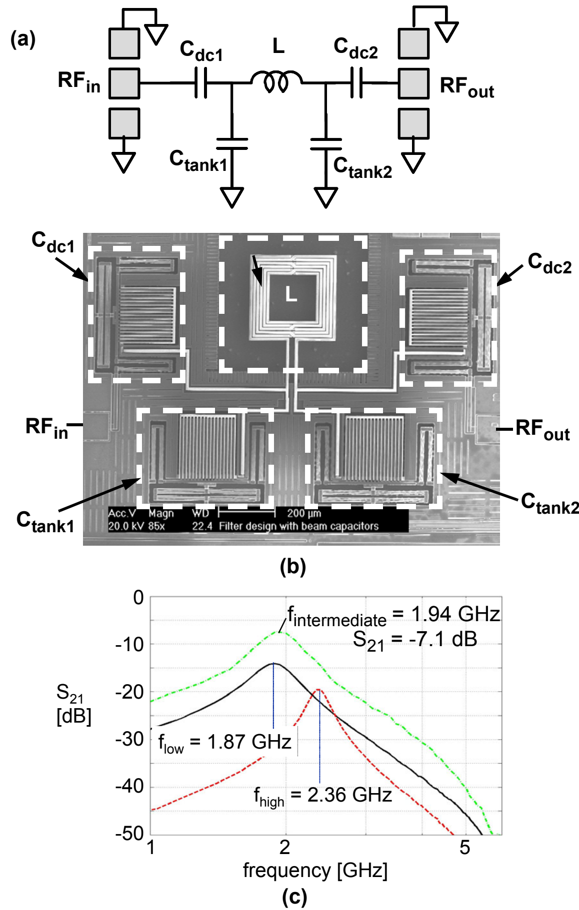


Figure 6. Reconfigurable bandpass filter. (a) Schematic, (b) SEM, (c) S_{21} measurements. After [7], [9].

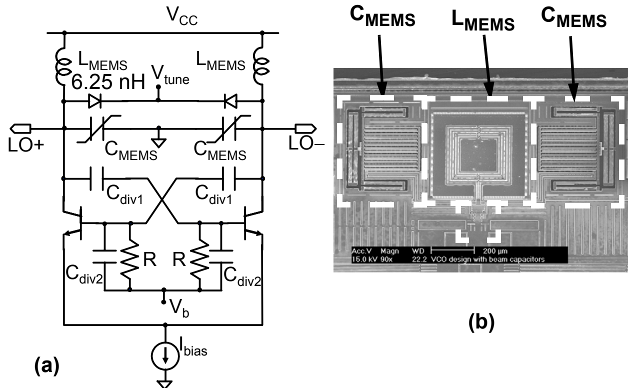


Figure 7. Wide range voltage controlled oscillator. (a) Schematic, (b) SEM. After [8], [9].

from 10 MHz to 400 MHz. Significant feedthrough exists in mixing measurements performed from 800 MHz to 3.2 GHz. The feedthrough sources were extracted from simulation and are reduced by eliminating on-chip capacitive coupling from the LO and RF to the bias current line and directly to the preamp inputs.

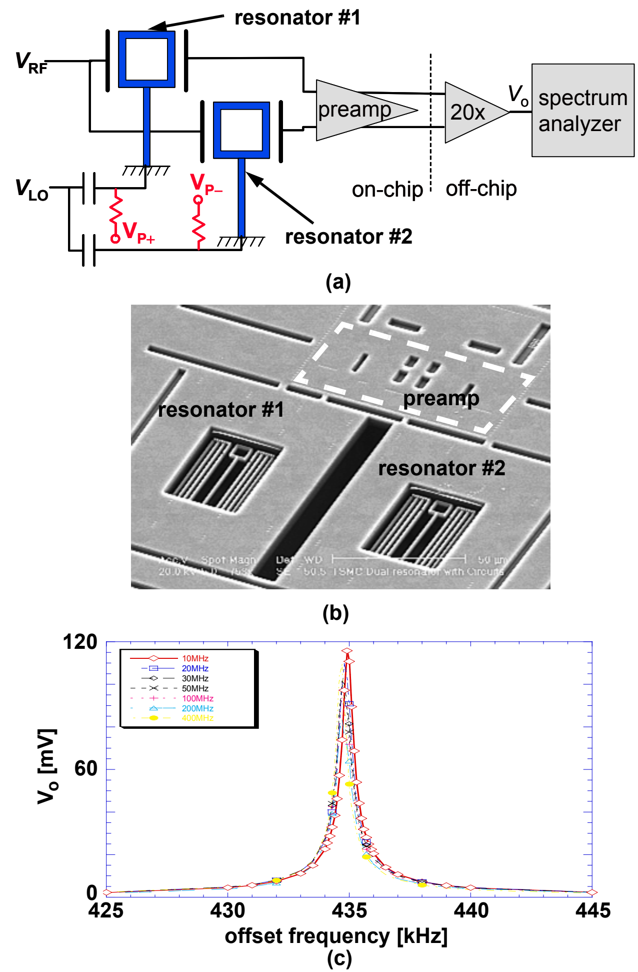
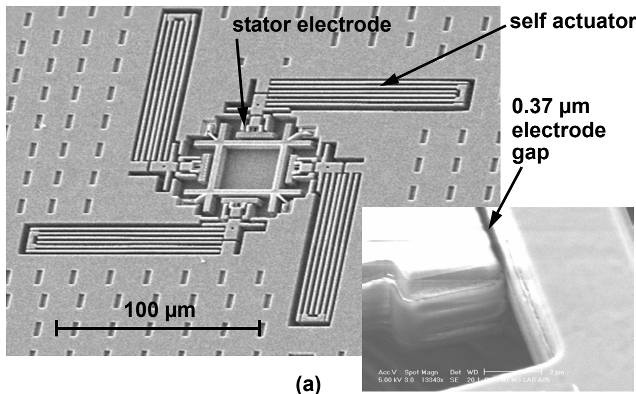
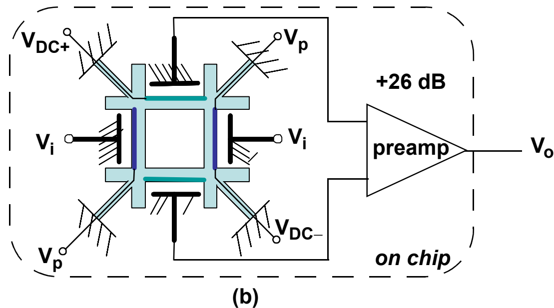


Figure 8. Dual cantilever resonator mixer-filter. (a) Schematic, (b) SEM, (c) mixer output measurement with pressure of 1 T, $|V_{LO}| = |V_{RF}| = 1$ V. After [10].

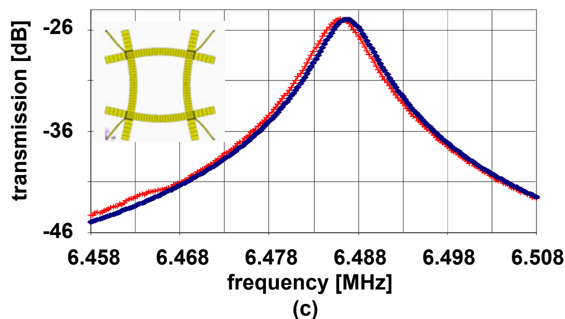
The insertion gain scales as $(\text{gap})^4$, so there is motivation to reduce further the 1.3 µm gap of the device in Figure 8. One approach is the self-assembly of smaller gaps as exemplified in the square-frame resonator (SFR) in Figure 9, which has a inherent differential input and output [11]. Upon microstructural release, the self-assembly actuators engage with a limit stop intended to set the gap 0.3 µm. Gaps on other structures have been set to as low as 100 nm, but not yet tested. The insertion loss (V_o/V_i) of the SFR, operating in the primary bending mode at 6.486 MHz, is –24.95 dB with a Q of 786. To fit simulation to experiment, the electrical gap is found to be 0.64 µm, which is larger than the mechanical gap due to the polymerization on the sidewalls. The measured insertion loss is improved by 10 times over a fixed electrode version with mechanical gap of 0.68 µm.



(a)



(b)



(c)

Figure 9. (a) Square frame resonator with self-assembled gaps. (b) Block diagram. (c) Measured and simulated resonance peak after feedthrough subtraction. P = 40 mT, V_i = 0 dBm, V_p = 6V, V_{DC+} = 20 V, V_{DC-} = 17.4 V. After [11].

7. CONCLUSION

Integrated MEMS RF passives enable low power reconfigurability from 100's of MHz to GHz. There are perhaps greater opportunities for such MEMS passives at frequencies above 5 GHz, where varactor diodes have greater loss and MEMS capacitors and waveguides provide potential solutions. For the CMOS-MEMS capacitors shown here, future refinements include addition of metal to raise Q, minimization of sidewall polymer to increase range, and reduction of electrothermal actuation power.

The MEMS mixer-filters provide a path toward multiple bandpass filters on a single chip, since the frequencies are set by lateral design features. Improvement of the overall resonant filter gain must include the design trade-off of increasing electronic gain while keeping small the capacitive loading that lowers the capacitive bridge gain. A goal of 0 dB insertion loss is expected to be reached with a combination of gap reduction to 100 nm, optimally sizing the preamp for maximum system gain, and arraying of matched resonators to boost signal. Arraying with active tuning is the expected path to achieve appropriate bandpass filter characteristics for channel selection. The elimination of feedthrough at RF frequencies from direct capacitive coupling and ancillary micromechanical modes is another significant design challenge.

8. ACKNOWLEDGEMENTS

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