Modeling and Design of An RF-MEMS Reconfigurable LC-based Bandpass Filter

by

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A thesis submitted in partial fulfillment of the requirements
for the
degree of

Master of Science

August 2005

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Abstract

CMOS-MEMS tunable capacitors, micromachined inductors and wiring interconnects fabricated in Jazz 0.35 μm BiCMOS and ST Microelectronics 0.25 μm processes have been modeled. These models were verified by comparing the simulation and measurement results of first and second generation RF-MEMS reconfigurable LC-based bandpass filters. The modeled and extracted model parameters matched well.

Third generation RF-MEMS reconfigurable LC-based bandpass filter with CMOS-MEMS tunable capacitors, micromachined inductors and wiring interconnect models is designed for covering the lowest three frequency bands of Ultra-Wide Band (UWB) with an insertion loss lower than 4 dB. The filter is fabricated in ST Microelectronics 0.25 μm process and post-processed in Carnegie Mellon University.

Acknowledgement

I would like to thank the people who have deserved to be mentioned for supporting me and contributing to this work I have been studying on for two years in Carnegie Mellon University. First of all, I would like to thank my advisor, Prof. Tamal Mukherjee, for teaching me how to do research, for his meticulous thinking and guidance, and for his friendship. He always tried to give the best advice and help me as soon as I needed. He also reviewed this thesis and led to significant improvement. Within two years of this work, Prof. Gary K. Fedder have been giving painstaking, creative advice, letting MEMS Lab be extremely comfortable working environment. I would also like to thank him for taking some time to read this thesis and give constructive feedback in his busy schedule.

Four of my colleagues and friends -Umut Arslan, Abhishek Jajoo, Ryan Magargle and Peter Gilgunn- deserve to be mentioned separately for their help and advice for both my research and social life. I also would like to acknowledge Gokce Keskin, Altug Oz, Amy Wung, Sarah Bedair, Fernando Alfaro, Fang Chen and Anna Liao for being available whenever I need discussion about my research.

I am grateful to Mary L. Moore, Dan Marks, Elaine Lawrence and Lynn Philibin for being very helpful in ensuring that any administrative issues related my graduate study in Carnegie Mellon University have been a wonderful experience.

I would like to thank my parents and my twin brother for making me feel their love every second even though they are overseas. Lastly, I would also like to thank my family in Pittsburgh- Oznur, Tankut, Volkan, Pinar, Mehmet and Tugba- for showing their love, encouragement and moral support for two years.

This work was funded in part by C2S2, the MARCO Focus Center for Circuit & System Solutions, under MARCO contract 2003-CT-888 as well as ITRI Labs in CMU.

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1 Introduction

The increase in the number of wireless standards, has boosted the desire for the development of reconfigurable transceiver architectures. The demand for realization of the wireless services, in which the users can switch between multi-standards using the same device, makes the development of reconfigurable transceiver architectures necessary. In such transceiver architectures, the RF front-end circuit needs to be tuned to communicate in multiple frequency bands.

The tunability of RF front end bandselect filters plays the most important role in a reconfigurable RF front end architecture. Figure 1-1 shows the basic single down conversion stage receiver architecture. In this specific architecture, the RF front end filter eliminates the interferers outside the band preventing desensitization of the desired signal from intermodulated signals generated due to nonlinearity of the LNA [1]. In narrowband communications systems such as those using the classic superheterodyne receiver, bandpass filters with fractional bandwidths on the order of 1% (Q of 100) are needed for preselection and image rejection prior to demodulation. In wideband communications systems, the fractional bandwidths are much higher, however, the need for band pre-filtering still remains. For reconfigurable architectures, two solutions are possible for the pre-select filter. One involves switching between a number of fixed filters each set to pass a different frequency band. The second involves hardware sharing a single reconfigurable RF filter.

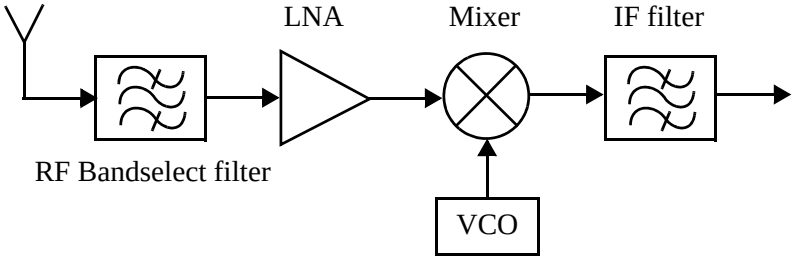


Figure 1-1 The basic single down conversion stage receiver architecture

Although most radio standards have specifications based on the capabilities of off-chip LC, ceramic and SAW filters, these filters are neither tunable nor integrable. In order to create reconfigurable receiver architectures, a number of off-chip filters need to be combined with a number of switches, which will increase the cost, size and isolation problems associated with employing off-chip filtering.

Analog on-chip RF bandpass filters can be categorized as passive filters and active filters. Active filters include RC, switched capacitor, gm-C and Q-enhanced LC filter, whereas passive filters include LC, MEMS, electroacoustic and Film Bulk Aqoustic Resonators (FBARs). Although opamp-RC filters have proved to have no bandwidth limitations, wide dynamic range and tunability, their operation frequency cannot reach to GHz [2][3]. Switched-capacitor and gm-C based on-chip filters have difficulty in achieving high operating frequencies with narrow bandwidths (high Q) [4]. Q-enhancement active filters have high quality factor, however in order to have the required dynamic range and insertion loss, they need to dissipate a high amount of power [5][6][7].

Among the passive filters, although MEMS and electroacoustic filters have high quality factors, it is difficult to implement them at high frequencies with low insertion loss [8][9]. FBARS achieve low insertion loss at high frequencies, however they are not reconfigurable [10]. The performance of on-chip passive LC filters is primarily limited by low quality factor of inductors, which leads to high insertion loss, or poor power transfer. Low inductor Q also limits the overall filter Q, limiting the ability to achieve a narrowband response. Micromachining is one technique to improve the quality factor of the on-chip inductors [11], and it simultaneously integrates on-chip MEMS varactors to enable wideband tuning of the on-chip LC filter.

In this thesis we use the Application Specific Integrated MEMS Process Service (ASIMPS) that is hosted by Carnegie Mellon University. It starts with a foundry-fabricated four-metal CMOS chip with cross-section shown in Figure 1-2 (a). MEMS structures are micromachined through a sequence of dry etch steps. First, a CHF_3:O_2 reactive-ion etch (RIE) removes any dielectric that is not covered with metal (Figure 1-2 (b)). The top metal layer is used to protect the electronic circuits that reside alongside the MEMS struc-

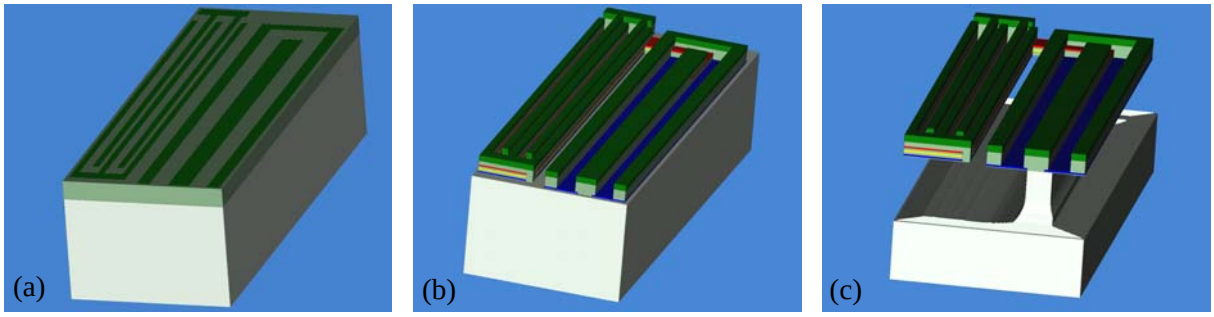


Figure 1-2 Cross-section of ASIMPS micromachining process: **(a)** After foundry CMOS processing, **(b)** after anisotropic dielectric etch, **(c)** after final release using a combination of anisotropic silicon DRIE and isotropic silicon etch.

tures. Second, an anisotropic etch of the exposed silicon substrate using the Bosch deep-reactive-ion etch (DRIE) sets the spacing from the microstructures to the substrate. A subsequent isotropic etch of silicon in an SF_6 plasma undercuts and releases the MEMS structures. The released structure is a stack of metal and oxide layers such as the beam shown in Figure 1-2 (c). The ASIMPS process enables reconfiguration over a wide range of frequency, due to mechanical movement of released MEMS structures. CMOS-MEMS capacitors fabricated via the ASIMPS process in an LC-filter achieve reconfiguration without any additional power, and cover a wider frequency range compared to CMOS varactors.

RF-MEMS LC bandpass filters can address the need for integration, tunability, low power dissipation, low noise figure, high linearity and compatible quality factor and insertion loss for reconfigurable receiver architectures. Specifications of the RF-MEMS reconfigurable front end LC-based filter are shown and described in Figure 1-3 and Table 1-1. As seen in the table, the specifications of resonant frequencies, bandwidth and insertion loss are defined for both minimum and maximum frequencies. Before the design of the filter, these specification values need to be derived from a link-budget analysis that distributes the wireless communication standard requirements across the receiver chain.

The first generation filter [12] and the second generation filters designed and fabricated with the Jazz 0.35 μm BiCMOS process have shown that several tunable CMOS-MEMS capacitors [13] can be integrated with micromachined inductors, and have demonstrated the benefits of micromachining and of RF-MEMS integration in an electronic circuit. Although, the reconfigurable characteristic in the filter perfor-

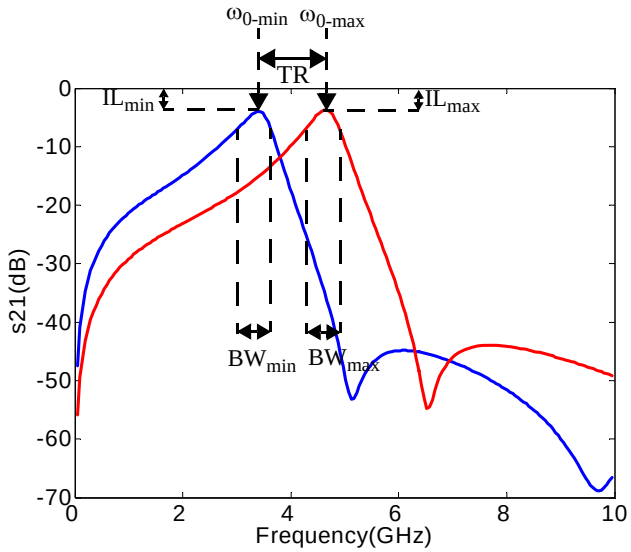


Figure 1-3 The typical response of an RF-MEMS reconfigurable bandpass filter and its specifications shown in the figure

Table 1-1. RF-MEMS Reconfigurable Filter Specifications

Specifications	**Description**
Resonant Freq. ($\omega_{0\text{-min}};\omega_{0\text{-max}}$)	minimum and maximum resonant frequencies
Tuning Range (TR)	$\omega_{0\text{-max}}$-$\omega_{0\text{-min}}$
Bandwidth (BW_{min}, BW_{max})	3-dB bandwidth of minimum and maximum resonance cases
Quality Factor (Q_{min}, Q_{max})	$Q_{min}=\omega_{0\text{-min}}/BW_{min}$ $Q_{max}=\omega_{0\text{-max}}/BW_{max}$
Insertion loss (IL_{min}, IL_{max})	loss at minimum and maximum resonant freqs.
Switching Time	time necessary to switch from minimum to maximum resonant freq.
Shape Factor	sharpness of filter response

mance has been demonstrated, due to lack of complete models for RF-MEMS capacitors, inductors and interconnects, the performance of the filter has shown poor matching with the predicted results.

This thesis presents a complete model for the RF MEMS capacitor, inductor and interconnect and design of a third generation RF-MEMS reconfigurable LC-based bandpass filter. To predict the resonant frequencies and tuning range of the filter properly, a complete electromagnetic model of the CMOS-MEMS capacitor is created. The analysis, model, simulation and measurement results of the CMOS-MEMS test capacitor designed with the Jazz 0.35 μm process are given in Chapter 2. Chapter 3 describes how micromachined inductor models are created from the foundry inductor models for both Jazz 0.35 μm and ST Microelectronics 0.25 μm processes. Chapter 4 gives the simulation and measurement results of modeled first generation and second generation filters. After capacitor and inductor models are created, the third generation filter is designed and fabricated with the ST Microelectronics 0.25 μm BiCMOS process. Chapter 5 presents the complete design of CMOS-MEMS capacitor, micromachined inductors, interconnects and filter. The simulation and measurement result comparison of the filter is given at the end of the chapter. Finally, Chapter 6 concludes the thesis and suggests directions for the future work.

2 MEMS Capacitor Model

In a RF-MEMS reconfigurable on-chip LC-based filter, design of the capacitor affects three main performance metrics, high quality factor, wide tuning range and small size. The quality factor of a capacitor is the ratio of toal energy stored to energy lost per cycle. The tuning range of the capacitor is the ratio of maximum capacitance value it can achieve to its minimum capacitance value. Lastly, the size of the capacitor is the total layout area which the capacitor occupies. MEMS capacitors have better tuning range and quality factor when compared to other on-chip capacitors such as diode varactors or accumulation region of MOS varactors [13]. Furthermore, MEMS capacitors have compatible quality factors with fixed-value (untunable) metal-insulator-metal (MIM) capacitors which are commonly used in RFIC design. However, MEMS capacitors occupy much larger area for a specific capacitance value.

The specific MEMS capacitor used in this project is composed of two parallel, interdigitated beams which provide parallel plate capacitance between side walls. The rotor, i.e. moving parallel beams, is connected to left and right lateral electrothermal actuators, whereas the stator is formed by a set of anchored parallel beams and is connected to stator interconnect shown in Figure 2-1 (a). The clutch actuator is used to latch the rotor beams at the desired position when the voltage across the actuators are turned off. The scheme of actuating both lateral capacitance tuning and latch electrothermal actuators is given in [13]. The signal path includes three parts of the capacitor: stator interconnect, interdigitated beams and the left electrothermal actuator (see Figure 2-1 (b)). As the design of the MEMS capacitor is considered, the core part of the capacitor is interdigitated beams which generates the intended capacitance, whereas the electrothermal actuator and stator interconnect are needed for mechanical properties of MEMS capacitor. The electri-

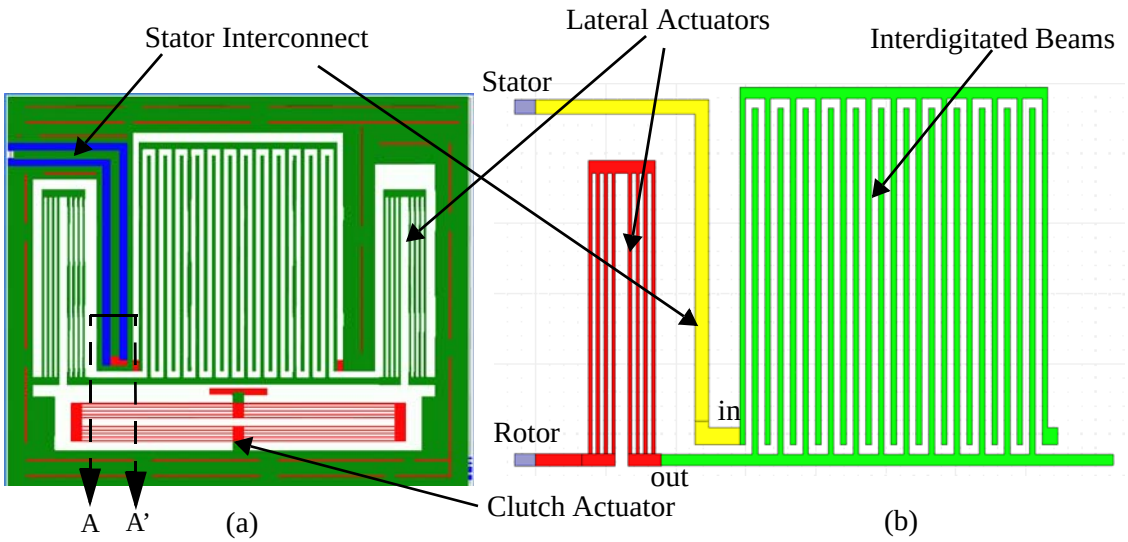


Figure 2-1 (a) Top view of the MEMS capacitor (b) signal path of the MEMS capacitor

cal model of the electrothermal actuator and stator interconnect must be considered as they form the primary parasitics of the MEMS capacitor.

In order to optimize the resonance frequencies, quality factor and size of the tunable RF-MEMS filter, an electromagnetic model of the MEMS capacitor is needed. In order to model the MEMS capacitor in schematic form for design purposes, the electromagnetic model alaysis should take the dimensions of the main design parts of the MEMS capacitor as inputs, and output the behavioural parameters of the MEMS capacitor. The model of the capacitor proposed in this thesis includes additional electrical effects such as self inductance of the metal lines on the signal path, fringing capacitance, and substrate loss, as well as micromachining effects such as metal bloating and polymer deposition on the sidewalls of the interdigitated beams in order to derive the parasitics of the capacitor as well as the core capacitance value. The three main parts of the capacitor- stator interconnect, interdigitated beams and electrothermal actuators- are studied and modeled separately. The new capacitor model parameter expression derivations are explained in the next section and a comparison of simulation results from the model with measurements is given at the end of the chapter.

2.1 Capacitor Model Schematic

The new capacitor model is derived from the main part of the capacitor generating the desired capacitance value, namely the interdigitated beams, as well as the rest of the signal path (signal path with current flow is shown in Figure 2-2), namely the electrothermal actuator and stator interconnect, which contribute to the parasitics. The complete capacitor model is combination of the models of all these parts.

2.1.1 Interdigitated Beams

The interdigitated beams generate a varying capacitance within the tuning range depending on the gap between the beams. The proper estimation of the capacitance of the MEMS capacitor is critically important as it affects the resonance frequency prediction of the filter. Indeed, the model created for the interdigitated beams includes the additional electrical effects such as fringing capacitance as well as parallel plate capacitance, the parasitic self inductance and resistance of the interdigitated beams and CMOS micromachining effects like metal bloating and polymer deposition on the sidewalls of the beams.

Figure 2-3 shows the layout and the model schematic of the interdigitated beams. The capacitance of reconfigurable interdigitated beams is shown as C_{min};C_{max} in the model. The model schematic includes the equivalent interdigitated beam inductance and resistance parasitics, L_{fin} and R_{fin}, respectively. The stator terminal, shown with the label 1 in Figure 2-3 (a) is anchored mechanically and the rotor terminal,

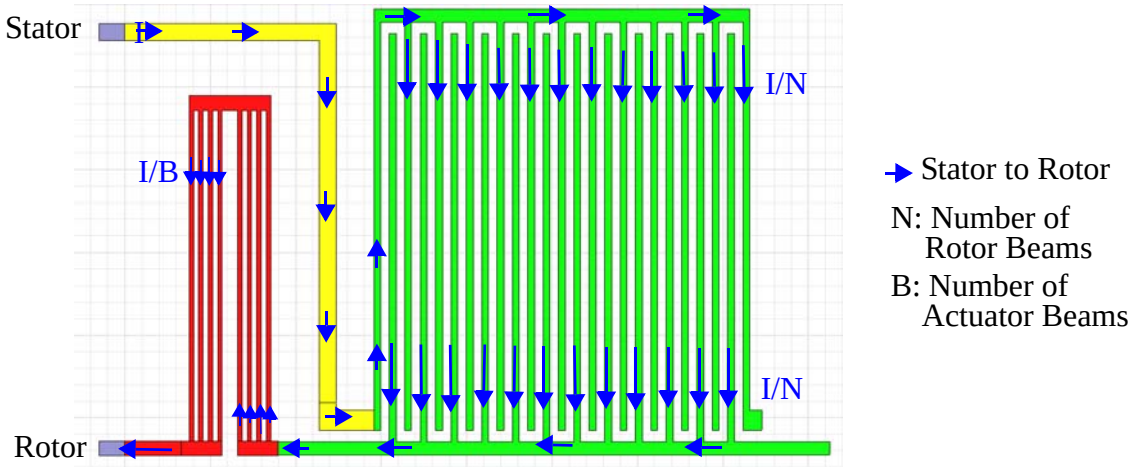


Figure 2-2 Current flows in signal path (from rotor to stator, inverse the current arrows)

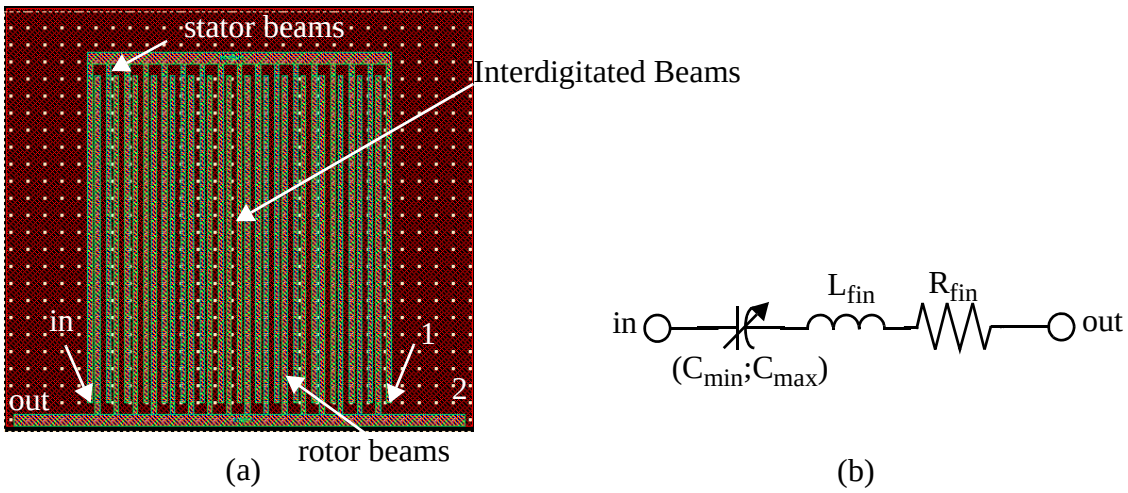


Figure 2-3 (a) layout and (b) model of an array of interdigitated beams

shown with the label *2* in Figure 2-3 (a), is connected to the right electrothermal actuator as shown in Figure 2-1. At these points, there is no electrical connection, hence the signal path shown in Figure 2-1 (b) does not include these parts. Although there is some coupling to the ground at these points, the parasitic capacitance at those points are small and can be neglected. The derivations of the model schematic parameters are described separately below:

2.1.1.1 Tunable Capacitance (C_{min};C_{max}) Derivation

In the derivation of the capacitance between the rotor and stator beams, the fringing capacitance and parallel plate capacitance expressions are derived in terms of the physical design dimensions of the interdigitated beams as well as the metal bloating and polymer deposition dimensions caused by CMOS fabrication and post-CMOS micromachining.

Metal bloating is the expansion of the metal layers in the fabrication, i.e., the metal width on the chip is wider than the width drawn in the layout. The amount of the metal bloating can be found by measuring test structures and it is highly dependent on the foundry process. While the primary sacrificial materials during post-processing are silicon dioxide and silicon, the aluminum layers are also affected by the reactive ion etching steps. Aluminum resputtering leads to the formation of a sidewall polymer film during the dielectric etch. The thickness of the polymer changes from beam to beam and is not uniform along a beam.

The importance of these two issues is that they decrease the tuning range of the MEMS capacitor. Since the metal bloating increases the metal width, the expected maximum gap between the beams decreases, increasing the minimum capacitance. Furthermore, due to polymer on the side walls, the expected minimum gap increases, decreasing the maximum capacitance. Hence the maximum gap is limited by metal bloating, while the minimum gap is limited by polymerization on the side walls.

SEM pictures of three different locations of a test capacitor in Figure 2-4 shows the variance in metal bloating and polymer thickness. As seen in the figure, the total width of the beams is 4.42 μm; since the layout width is 4 μm, the metal bloating , m_b is 0.4 μm.The polymer thickness, t_p, has much more variance and is not uniform, hence this value is given as an average across a given sidewall. The average polymer thickness on the sidewall of a beam from beam to beam varies from 0.1 μm to 0.2 μm. As seen in Figure 2-4, the beams are in the maximum capacitance situation, however, there is an air gap between the polymers. The main reason for this air gap is lateral curling of the beams because of residual stress variance along the beam. Instead of addressing a new model parameter, for simplicity, an effective polymer thickness is introduced in the model that includes the effect of this gap as well. Since the polymer dielectric constant is not known, a relative permittivity of 1 is assumed. Hence, t_p in the model can change from 0.2 μm to 0.5 μm including the air gap.

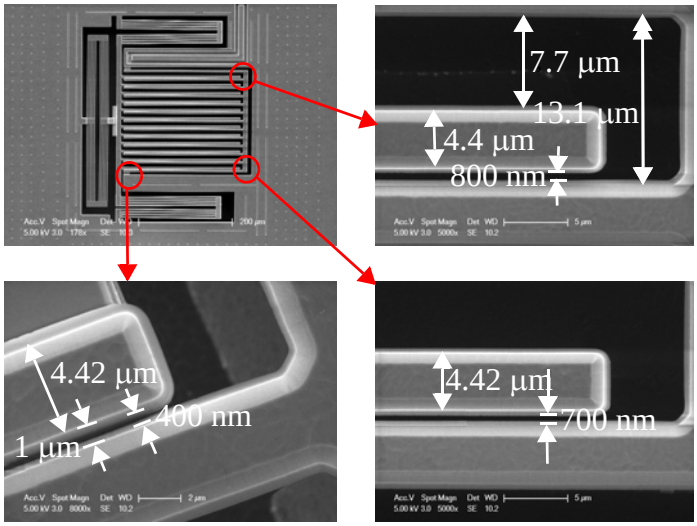


Figure 2-4 SEM photos of edges of interdigitated beams for extracting metal bloating amount and polymer thickness on the sidewalls of the beams

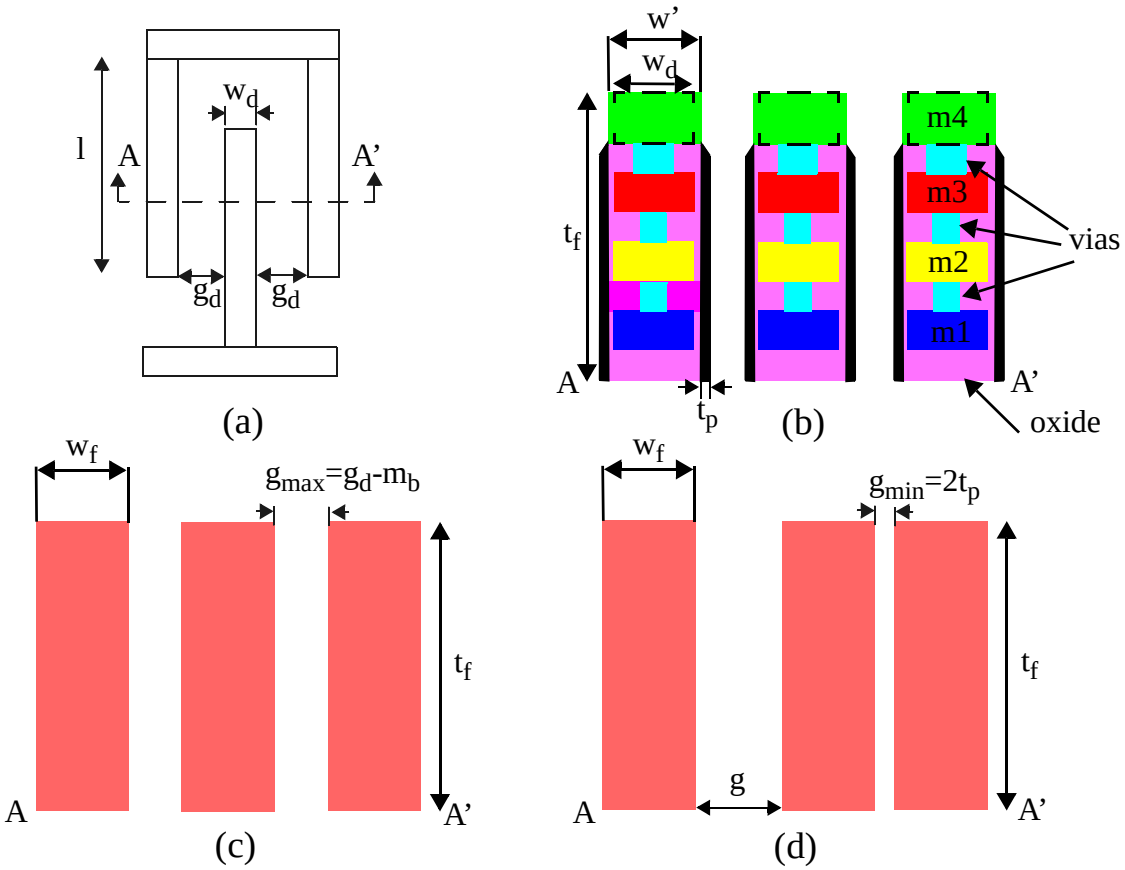


Figure 2-5 (a) top view of a set of interdigitated beams (b) cross-section view of one set of interdigitated beams with metal bloating and polymer (c) cross-section of modeled set of beams for minimum capacitance case (d) cross-section view of modeled set of beams for maximum capacitance case (the figures are not scaled)

The derivation of the capacitance formula assumes that the beams are a single metal layer instead of stacked metal-oxide composite with via layers as shown in Figure 2-5. After making this assumption, the capacitance derivation formula of Johnson and Warne [14] can be used. A brief explanation of [14] is given in Appendix A.1.3. As can be guessed, since modeling the beams as a single solid metal layer can cause a capacitance overestimation, some simulations verifying the accuracy of this assumption were performed with a finite element modeling tool, FEMLAB. The simulation results are given at the end of the chapter.

The cross-section model of a set of interdigitated beams at the minimum and maximum capacitance configurations are shown in Figure 2-5 (c) and Figure 2-5 (d), respectively. For the maximum capacitance case, the gap labeled as g is much greater than g_{min}, hence the capacitance generated by this wider gap is neglected.

The complete minimum and maximum capacitance expressions of the interdigitated beams model are given below:

$$C_{min} = Nl_{fin}\left(\frac{2\varepsilon_0 t_f}{g_{max}} + \frac{2\varepsilon_0 K(\sin((\pi w')/4(w'+g_{max})))}{K(\cos((\pi w')/4(w'+g_{max})))}\right) \tag{2.1}$$

$$K(x) = \int_0^{\pi/2} \frac{1}{\sqrt{1-x^2(\sin(\theta))^2}} d\theta \tag{2.2}$$

$$C_{max} = Nl_{fin}\left(\frac{\varepsilon_0 t_f}{g_{min}} + \frac{\varepsilon_0}{\pi} ln\left(\left(\left(\frac{w'}{g_{min}}+1\right)^2 - 1\right)\left(1+\frac{2g_{min}}{w'}\right)^{\left(1+\frac{w'}{g_{min}}\right)}\right)\right) \tag{2.3}$$

$$w' = w_d + m_b, g_{max} = g_d - m_b, g_{min} = 2t_p \tag{2.4}$$

where N is the number of beams, w_d is the width drawn on the layout, t_f is the beam thickness, w_f is the beam width, m_b is the metal bloating amount, t_p is the thickness of the polymer deposited on the side walls of the beams.

2.1.1.2 Equivalent Inductance of Interdigitated Beams

The expression of the dc inductance of a metal line [15] can be found in Appendix A.1.1. Since it is tedious to try to derive a formula for the inductance at both minimum and maximum capacitance cases, the worst case inductance is derived. The mutual inductance between the rotor beams and stator beams will change depending on the whether the capacitor is at its minimum or maximum configuration. Figure 2-6 shows the representation of self inductances and mutual inductances of the interdigitated beams. As seen in Figure 2-6 (a), the currents passing through the inductances are in the same direction except for the left most stator beam. The mutual inductance will have its maximum value when the rotor beams are in the position creating the maximum capacitance, whereas it is minimum when the rotor beams are in the middle of the gap between stator beams (shown in Figure 2-6 (b)). As the worst case is when the mutual inductance is maximum, the equivalent inductance will be approximately equal to $L + (L + M)/N$. In the minimum

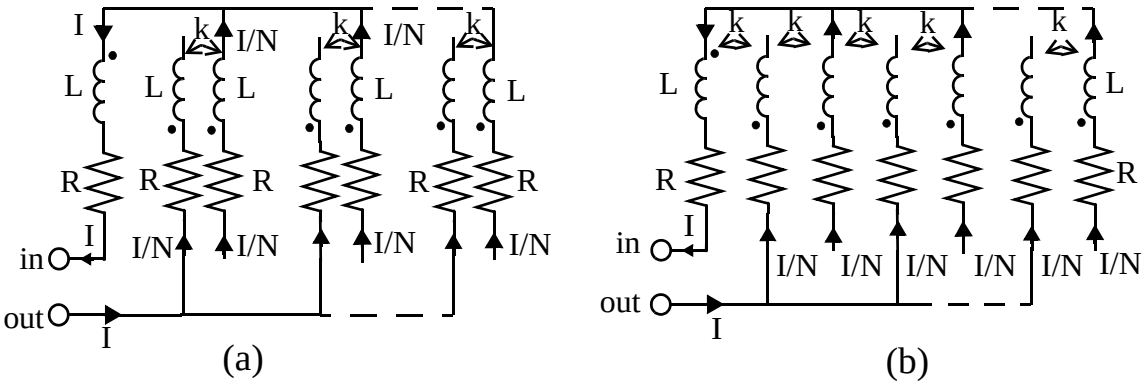


Figure 2-6 interdigitated beams represented with inductances and resistances for (a) maximum and (b) minimum capacitance positions

mutual inductance case, predicting the equivalent inductance is more difficult because the rotor beams interact with the stator beams on both sides. However, since the mutual inductance is smaller, and there will be a negative mutual inductance between the most left most stator beam and the left most rotor beam, the equivalent inductance of minimum capacitance case will be slightly lower than the one for maximum capacitance. As a result, (2.5) shows the worst case equivalent inductance for the interdigitated beams.

$$L_{fin} = 2l_{fin}\left(\frac{(N+1)}{N}\left(ln\left(\frac{2l_{fin}}{w'+t_f}\right)+\frac{1}{2}+\frac{w'+t_f}{3l_{fin}}\right)+Q\right) \tag{2.5}$$

$$Q = ln\left(\frac{l_{fin}}{w'+g}+\sqrt{1+\left(\frac{l_{fin}}{w'+g}\right)^2}\right)-\sqrt{1+\left(\frac{w'+g}{l_{fin}}\right)^2}-\frac{w'+g}{l_{fin}} \tag{2.6}$$

2.1.1.3 Equivalent Resistance of the Interdigitated Beams

While calculating the equivalent resistance of the interdigitated beams, since all the metal layers are parallel to each other, the equivalent sheet resistance of one beam, R_s, is calculated using all of sheet resistances of metal layers as shown in (2.7). As seen in Figure 2-5, there are vias between the metal layers decreasing the equivalent resistance. For simplicity, these vias are neglected to calculate the worst case resistance. Figure 2-6 shows the interdigitated beams with the resistor representations. With this configuration, the worst case equivalent resistance can be calculated. Since there are 2N beams of 2R parallel resistances, the equivalent resistance of the interdigitated beams is $\frac{(N+2)}{N}R$. As can be seen, the truss

resistances are neglected in the calculation. The equivalent resistance does not change with the rotor position assuming that there is no lateral curl due to actuation.

$$R_s = \left(\frac{1}{R_{s_{M1}}} + \frac{1}{R_{s_{M2}}} + \frac{1}{R_{s_{M3}}} + \frac{1}{R_{s_{M4}}}\right)^{-1}; R_{fin} = \frac{(N+2)}{N}\frac{R_s l_{fin}}{w_f} \tag{2.7}$$

2.1.2 The Parasitics of the MEMS Capacitor

2.1.2.1 Stator Interconnect

In order to match the vertical curl of the stator and rotor beams, both the sets of beams need to be anchored at the bottom as shown in Figure 2-1. Hence, in order for the current to reach the stator beams, an interconnect must be designed within the capacitor. Although the stator interconnect is needed for mechanical stability, it creates significant parasitics. In order to predict and optimize the parasitics of the MEMS capacitor, the stator interconnect model is developed next.

Figure 2-7 shows the cross-section views of a microstrip line and the stator interconnect design used in MEMS capacitor. As seen in this figure, to decrease the oxide capacitance, C_{ox}, the metal1 shielding is removed under the signal line except for a small amount of overlap (set by the CMOS-MEMS design rules [16]). This overlap prevents the etch step from removing the silicon under the interconnect. However, this creates the need for the substrate resistance to be included in the schematic model of interconnect. The effect

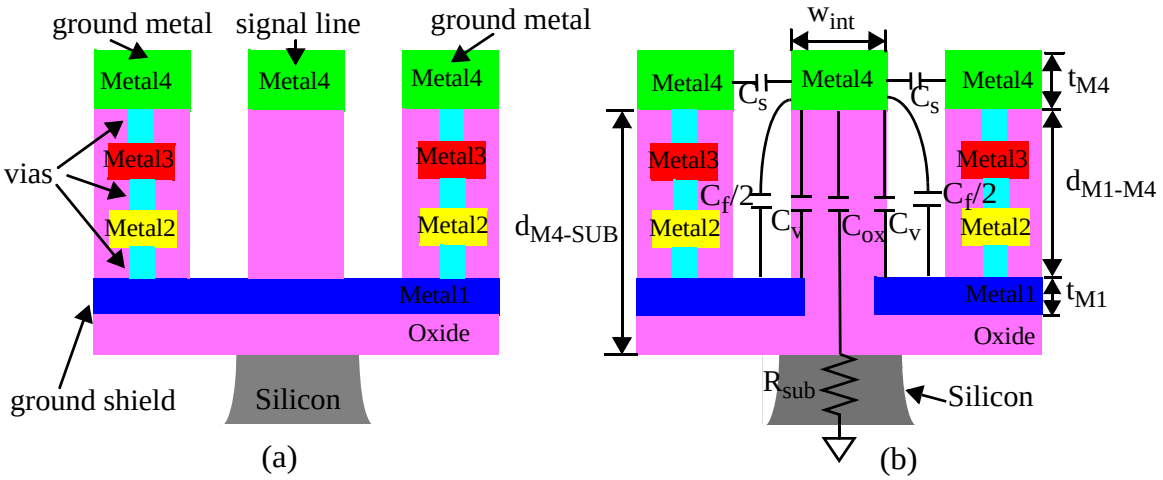


Figure 2-7 Cross-section of A-A' pointed in Figure 2-1(a) for (a) a microstrip line (b) stator interconnect

of the substrate resistance can be suppressed by putting as many substrate contacts as possible close to the etch pit.

The proposed model of the stator interconnect is shown in Figure 2-8. The self inductance and self resistance of the stator interconnect are shown as L_{int} and R_{int} in the model, respectively. The total parasitic capacitance between signal line and ground is shown as C_{gr}, the capacitance between signal line and substrate is C_{ox} and the equivalent substrate resistance to ground is shown as R_{sub}.

The expressions for self inductance, L_{int}, and self resistance, R_{int}, of the stator interconnect is given below:

$$L_{int} = 2l_{int}\left(ln\left(\frac{2l_{int}}{w_{int}+t_{M4}}\right)+\frac{1}{2}+\frac{w_{int}+t_{M4}}{3l_{int}}\right), R_{int} = \frac{R_{s_{M4}}l_{int}}{w_{int}} \quad (2.8)$$

where l_{int} is the length of the stator interconnect, t_{M4} is the thickness of the top metal, w_{int} is the width of the stator interconnect and $R_{s_{M4}}$ is the sheet resistance of metal4.

In the cross section shown in Figure 2-7 (b), the capacitance between the signal line and ground, C_{gr}, is composed of the lateral parallel plate capacitances, $2C_s$, the vertical parallel plate capacitance between the signal line and the bottom metal ground, $2C_v$, and the fringing capacitance between signal line and the bottom metal plate, C_f. The fringing capacitance, C_f, is sum of the fringing capacitance in the air, C_{f1} and the fringing capacitance in the oxide, C_{f2}. A brief explanation of fringing capacitance formula [17] is given in Appendix A.1.2. The vertical parallel plate capacitance between the signal line and the substrate

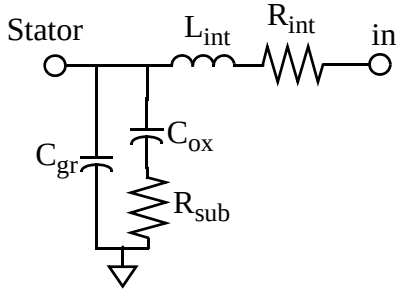


Figure 2-8 Proposed schematic of stator interconnect

and the substrate resistance are modeled as C_{ox} and R_{sub}, respectively. The expressions for all these parameters were given in (2.9)-(2.11).

$$C_s = \frac{\varepsilon_0 l_{int} t_{M4}}{g_{int}}, C_v = \frac{\varepsilon_0 l_{int} d_{ov}}{d_{M1-M4}} \tag{2.9}$$

$$C_{f1} = \frac{2\pi\varepsilon_0 l_{int}}{ln(1 + k_1 + \sqrt{k_1(k_1+2)})}, C_{f2} = \frac{2\pi\varepsilon_{rox}\varepsilon_0 l_{int}}{ln(1 + k_2 + \sqrt{k_2(k_2+2)})}, C_f = C_{f1} + C_{f2} \tag{2.10}$$

$$C_{gr} = 2C_s + 2C_v + C_{ox}, C_{ox} = \frac{\varepsilon_0 l_{int} w_{int}}{d_{M4-SUB}} \tag{2.11}$$

where ε_0 is the air permittivity constant, 8.854×10^{-12} F/m, g_{int} is the lateral gap between the signal line and the top metal ground, d_{ov} is the overlap of metal1 and metal4 drawn in the layout which is 0.3μm, d_{M1-M4} is the vertical distance between the bottom of the top metal layer and the top of the lowest metal layer. In the fringing capacitance formula, k_1 and k_2 are $2(d_{M1-M4}/t_{M4})$ and $2(d_{M1-M4}/t_{M1})$, respectively, where t_{M1} is the thickness of the lowest metal layer. In the expression of C_{ox}, d_{M4-SUB} is the vertical distance between the bottom of top metal layer and the top surface of the substrate. Since the substrate resistance is dependent on several parameters such as substrate contacts locations and silicon undercut, there is no substrate resistance expression proposed with this model. The substrate resistance for this model is found roughly by assuming that the silicon under the signal line has a rectangular cross-section. The length and area of the silicon is approximated according to the locations of metal4 to substrate contacts. As mentioned earlier, the substrate resistance can be decreased by putting many substrate contacts close to the etch pit. The stator interconnect parasitics decrease the overall quality factor of the MEMS capacitor significantly.

2.1.2.2 Electrothermal Actuator

The rotor beams move to tune the MEMS capacitor by means of electrothermal actuators. The design and the working principles of the electrothermal actuators can be found in [13]. Although two electrothermal actuators are used to move the beams, only one electrothermal carries the RF signal as shown in

Figure 2-1 (b) and Figure 2-2. Like stator interconnect, the electrothermal actuator carrying the signal causes parasitics for the MEMS capacitor, hence decreases the quality factor.

The top view, cross-section view and the schematic model of the electrothermal actuators are shown in Figure 2-9. As seen in Figure 2-9 (b), the RF signal is carried by stack of metal2, metal3 and metal4 layers, whereas the dc signal to actuate the beams is carried by metal1. Since the ground lines and signal sources of both RF and dc paths are different, the coupling between these two lines do not need to be included in the model. For simplicity, while expressing the self inductance of the actuator, only the top metal layer is taken into account. Furthermore, the coupling inductance between the beams is neglected. The expressions for the model parameters are given below:

$$L_{act} = \frac{2}{b}L_b = \frac{4}{b}l_b\left(ln\left(\frac{2l_b}{w_b + t_b}\right) + \frac{1}{2} + \frac{w_b + t_b}{3l_b}\right) \tag{2.12}$$

$$R_{s_b} = \left(\frac{1}{R_{s_{M2}}} + \frac{1}{R_{s_{M3}}} + \frac{1}{R_{s_{M4}}}\right)^{-1}, R_{act} = \frac{2}{b}r_b = \frac{2}{b}\frac{R_{s_b}l_b}{w_b} \tag{2.13}$$

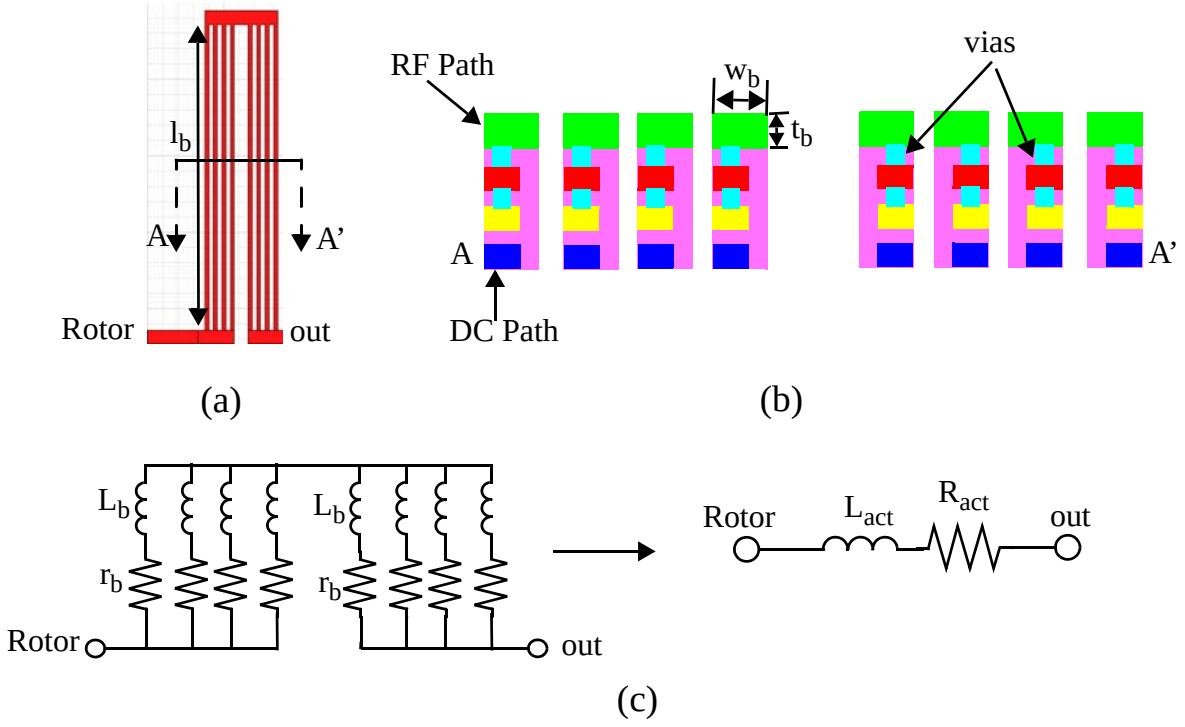


Figure 2-9 (a) top view of actuators with resistors and inductors (b) cross-section view of A-A' pointed in (a) and (c) proposed model for electrothermal actuator

where b is the number of beams in one arm of the actuator, l_b is the length of a beam, w_b is the width of a beam, t_b is thickness of a beam, and R_{s_b} is the overall sheet resistance of a beam.

2.1.3 The Complete Schematic of MEMS Capacitor Model

In order to complete the model of the MEMS capacitor, the model schematics of interdigitated beams, stator interconnect and actuator are combined in Figure 2-10. The model parameters and the equations to be used to calculate them are shown in Table 2-1.

In order to increase the speed of modeling process, a MATLAB file evaluating all the equations is created. The capacitor_model.m file (see Appendix A.2.5) takes all necessary process constants and capacitor dimensions as inputs, and it outputs all the schematic component values, capacitance vs. frequency and quality factor vs. frequency graph for both minimum and maximum capacitance cases. The inputs and the outputs of the capacitor_model.m file are shown in Table 2-2. The parameters declared as constant in the model parameter expressions are not included in the table.

It is important to mention again that this capacitor model is generated to predict the tuning range and the quality factor properly in order to have better control in the specifications of an RF-MEMS reconfigurable LC-based filter. As can be guessed easily, the parasitics of the MEMS capacitor are calculated assuming the worst case, hence it is expected that the parasitic inductance and resistance values of the capacitor can be higher than the actual values. Although the parasitic values calculated from geometry are higher than expected, the model file enables the designer extract the actual values by matching the model simula-

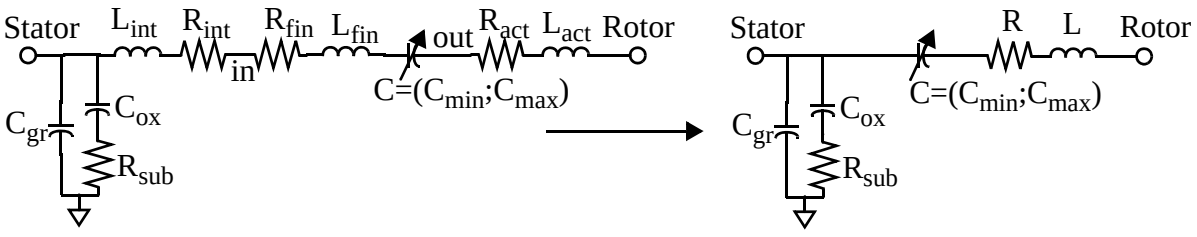


Figure 2-10 (a) Complete model of MEMS capacitors

Table 2-1. The model parameters and the equations needed to calculate them

Model Parameter	**Equations**
C_{min}	(2.1), (2.2) and (2.4)
C_{max}	(2.3) and (2.4)
$L=L_{fin}+L_{int}+L_{act}$	(2.5), (2.6), (2.8) and (2.12)
$R=R_{fin}+R_{int}+R_{act}$	(2.7), (2.8) and (2.13)
C_{gr}	(2.9), (2.10) and (2.11)
C_{ox}	(2.11)
R_{sub}	N/A

Table 2-2. Dimensions and model parameter values of the MEMS capacitor

Inputs	**Description**	**Outputs**	**Description**
lf	beam length	Cmin	minimum capacitance
wf	beam width	Cmax	maximum capacitance
tf	beam thickness	L	self inductance
gmin	minimum gap	R	self resistance
gmax	maximum gap	C_{gr}	capacitance to the ground
n	number of rotor beams	C_{ox}	oxide capacitance
GMD	pitch of the beams	R_{sub}	substrate resistance
b	number of actuator beams	C_{min} vs. Freq, C_{max} vs. Freq.	graph
lb	length of actuator beams	Q_{min} vs. Freq, Q_{max} vs. Freq	graph
wb	width of actuator beams		
lint	interconnect length		
wint	interconnect width		
gint	gap next to interconnect		

tion and measurement results. This model is applied for several capacitors. The next section presents the model schematic simulations using several simulation tools, measurement results of test capacitors, and their comparison.

2.2 Simulation and Measurement Results

In order to test and verify the MEMS capacitor model, simulations with the finite element modeling tool FEMLAB, electromagnetic simulation tool HFSS, and the analog and mixed-signal circuit simulator Virtuoso Spectre, are performed. One test capacitor with one port was designed and fabricated in the Jazz

0.35 μm BiCMOS process. The validity check of modeling the beams as one composite layer of metal is performed with the FEMLAB simulations, is described in the next section.

2.2.1 FEMLAB Simulations

In order to verify the approximation of interdigitated beams as one composite metal layer, 2D FEMLAB simulation of one set of beams consisting of two stator beams and one rotor beam has been performed. The three adjacent beams that form a set are shown with vias in Figure 2-11 (a), without vias in Figure 2-11 (b) and as a single composite layer in Figure 2-11 (c). To account for the fact the two outer stator beams have their own adjacent rotor beams, symmetrical boundary conditions are used on middle of the stator beams at the left and right of the finite element model as shown in Figure 2-11. The top and bottom of the model is extended far enough away from the top and bottom of the beams to ensure it does not affect the solution. Secondly, the subdomains such as metal layers, oxide layers and air have been defined. The boundaries of the metal layers in the left and right beams are defined as the same voltage, V_0, and those of middle beam are defined as ground. Outside rectangle boundaries representing air are defined as zero-charge. After setting the boundaries, the meshes are created, refined and the problem is solved for all three combinations. The electric potential spectrum and electric field arrows for the corresponding combinations

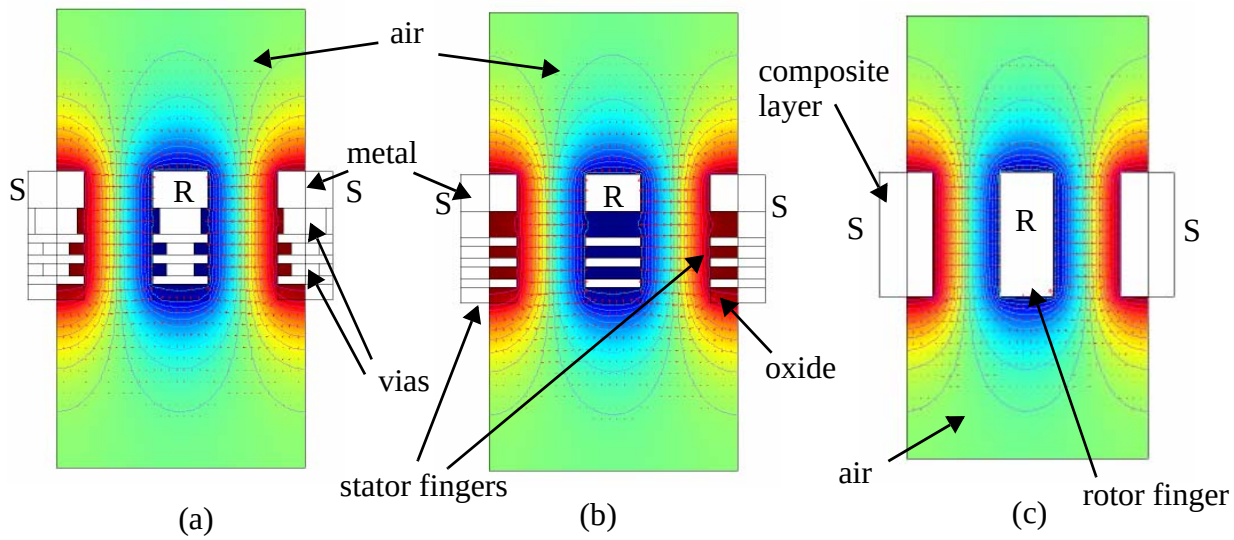


Figure 2-11 2D simulation results with electric potential spectrum and electric field arrows for interdigitated finger group (a) with vias (b) without vias and (c) as one composite metal layer in FEMLAB

are shown in Figure 2-11. Since these structures are two dimensional (2D), the capacitance per length is calculated as shown in (2.14).

$$C_{per-length} = \int 2\frac{w_{e-emes}}{V_0^2} \tag{2.14}$$

where w_{e-emes} electical energy density. In Figure 2-11, the width of the beams and the gap between the beams are 4 μm and 5 μm, respectively. The capacitance per length for the set of interdigitated beams modeled as one composite metal layer has the most capacitance per unit length, 5.21×10^{-11} fF/m, while the case with vias and without vias has capacitance per length of 4.99×10^{-11} fF/m and 4.98×10^{-11} fF/m, respectively. As can be calculated with these numbers, the model of interdigitated beams estimated the capacitance with less than 5% error. The main reason for the interdigitated beams with vias and without vias have almost same capacitance values is that higher permittivity of oxide between the metal layers shield the electric field lines like a conducting boundary. Hence, as the permittivity increases between the metal layers, the capacitance values converge to each other. This simulation verifies that the approximation of the interdigitated beams as one composite metal layer is accurate to 96%.

2.2.2 Circuit Simulations

In order to verify the overall capacitor model, in Virtuoso Spectre, a one port S-parameter analysis is performed with the test bench schematic shown in Figure 2-12. After getting the S_{11} data, the capacitance, C, and the quality factor, Q can be extracted by using (2.15).

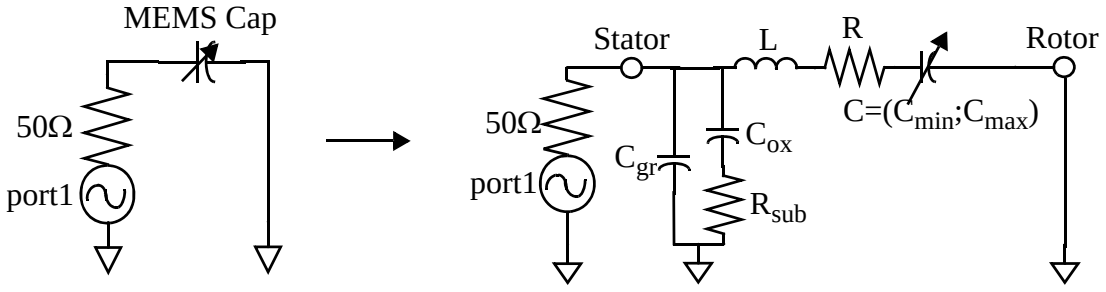


Figure 2-12 (a) Test bench schematic of MEMS capacitor with proposed capacitor model

$$Z_{11oneport} = Z_0 \frac{1+S_{11}}{1-S_{11}},\ C = \frac{-1}{wIm(Z_{11oneport})},\ Q = \frac{Im(Z_{11oneport})}{Re(Z_{11oneport})} \tag{2.15}$$

As can be guessed from (2.15), the capacitance is extracted assuming that the whole device under test (DUT) is behaving like a capacitor. Hence, all the reactance of the input impedance is assumed to be negative. However that is not the case in reality. This phenomenon can be explained with an example. If the capacitor model is assumed to be an RLC series network, the input impedance of the model will be

$$Z = R + jwL + \frac{1}{jwC_0} = R + j\left(wL - \frac{1}{wC_0}\right) = R + j\left(\frac{w^2LC_0 - 1}{wC_0}\right) \tag{2.16}$$

If we use (2.15) to extract the capacitance from the input impedance, we get

$$C = \frac{-1}{wIm(Z)} = \frac{-C_0}{w^2LC_0 - 1} \tag{2.17}$$

As can be seen in (2.17), the capacitance at dc gives the series capacitance. Furthermore, this expression goes to infinity at the self resonance frequency of $1/(\sqrt{LC_0})$. The self inductance of the capacitor can be extracted by using $1/w_0{}^2C_0$, where w_0 is the self resonance frequency. However, as seen in Figure 2-12, the MEMS capacitor model consists of parallel branches of RC networks as well as series RLC network which makes the analysis more difficult. The derivation of capacitance and quality factor for the MEMS capacitor model is shown in Appendix A.2.3 and Appendix A.2.4.

2.2.3 Electromagnetic Simulations with HFSS

Although electromagnetic simulation tools takes significant computation time, they provide precise results to predict the measurement data. The test capacitor layout in the minimum capacitance position is transferred into the 3D electromagnetic simulation tool HFSS and a two port test is applied. The steps for HFSS simulation are given in Appendix B. Figure 2-13 shows the oblique and top view of the MEMS capacitor modeled for HFSS simulations. As shown in the figure, port1 is placed to the node “stator”, while port2 is at node “rotor”. After two port S-parameter analysis, $Z_{11oneport}$ can be found as shown in (2.18).

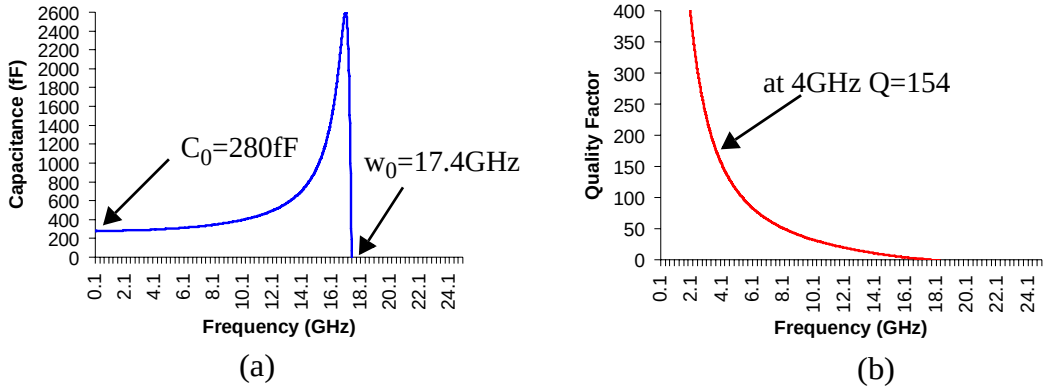


Figure 2-14 l(a) Capacitance and (b Quality factor change with frequency extracted from HFSS simulation

$$S_{11oneport} = S_{11} - \frac{S_{12}S_{21}}{1+S_{22}}, Z_{11oneport} = Z_0\frac{1+S_{11oneport}}{1-S_{11oneport}} \tag{2.18}$$

$Z_{11oneport}$ data can be used to extract the capacitor and quality factor using (2.15). The capacitance and quality factor change with frequency are shown in Figure 2-14. Although C and Q-factor of the capacitor can be extracted from two-port S-parameter simulation, this extraction method is not different from one-port test. In order to write the expressions in (2.18), the capacitor should be terminated with ground. The proof of the expressions in (2.18) can be obtained in [12]. HFSS simulation gives consistent results for dc capacitance and self inductance, however the quality factor (Q) is much higher than it is expected. The main reason for this difference is that the layout transferred to HFSS models treats the interdigitated and actuator

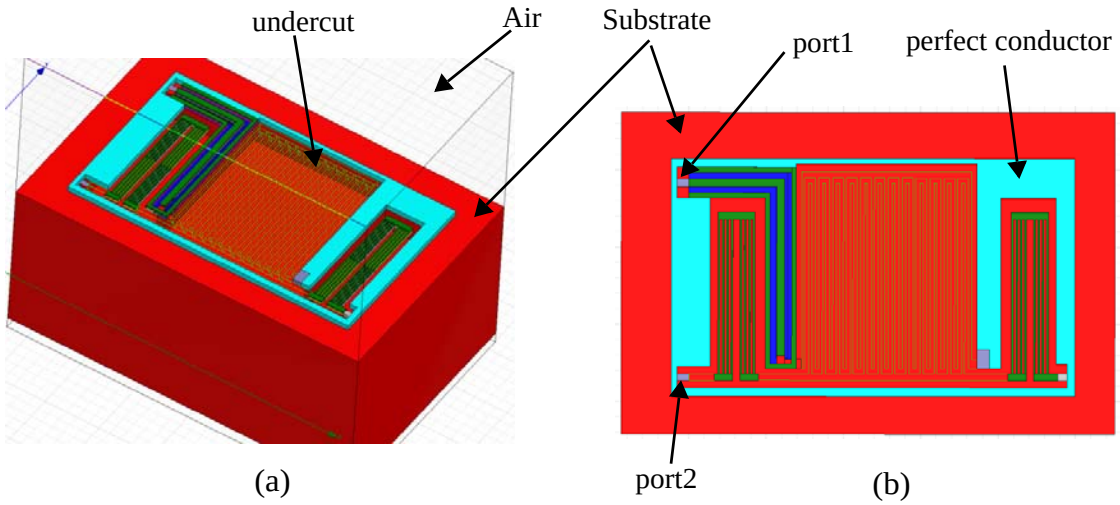


Figure 2-13 (a) Oblique and (b) top view of MEMS cap layout in HFSS

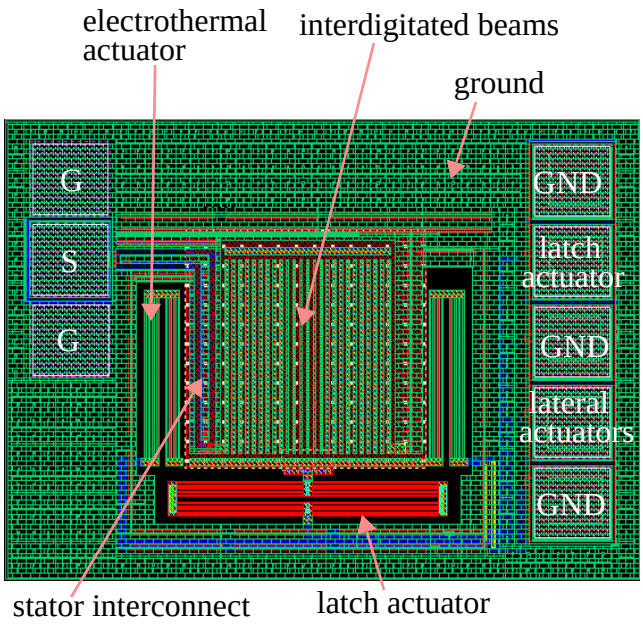


Figure 2-15 Layout of the test capacitor

Table 2-3. Model file Inputs and Outputs

Input	Value	Output	Value
lf	247 µm	Cmin	163 fF
wf	4 µm	Cmax	479 fF
tf	9.835 µm	L	649 pH
gmin	0.65 µm	R	1.7 Ω
gmax	4.6 µm	C_{gr}	37 fF
n	12	C_{ox}	23 fF
GMD	5 µm	R_{sub}	1500 Ω
b	4		
lb	200 µm		
wb	2.6 µm		
lint	350 µm		
wint	10 µm		
gint	8 µm		

beams as composite layers, decreasing the equivalent resistance of the capacitor substantially. As the series equivalent resistance decreases, Q of the MEMS capacitor increases as seen in (2.15).

2.2.4 Measurement Results

The test capacitors were fabricated in Jazz 0.35 µm BiCMOS process, and are released using the ASIMPS post-foundry micromachining process [18]. One port S-parameter measurements were performed using an Agilent E8364A Network Analyzer and Cascade Microtech 6” RF Probe Station with GSG probes. The schematic representation of the test circuit is given in Figure 2-12. Beside the test capacitors, open and short GSG pads were also fabricated, and the parasitics of open and short GSG pad are de-embedded in MATLAB. The capacitance and quality factor change with frequency are extracted by means of a MATLAB file. The file, capacitor test set-up and deembedding steps are given in Appendix D.

The layout, dimensions and the model parameter values of the test capacitor are given in Figure 2-15. The values given in Table 2-3 were placed to the circuit schematic shown in Figure 2-12. S-parameter data from Spectre and the Network Analyzer were processed in the Matlab file given in Appendix A.2.5,

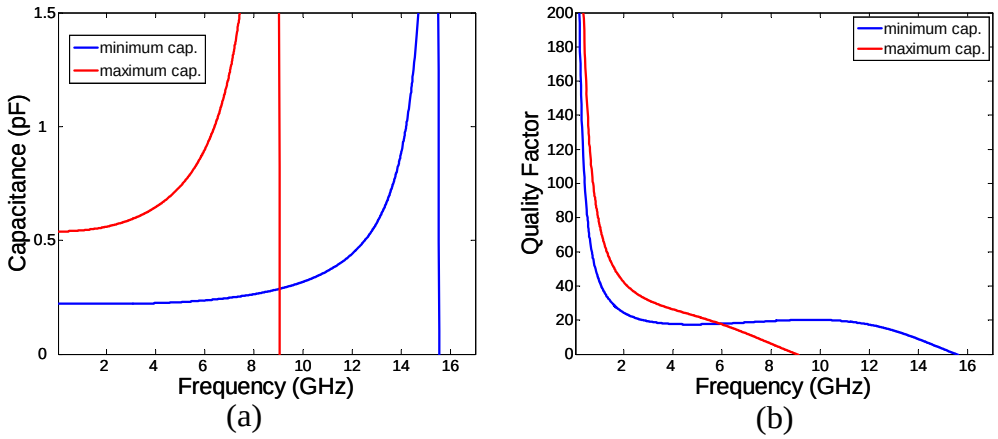


Figure 2-15 (a) Capacitance and (b) Quality factor characteristics for both minimum and maximum cases extracted from MATLAB model file

and as a result, the capacitance and quality factor change with frequency was characterized for both minimum and maximum frequency cases. Figure 2-15 shows the capacitance and quality factor data obtained from the MATLAB file. The measurement and the fitted simulation results are given in Figure 2-16.

As can be seen in Figure 2-15 and Figure 2-16, the model and measured capacitance values match each other, however the inductance values are overestimated in the model as expected. This overestimation

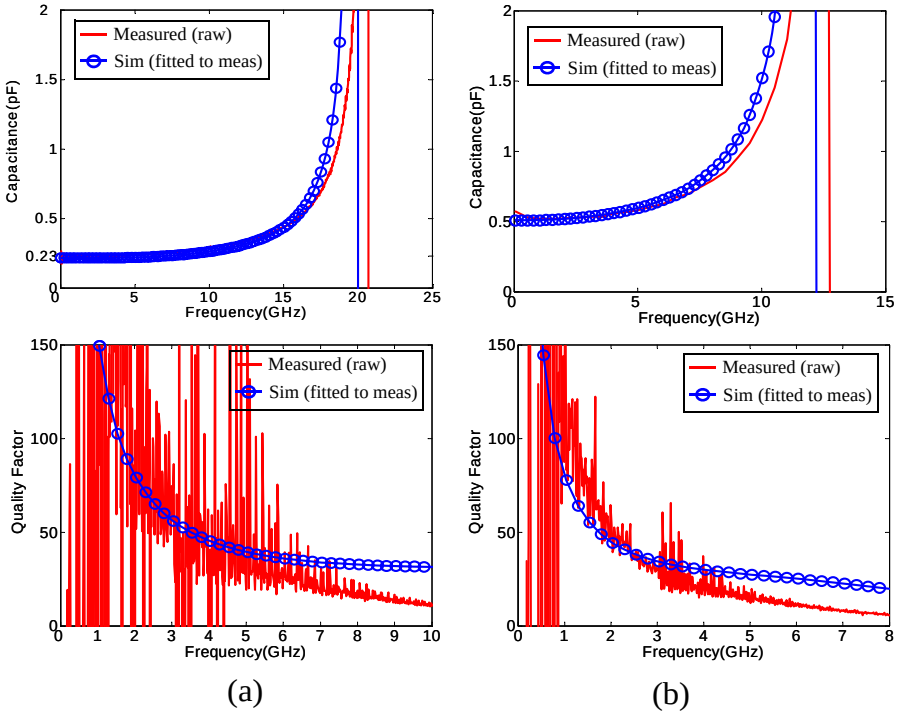


Figure 2-16 Measured and fitted capacitance and quality factor characteristics for both (a) minimum and (b) maximum capacitance cases of the test capacitor

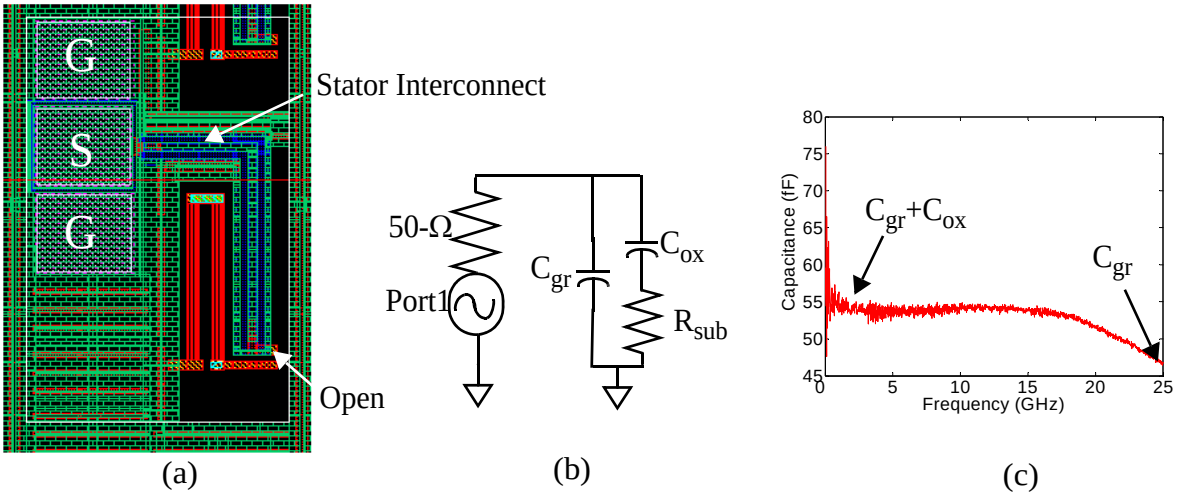


Figure 2-17 (a) Layout and (b) model schematic of stator interconnect test structure (c) Parasitic capacitance extraction using open stator interconnect test structure

causes the self resonance frequencies of the model simulation results to be lower for both maximum and minimum capacitance cases. The calculated results are obtained by putting the extracted values of the components from the measured data. The extraction of the schematic components are given in the next section.

2.2.4.1 Extraction of Model Parameters

As the input impedance of the model schematic is placed into (2.17), it can be seen that, at DC, the capacitance, C_0, is equal to $C_{gr} + C_{ox} + C$. In order to find the individual values of C_{gr}, C_{ox} and C, the stator interconnect test structure is designed and fabricated. Figure 2-17 shows the stator interconnect test structure layout, model schematic and the capacitance vs. frequency graph. As shown in Figure 2-17, the values of C_{gr} and C_{ox} can be extracted from the figure. As these values are found, C can also be found by using $C_0 - C_{gr} - C_{ox}$. The self inductance of the MEMS capacitor can be found approximately by using self resonance frequency and C.

The substrate resistance and the series parasitic resistance are not easy to extract, the real part of the impedance is highly dependent on the frequency and other component values. Hence, the series resistance predicted in the model is assumed to be correct for measured data as well. In order to estimate substrate resistance, the model MATLAB file is used. The substrate resistance is tuned until the model simulation

Table 2-4. Estimated values and extracted values of capacitor model parameters

Parameters	**Simulated Values**	**Extracted Values**
Cmin	163 fF	176 fF
Cmax	479 fF	478 fF
L	649 pH	332 pH
R	1.7 Ω	1.7 Ω
C_{gr}	37 fF	43 fF
C_{ox}	23 fF	12 fF
R_{sub}	1500 Ω	300 Ω

results fit the measured data. The model component values from this procedure and the extracted values are given in Table 2-4.

As seen in the table, the simulated values are matching the extracted values for minimum and maximum capacitance with less than 7% difference, however, the self inductance is estimated much higher than the extracted value. As declared in Section 2.1.1 and Section 2.1.2, the self inductance is estimated as the worst case value. In order to decrease the error in self inductance, some HFSS simulations need to be done to understand which part of inductance is overestimated. The values of C_{gr} and C_{ox} are extracted as shown, in Figure 2-17 (c). The substrate resistance value affect the real part of the input impedance, hence its value is adjusted to fit the quality factor curves. As seen in Figure 2-16, the quality factor curves match until 6GHz and 3.5GHz for minimum and maximum capacitance cases, respectively. The main reason for mismatch at high frequencies is that the series RLC network model of interdigitated beams is a distributed RLC network in reality.

2.3 Summary

In this chapter, electromagnetic characterization of the MEMS capacitor is performed combining the models of main parts of the capacitor, interdigitated beams, electrothermal actuator and stator interconnect. It should be mentioned again that deriving the complete model of MEMS capacitor enables prediction and design the RF-MEMS reconfigurable LC based filter. Moreover, by deriving the model, the detailed

analysis of parasitic effects have been understood, and in the new design, parasitics are minimized. The new MEMS capacitor design used in third generation filter is presented in Section 5.2.3.

The model of MEMS capacitor is verified by simulations performed in FEMLAB, HFSS and comparison between simulations in Spectre and measurement results. As mentioned before, the model overestimates the parasitic inductance and resistance. While designing the filter, the inductance values obtained from the capacitor model file are decreased by the avarage ratio of the extracted inductance values to the estimated inductance values (40%) to compensate the overestimation of self inductance of the MEMS capacitor.

3 MEMS Inductor Model

A MEMS inductor model is needed to estimate the insertion loss and quality factor of the RF-MEMS on-chip LC-based filters. Although usage of differential inductors and post-foundry micromachining increases the quality factor by a significant amount [19], it remains a limiting factor to overall filter performance. An accurate model of MEMS inductor enables effective use of this high quality factor in filter design optimization. For the differential spiral inductors in both the Jazz 0.35um BiCMOS and ST Microelectronics 0.25um BiCMOS, the models provided by the foundry represent the inductor after CMOS fabrication. Hence the inductor models need to be modified to incorporate the effects of post-CMOS micromachining. This chapter describes how the foundry inductor models are modified and compares the foundry inductor with the micromachined inductor. The foundry inductors for Jazz and ST are presented separately, with the simulation and measurement results provided at the end of each section respectively.

3.1 Jazz 0.35 μm Inductor Modeling

Figure 3-1. shows a 12 nH Jazz differential inductor layout, and zoomed view of the part circled in Figure 3-1(a) after foundry fabrication and after post-foundry micromachining. In the foundry inductor, in Figure 3-1(b), the total capacitance between inductor's two terminals, C_{p12}, is parallel combination of three different capacitances, turn-to-turn capacitance C_{t-t}, the total fringing capacitance between the terminals of the inductor, C_f, and the overlap capacitance C_{ov}. The inductor is coupled with the silicon substrate through the capacitance C_{ox}. The silicon substrate is modeled by parallel resistance R_{sub} and capacitance C_{sub}. The complete schematic of the foundry inductor model is shown in Figure 3-2. As seen in this model, the differential inductor pairs are modeled separately and combined with a coupling factor of k_{12}. The total

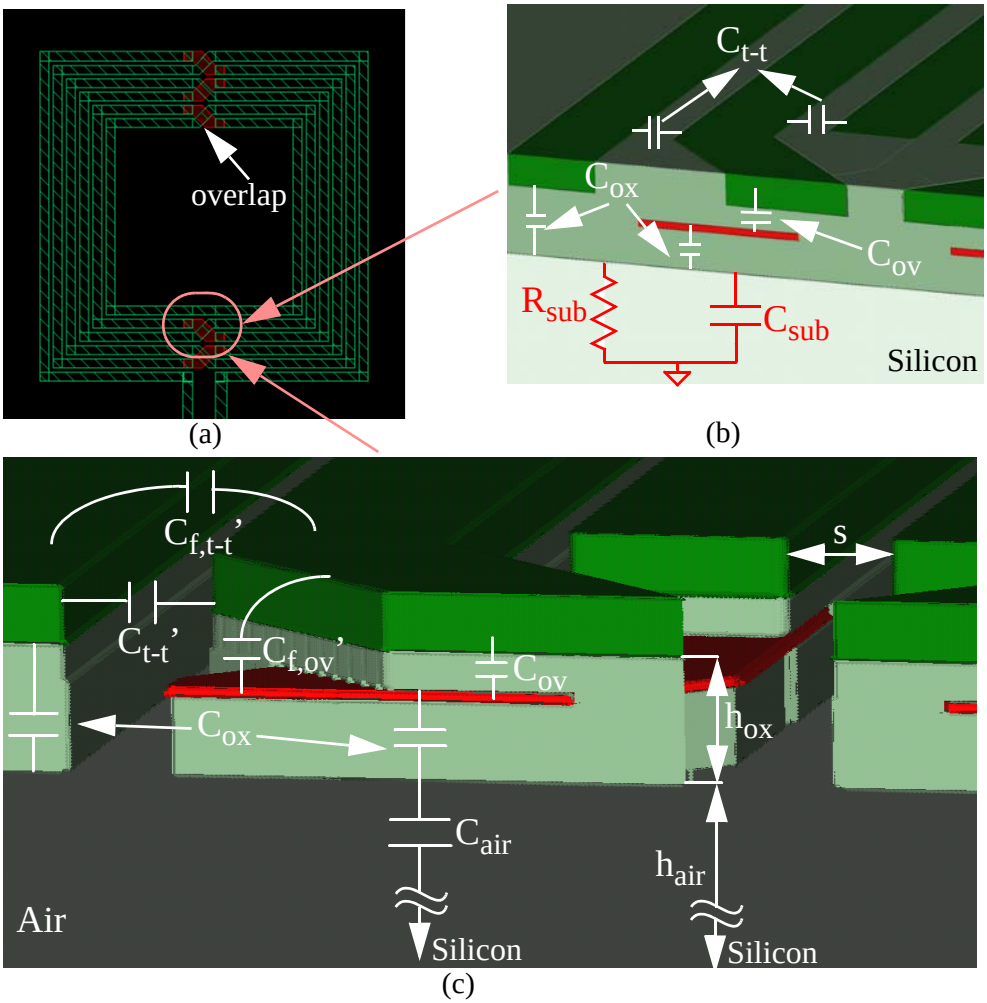


Figure 3-1 (a) Jazz 0.35um Inductor layout (b) inductor after fabrication (c) inductor after release

capacitance between terminals p_1 and p_2 is shown as C_{p12}. In this specific model, the increase in the impedance due to skin and proximity effect is modeled by four parallel groups of series resistors and inductors [20].

Figure 3-1(c) shows the micromachined inductor at the overlapping arms (circle shown in Figure 3-1(a)). As can be seen in this figure, the dielectric between the arms of the inductor and the silicon substrate under whole inductor has been removed. The main changes in the inductor model schematic after release are described step by step below:

- The dielectric capacitance C_{ox} is now in series with the capacitance across the air gap between the suspended inductor and the substrate, C_{air}:

$$C_{air} = \frac{\varepsilon_0 A}{h_{air}} = \frac{\varepsilon_0}{h_{air}}\left(\frac{C_{ox}h_{ox}}{\varepsilon_0\varepsilon_{rox}}\right) = \frac{C_{ox}h_{ox}}{\varepsilon_{rox}h_{air}} \tag{3.1}$$

- The turn-to-turn capacitance reduces by the ratio of relative permittivity of the dielectric, ε_{rox} to relative permittivity of air, $\varepsilon_{r0} = 1$:

$$C_{t-t}' = \frac{C_{t-t}}{\varepsilon_{rox}} \tag{3.2}$$

- The substrate model parameters, R_{sub} and C_{sub}, are short circuited to ground, since C_{air} is too small, making the coupling between inductor arms and substrate negligible.

The micromachined inductor model is shown in Figure 3-3. The oxide capacitance, C_{ox} and air capacitance, C_{air} under the arms of the inductor are in series, hence the total capacitance between the inductor and silicon substrate is given in equation (3.3):

$$C_{ox}' = (C_{ox} \parallel C_{air}) = \frac{C_{ox}C_{air}}{C_{ox} + C_{air}} = \frac{C_{ox}}{\left(1 + \frac{\varepsilon_{rox}h_{air}}{h_{ox}}\right)} \tag{3.3}$$

where h_{air} is the height of the silicon removed during post processing, h_{ox} is the height of the oxide under the arms of the inductor (shown in Figure 3-1(c)) and ε_{rox} is the relative permittivity constant of silicon dioxide used as a dielectric between the metal layers in the CMOS process. The target etch-pit depth or h_{air} is 30 μm. In a typical CMOS process, h_{ox} lies between 5 μm to 15 μm, hence C_{ox}' can be expected nine

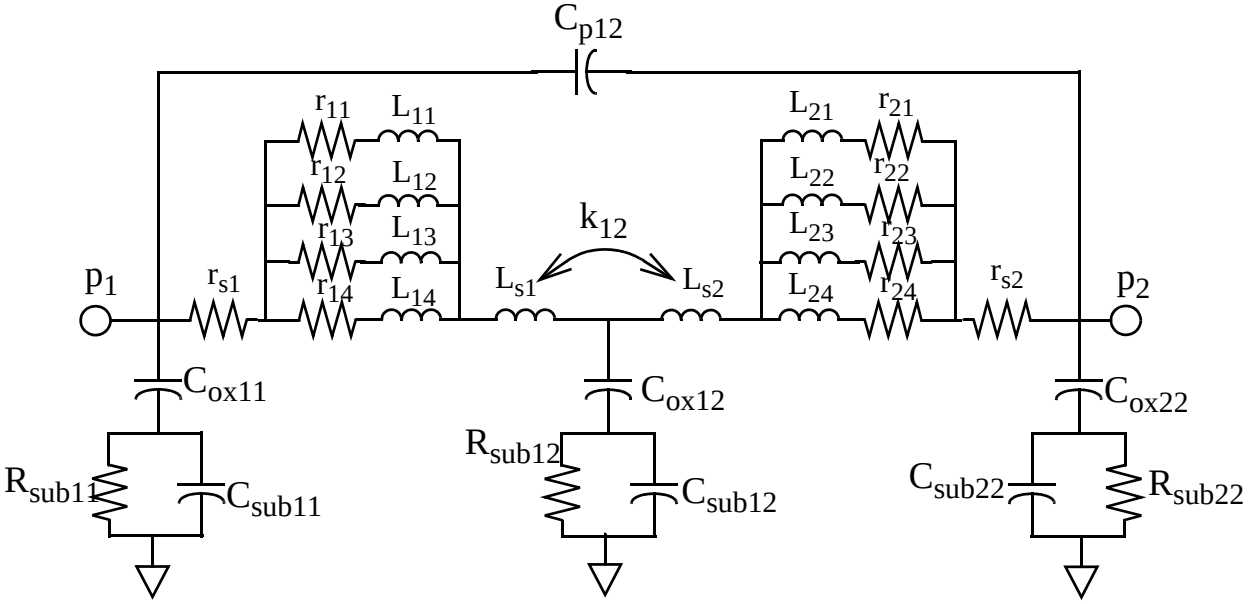


Figure 3-2 The schematic of the fabricated inductor model

to twenty times lower than C_{ox}.These very low values of C_{ox}' results in very high shunt impedance, *i.e.*, very low coupling between the inductor and substrate within the frequency range of interest. The substrate model parameters, R_{sub}' and C_{sub}', for the micromachined inductor should be different than the parameters, R_{sub} and C_{sub}, due to silicon etch. However, it is very difficult to model silicon due to unpredictability in the etching process. Furthermore, because of the low C_{ox}', the substrate model parameters do not change the simulation results. Thus, the substrate model parameters were not modified. Indeed, the substrate model can be replaced with ground without loss of accuracy, as shown in Figure 3-3.

The dielectric etch during post-foundry micromachining also modifies the parasitic capacitance between the terminals of the inductor. As mentioned earlier, the total parasitic capacitance in the foundry inductor model, C_{p12}, is the total of C_{t-t}', C_{ov} and C_f. After micromachining, the turn-to-turn capacitance and total fringing capacitance decreases by ε_{rox}, while the overlap capacitance remain same. In the micromachined inductor model, total parasitic capacitance, C_{p12}', can be calculated as below:

$$C_{p12}' = \frac{C_{p12} - C_{ov}}{\varepsilon_{rox}} + C_{ov},\ C_{ov} = \frac{\varepsilon_0(\varepsilon_{rox}A_{ov})}{t_{M3-M4}}(n-1) \tag{3.4}$$

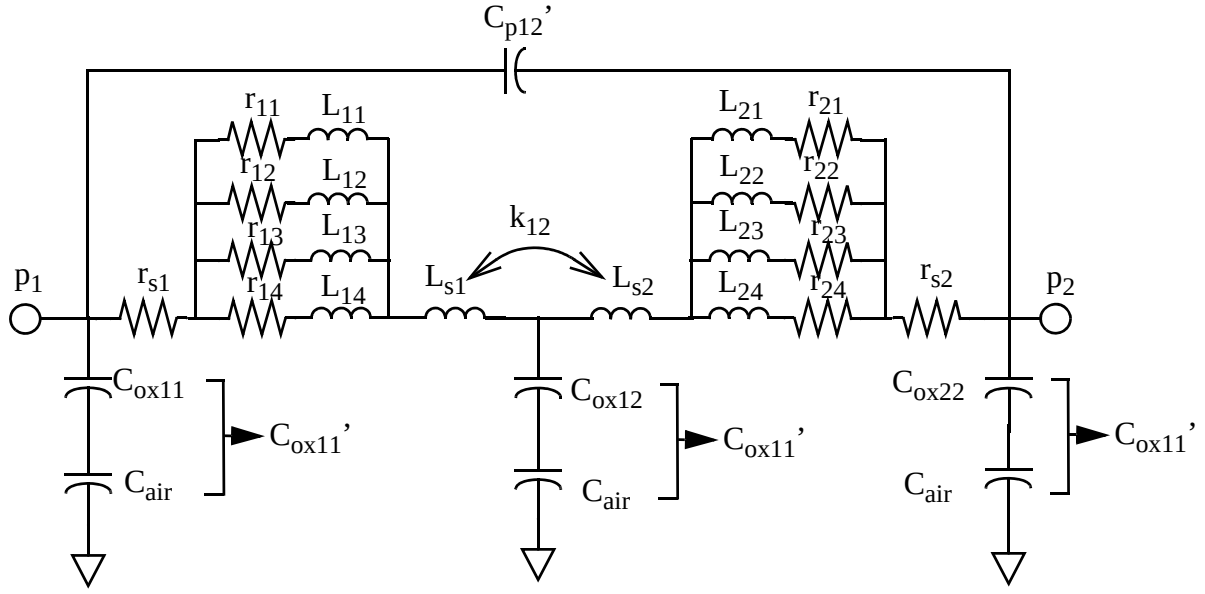


Figure 3-3 The schematic of the micromachined inductor model

where A_{ov} is the area of the overlap between top metal and one lower metal, t_{M3-M4} is the thickness of the oxide between top metal and one lower metal, n is the number of turns (in an n turns differential inductor, there are $n-1$ overlaps). The total fringing capacitance is total of the fringing capacitance between the turns of the inductor, $C_{f,t-t}'$, and fringing capacitance at the overlaps, $C_{f,ov}'$, as shown in Figure 3-1(c). Since the oxide both on and between the turns are etched away, as expressed in (3.4), the total turn-to-turn and fringing capacitances are divided by the relative dielectric constant of oxide, ε_{rox}. In this calculation, the fringing capacitance generating within the oxide is assumed to be zero. The oxide between the layer still exist after the oxide etch, hence the overlap capacitance, C_{ov}, stays same in micromachined inductor model schematic. Since the micromachined inductor model's parasitic capacitance is obtained from the foundry inductor model's parasitic capacitance estimate, the accuracy of the parasitic capacitance in the foundry inductor model strongly affects the accuracy of the parasitic capacitance in the micromachined inductor model.

The foundry provides the model schematic shown in Figure 3-2 where the model component parameters are calculated using the inductor dimensions; in particular, the spacing between the arms of the inductor, s, the number of turns, n, the outer dimension, $0.D$, and the width, w, of the inductor arms. These model component parameters are calculated in using a device callback routine that uses an external executable. The mapping from the foundry model to the micromachined inductor model as encoded in (3.3) and (3.4) are done using equations in the model schematic file. The simulation and measurement details are given in the next section.

3.1.1 Simulation and Measurement Results

In order to test the foundry and micromachined inductor models, 4 nH and 12 nH differential inductors were designed and fabricated in Jazz 0.35um BiCMOS process. The models of the differential inductors were simulated using a circuit simulator, Spectre, and with a finite element continuum solution of Maxwell's equations, HFSS. S-parameter analysis was performed for the inductor with the schematic of the inductor test circuit shown in Figure 3-4(a). With differential excitation, the substrate parasitics have higher

impedance at a given frequency than in the single-ended connection. This reduces the real part and increases the reactive component of the input impedance. The response due to a differential excitation and the input impedance of the differential inductor, Z_d, shown in Figure 3-4(b) can be derived from two port S-parameter analysis using the relationship [21]:

$$S_D = S_{11} - S_{21} \tag{3.5}$$

$$Z_D = Z_{11} + Z_{22} - Z_{12} - Z_{21} = 2Z_0 \frac{1 + S_D}{1 - S_D} \tag{3.6}$$

where Z_0 is the system impedance (50–ohm). In order to extract the inductance, L, and the quality factor, Q, the expressions given below can be used:

$$L = \frac{Im(Z_D)}{2\pi f} \tag{3.7}$$

$$Q_L = \frac{Im(Z_D)}{Re(Z_D)} \tag{3.8}$$

As in the case of the capacitor, the whole device is considered as a pure inductor with series resistance without regarding the parasitic capacitance. Hence, the mapping of the imaginary part of the impedance to inductance in (3.7), implies that L also includes information about the parasitic capacitance. Figure 3-4(c) shows the simplified inductor model when the coupling between the inductor and substrate is negligible. In this case, the input impedance of the inductor model can be written in equation (3.9).

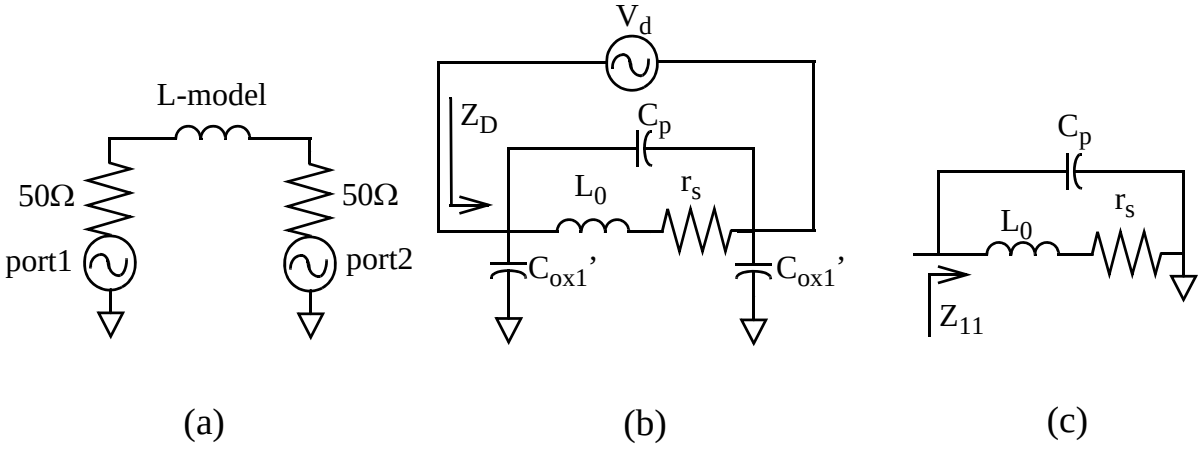


Figure 3-4 (a) S parameter analysis circuit schematic (b) Input impedance of the inductor model (c) input impedance of inductor model (oxide capacitance is neglected) with single-end excitation

$$Im(Z_{11}) = \frac{(1-(2\pi f)^2 L_0 C_p)2\pi f L_0 - 2\pi f r_s^2 C_p}{(1-(2\pi f)^2 L_0 C_p)^2 + (2\pi f)^2 r_s^2 C_p^2} \tag{3.9}$$

According to (3.9) and (3.7), at zero frequency, L is equal to $L_0 - r_s^2 C_p$. If $r_s^2 C_p$ is very small compared to L_0, the inductance at dc is equal to L_0 and self resonance occurs at the frequency of $1/(2\pi\sqrt{L_0 C_p})$. Therefore, L_0 and C_p values can be extracted from the S-parameter simulation response. In order to verify model, the layout of the test inductor is generated for HFSS simulation and two port S-parameter simulation has been performed.Figure 3-5 shows the test inductor generated in HFSS. HFSS simulation steps are described in Appendix B. The inductance and quality factor of the test inductor are extracted as expressed in (3.7) and (3.8). Figure 3-6 shows how inductance and quality factor of the inductor change with frequency in HFSS simulations. The layout generated for HFSS simulations include the vias between metal3 and metal4 as a complete structure, hence the resistance of vias are lower than usual. Therefore, it is expected that the HFSS simulations results give better quality factor than measured quality factor.

As mentioned earlier in this chapter, two test inductors have been designed, fabricated in Jazz 0.35um BiCMOS process and post-processed using ASIMPS post-foundry micromachining process. The top view of the inductors are shown in Figure 3-7 and their dimensions are given in Table 3-1. Two port S parameter measurement of the inductors was performed using an Agilent E8364A Network Analyzer and

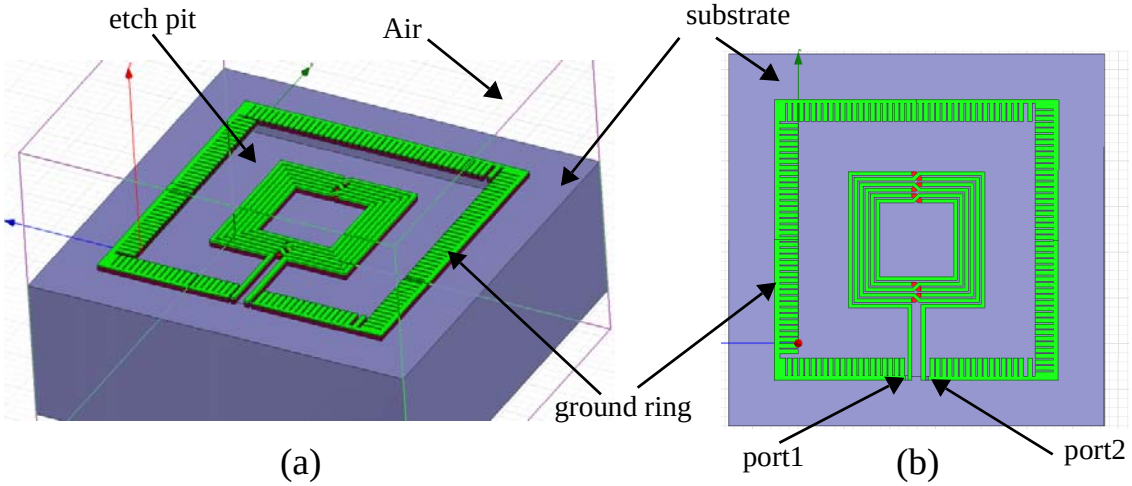
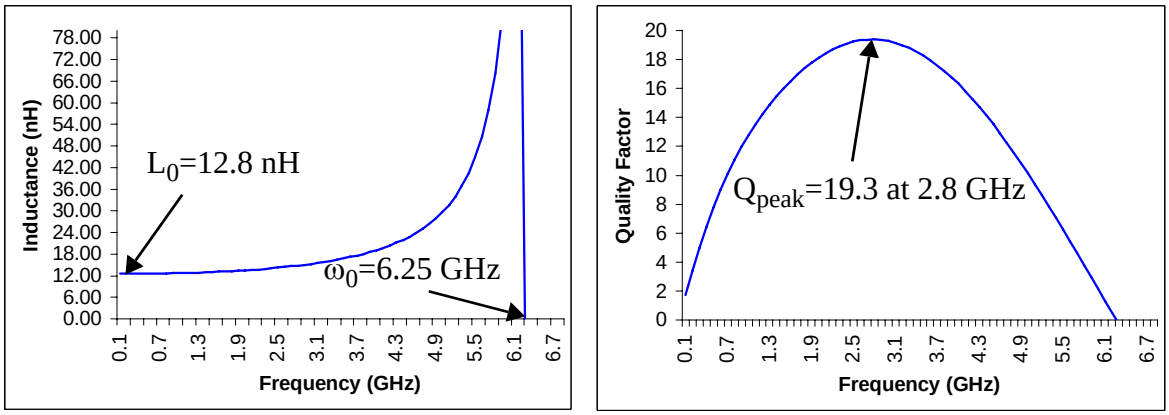


Figure 3-5 (a) The oblique and (b) top view of the 3D inductor layout generated for HFSS two-port S-parameter analysis

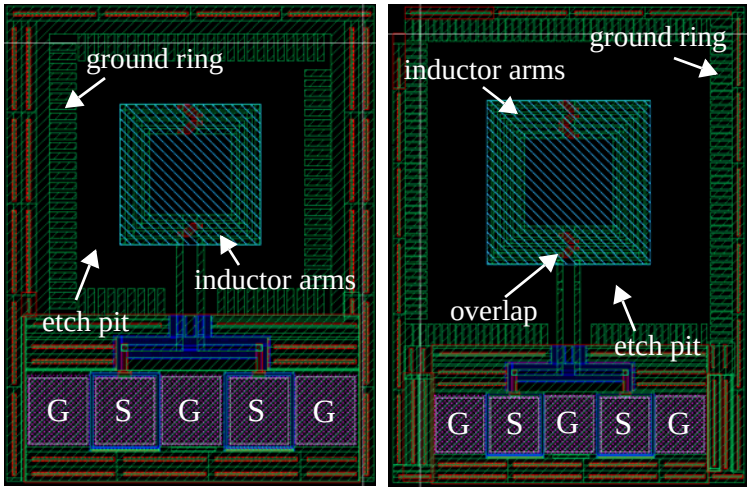


(a) (b)

Figure 3-6 (a) Inductance and (b) Quality factor characteristics results obtained for 12-nH inductor in HFSS S-parameter analysis

Cascade Microtech 6" RF Probe Station with GSGSG probe. Before measurement of the device, the parasitics of the cables and pads are deembedded by using on-chip open-short-load-through (SOLT) calibration pads (steps are given in Appendix C). After obtaining S-parameter responses, the inductance and quality factor characteristics of the inductor were extracted by means of a MATLAB file shown in Appendix C.

The measured and simulated inductance and quality factor graphs of the both 4nH and 12nH differential inductors are shown in Figure 3-8.The simulation results show good matching with the measured



(a) (b)

Figure 3-7 Layout of (a) 4nH test inductor (b) 12nH test inductor with GSGSG pads

Table 3-1. The values and dimensions of the test inductors

L=4nH	L=12nH
n=4	n=6
O.D.=211µm	O.D.=298µm
s=4µm	s=4µm
w=8µm	w=8µm

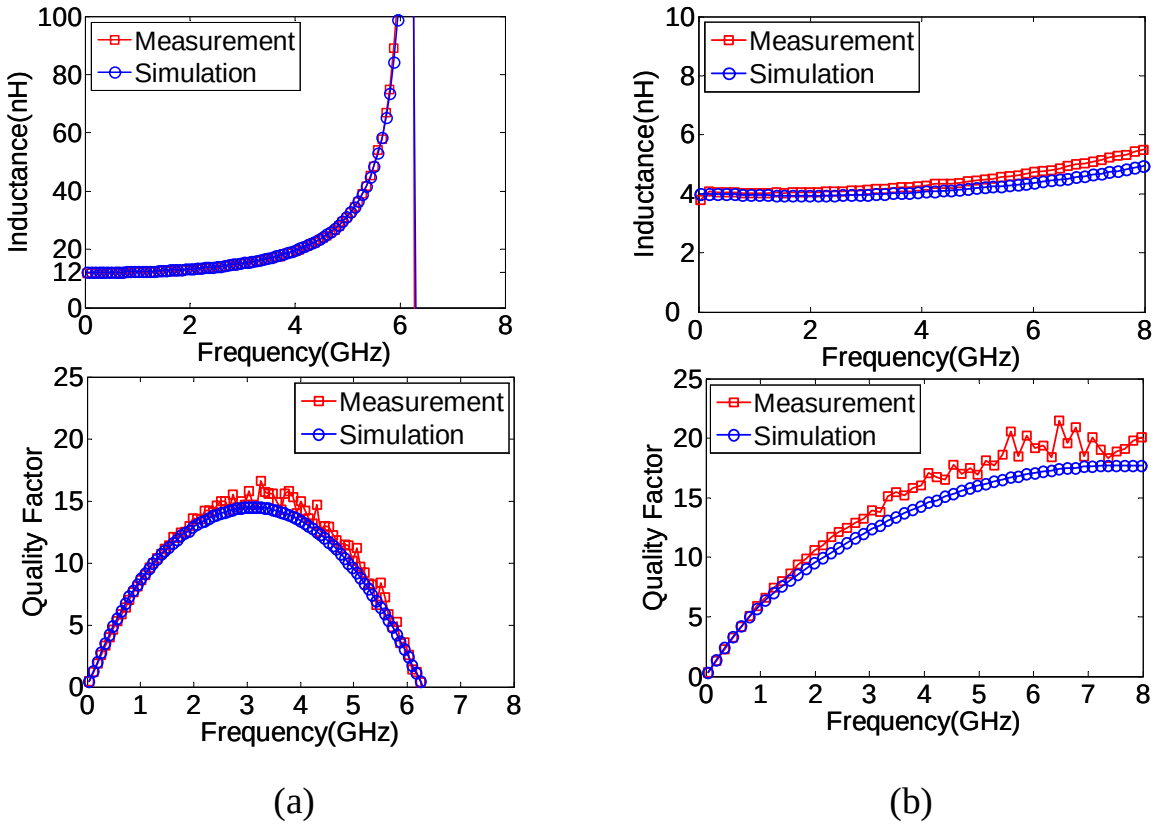


Figure 3-8 Measured inductance and quality factor characteristics of (a) 12 nH inductor (b) 4 nH inductor

results. The extracted inductance and quality factor values from HFSS, Spectre simulations and measurements are shown in Table 3-2. The model of the micromachined inductor predicts the inductance and the parasitic capacitance values accurately, hence as seen in Figure 3-8(a), the inductance values at dc and self resonance frequencies of simulated and measured capacitors match with each other. The small difference between the peak quality factor is caused by small error in the prediction of skin and proximity effect at corresponding frequencies. The self resonance frequency of 4nH inductor is not extracted due to the frequency range of simulation and measurements performed.

Table 3-1. The inductor characteristics extracted from simulation and measurement results for both 4 nH and 12 nH inductors

	12 nH Inductor			4 nH Inductor	
	HFSS	**Spectre**	**Measured**	**Spectre**	**Measured**
L_0	12.8 nH	12.1 nH	11.9 nH	3.99 nH	4.07 nH
ω_0	6.25 GHz	6.19 GHz	6.25 GHz	Not extracted	Not extracted
Q_{peak}	19.3 at 2.8 GHz	14.5 at 3 GHz	16.6 at 3.26 GHz	17.7 at 7.5 GHz	20.1 at 7.2 GHz

3.2 ST7RF Inductor Modeling

Figure 3-9(a) and (b) shows the layouts of the differential foundry inductor with a patterned ground shield (PGS) and the differential MEMS inductor, respectively. PGS used in foundry inductor design is removed to enable the post-processing to release the inductor. However, the model for the foundry inductor is generated assuming that there is a ground shield under the inductor. As with the Jazz inductor, the ST foundry inductor model needs to be modified to incorporate the removal of the PGS and the micromachining effects. The foundry inductor model and the MEMS inductor model schematics are shown in Figure 3-10. The foundry inductor model does not include the turn-to-turn capacitance, overlap capacitance and fringing capacitance between two terminals of the inductor. The main reasons for neglecting the total parasitic capac-

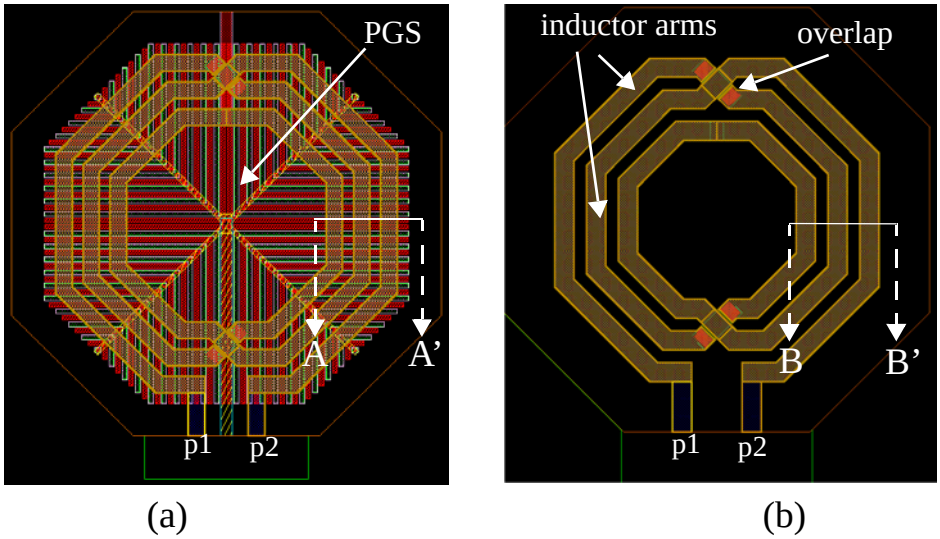


Figure 3-9 Layout of (a) foundry inductor with patterned ground shield (PGS) (b) MEMS inductor (PGS removed)

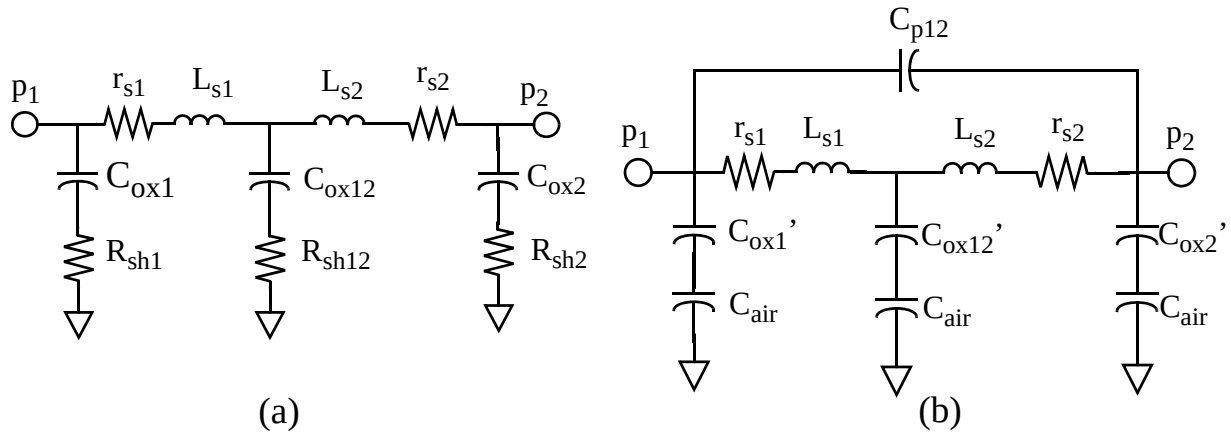


Figure 3-10 Model Schematics of (a) foundry inductor with patterned ground shield (PGS) (b) MEMS inductor (PGS removed)

itance between two terminals of the inductor are the huge capacitance between inductor arms and PGS, and the relatively large spacing between the arms of the inductor. Hence, the main capacitance causing the self resonance is the huge oxide capacitance under the inductor. The oxide capacitances under the inductor are represented as C_{ox1}, C_{ox12} and C_{ox2}, while the shield resistances are shown as R_{sh1}, R_{sh12} and R_{sh2} in Figure 3-10(a).

The modifications for the micromachined inductor model are:

- The oxide capacitance under the inductor is modified to remove the ground shield, C_{ox}', and including the air capacitance, C_{air},
- Since there is no dominant capacitance setting the self-resonance under the inductor after removing PGS, a model of the parasitic capacitance between the terminals of the inductor, C_{p12} is added.

Figure 3-11 shows the cross-section view of the foundry inductor and the MEMS inductor. The fringing capacitance under the inductor arms is neglected, hence the parallel plate oxide capacitance, C_{ox} can be written as in (3.10). As the metal shield is removed, the distance between the bottom of top metal and the surface of silicon substrate becomes $t_{M5-SUB} = h_{ox}$ as shown in Figure 3-11 (a) and (b). Therefore, the modified oxide capacitance can be written as below:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{rox} A_{ind}}{t_{M1-M5}}, \; C_{ox}' = \frac{\varepsilon_0 \varepsilon_{rox} A_{ind}}{h_{ox}} \Rightarrow C_{ox}' = \frac{C_{ox}}{h_{ox}} t_{M1-M5} \tag{3.10}$$

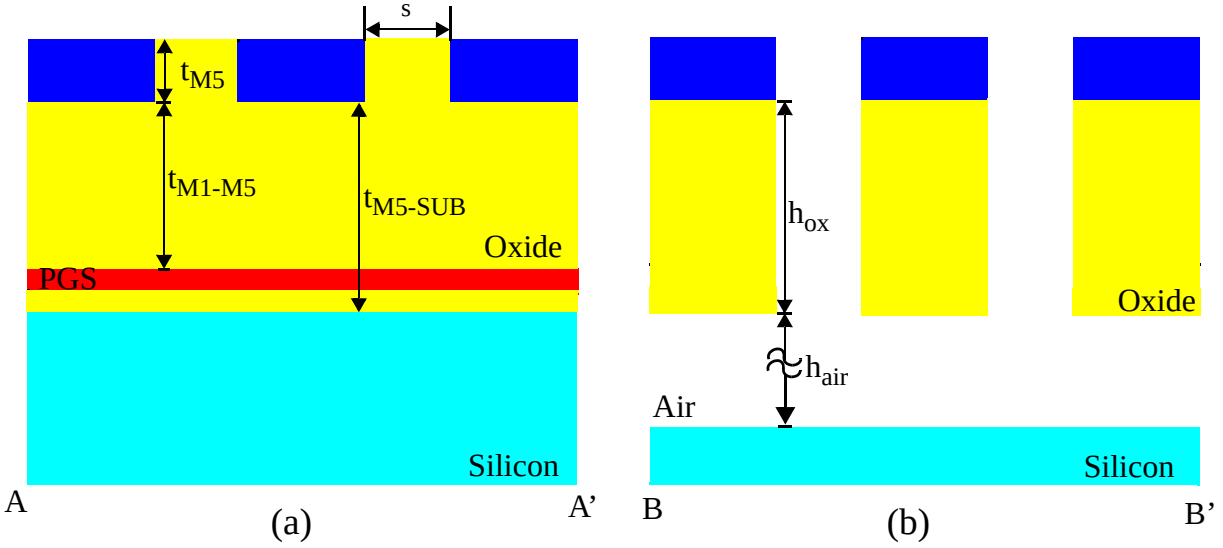


Figure 3-11 Cross-section views of (a) A-A' (b) B-B' shown in Figure 3-9

where A_{ind} is the area under the inductor arms and t_{M1-M5} is the height from top of the shield to the bottom of the top metal. The air capacitance under the inductor arms is given in equation (3.11).

$$C_{air} = \frac{\varepsilon_0 A_{ind}}{h_{air}} = \frac{C_{ox} t_{M1-M5}}{h_{air} \varepsilon_{rox}} \tag{3.11}$$

where h_{air} is the gap between the oxide under the inductor arms and silicon substrate.

After post processing, the oxide capacitance and air capacitance can be combined together and the equivalent capacitance, C_{ox}'' can be written as in (3.12).

$$C_{ox}'' = C_{ox}' \parallel C_{air} = \frac{C_{ox}' C_{air}}{C_{ox}' + C_{air}} = \frac{C_{ox} t_{M1-M5}}{h_{ox} + h_{air} \varepsilon_{rox}} \tag{3.12}$$

where h_{ox} is the oxide height under the inductor arms. As can be seen in Figure 3-10 (b), the substrate model has been neglected due to very low capacitance between inductor arms and the substrate as in the case of Jazz inductor.

The second modification to the foundry inductor model is the capacitance between the terminals of the inductor. While deriving the parasitic capacitance between the terminals, the fringing capacitance can be neglected due to large spacing between the inductor arms, and the overlap capacitance is assumed to be much lower than turn-to-turn capacitance due to low overlap area. Hence the total parasitic capacitance, C_{p12}, is approximated as the turn-to-turn capacitance. The turn-to-turn capacitance, C_{t-t}, can be calculated as below:

$$C_{p12} \cong C_{t-t} = \frac{\varepsilon_0 l_{ind} t_{M5}}{s} \tag{3.13}$$

where t_{M5} is the thickness of top metal, l_{ind} is the length of the inductor and s is the spacing between the inductor arms.

The foundry provides the model schematic shown in Figure 3-10 (a) where the model component parameters are calculated using the inductor dimensions; in particular, the spacing between the arms of the inductor, s, the number of turns, n, the outer dimension, $0.D$, and the width, w, of the inductor arms.

These model component parameters are calculated in using a device callback routine that uses an external executable as in the case for Jazz inductor. The mapping from the foundry model to the micromachined inductor model as encoded in (3.10)-(3.13) are done using equations in the model schematic file. The simulation and measurement details are given in the next section.

3.2.1 Simulation Results

In order to verify the foundry and micromachined inductor models, the two-port S-parameter simulations in HFSS and Spectre have been performed. The layout of a 4 nH inductor in ST Microelectronics 0.25 μm process is generated for HFSS simulations as shown in Figure 3-12. The HFSS simulation steps are given in Appendix B. The two-port S-parameter simulation result is used to extract the inductance and the quality factor of 4nH octagon inductor using the equations (3.7) and (3.8). The extracted inductance and quality factor graphs are shown in Figure 3-13.

As seen in Figure 3-13, the inductance value is 4 nH and quality factor is 42 around 7 GHz. Since the vias in the inductor have been drawn as a complete structure and bigger than reality, the equivalent resistance of the inductor is expected to be lower than one of a micromachined inductor. Hence, the quality factor

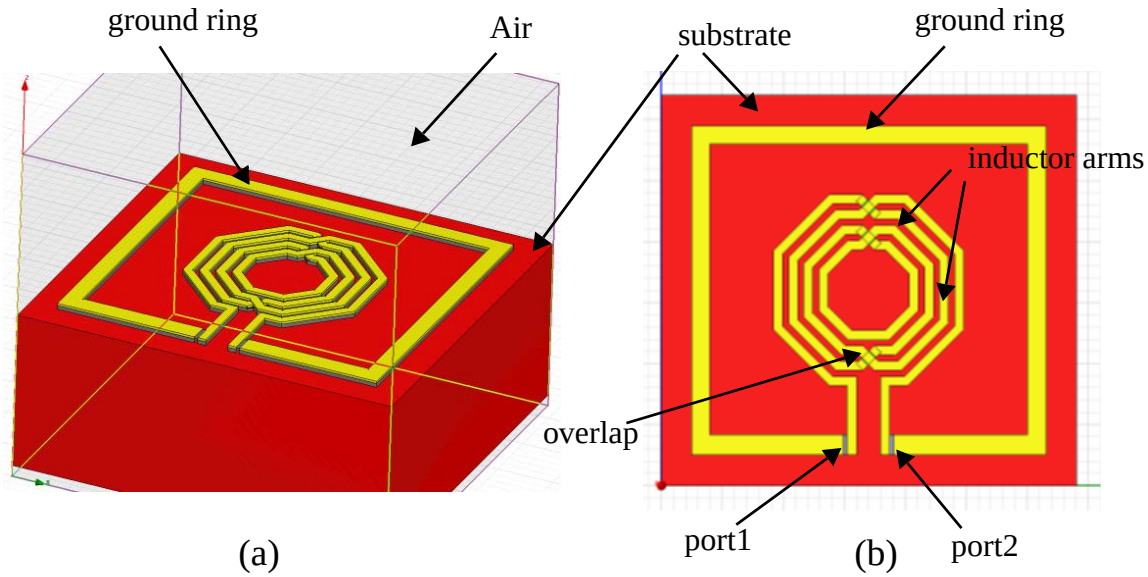


Figure 3-12 (a) Oblique and (b) top view of 4 nH inductor generated in HFSS

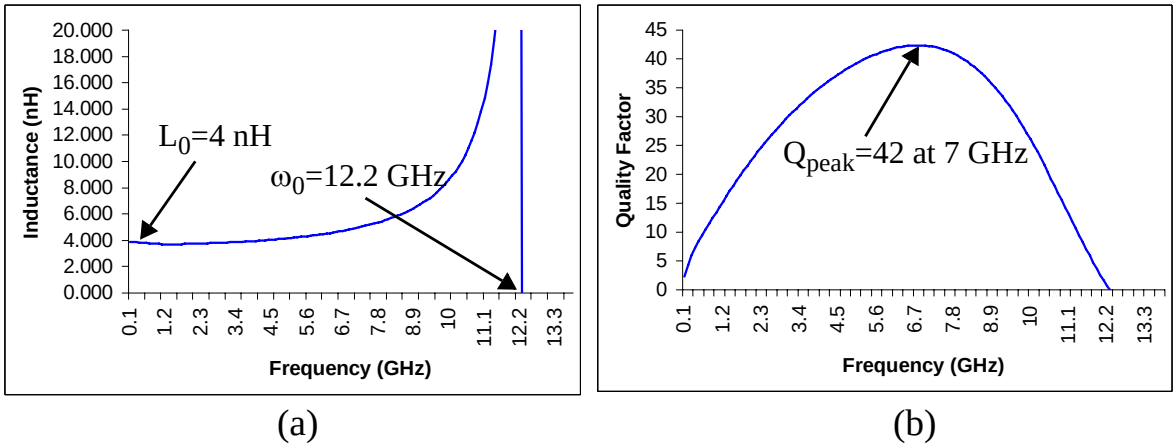


Figure 3-13 (a) Inductance and (b) Quality factor characteristics results obtained for 4 nH inductor in HFSS S-parameter analysis

graph given in Figure 3-13 (b) shows higher values than it is expected in reality. As Figure 3-13 (a) shows, the self resonant frequency of the inductor is 12.2 GHz.

The layout and schematic of 4 nH octagonal inductor test circuit are shown in Figure 3-14. The dimensions of the inductor is given in Table 3-2. Two-port S-parameter analysis has been performed in circuit simulator, Spectre. The S-parameter data is used to extract the inductance and quality factor change with frequency. The extracted inductor characteristics are shown in Figure 3-15.The inductance at dc, L_0, is 4 nH and quality factor is 25 at 5 GHz. The self resonant frequency of the inductor is 11.3 GHz. The

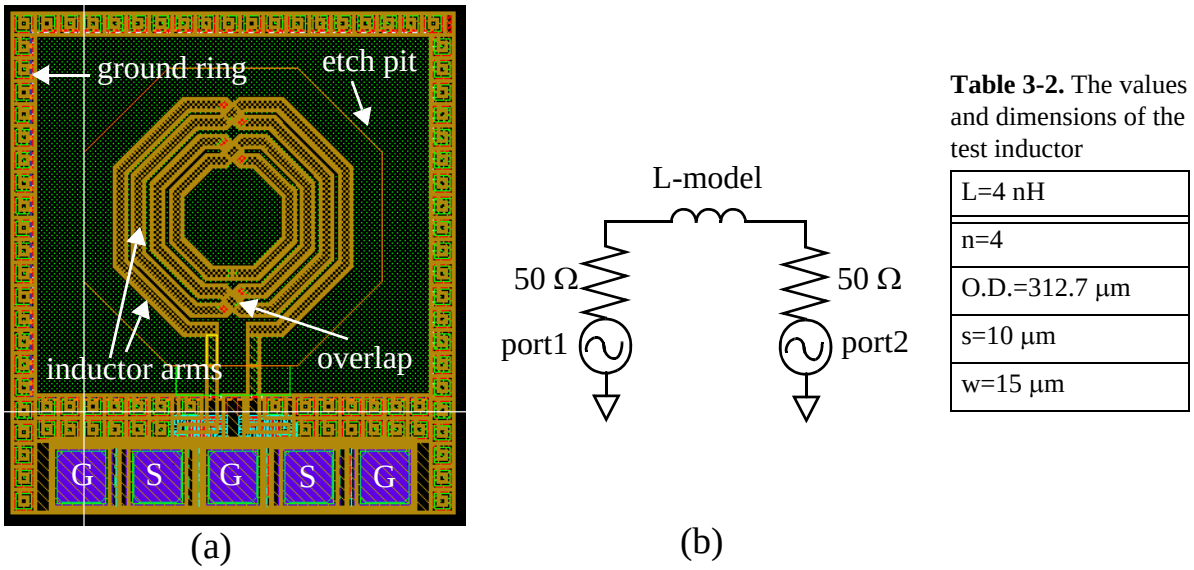


Table 3-2. The values and dimensions of the test inductor

L=4 nH
n=4
O.D.=312.7 μm
s=10 μm
w=15 μm

Figure 3-14 (a) Layout and (b) schematic of 4 nH inductor test circuit

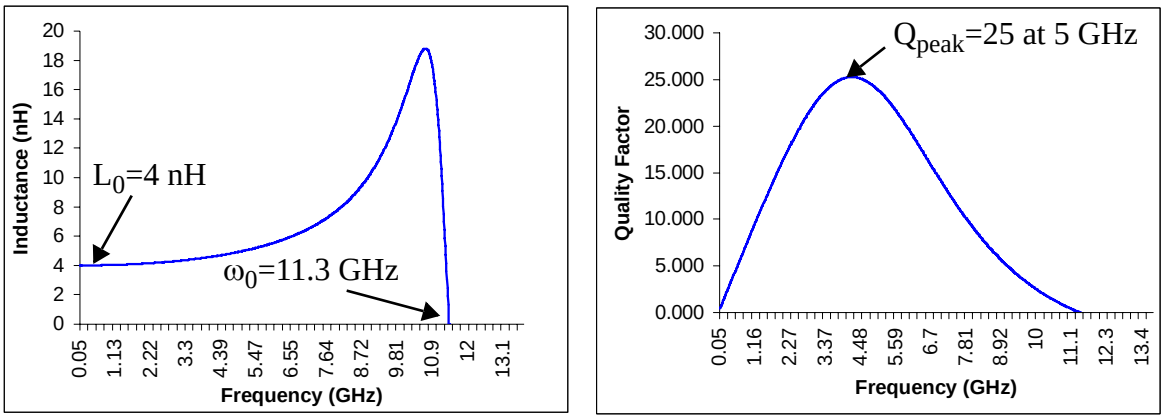


Figure 3-14 (a) Inductance and (b) Quality factor characteristics results obtained for 12-nH inductor in HFSS S-parameter analysis

extracted inductance value matches the value obtained from the HFSS simulations. However, as expected, the quality factor values in Figure 3-14 (b) are lower compared to values extracted from HFSS S-parameter analysis. As mentioned earlier in this section, the main reason for this difference is the layout generated for HFSS has one big via structure at the overlap points, decreasing the equivalent series resistance. As seen in Figure 3-14 (b) and Figure 3-13 (b), the self resonant frequency values are very close for both simulations, hence the parasitic capacitance calculations in the model give consistent value with the HFSS simulations.

3.3 Summary

In this chapter, the models for both foundry and micromachined inductors designed in Jazz 0.35 μm and ST 0.25 μm processes are described. The simulation and measurement results of Jazz inductors show good matching. The inductor models for Jazz 0.25 μm process have been used to generate the first and second generation filter models presented in Chapter 4. The models of ST Microelectronics inductors are used in the design of third generation filter described in Chapter 5.

4 Results of Previously Designed Filters

This chapter validates the models described in Chapter 2 and Chapter 3 by using them to model the capacitors and inductors in two previously designed filters. For this validation, the previously designed filters were measured again to ensure that the proper de-embedding and calibration procedure was followed.

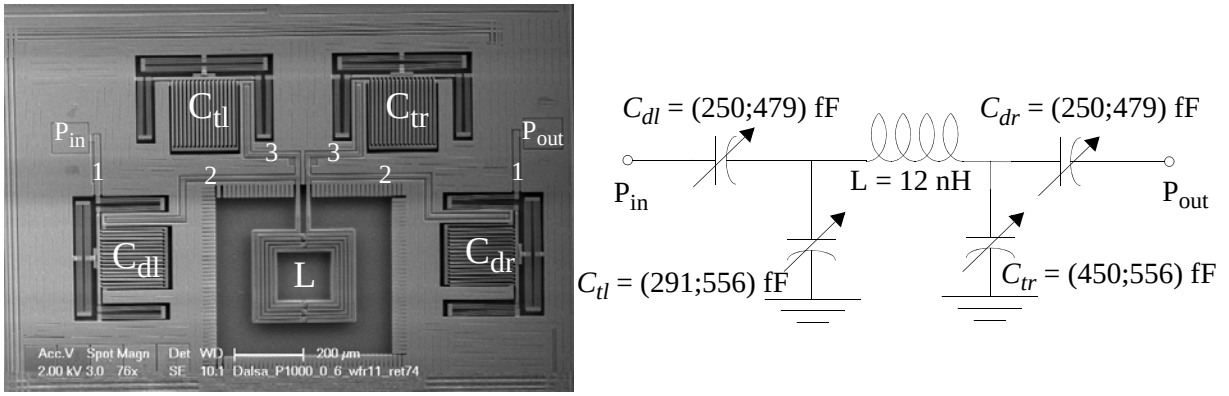
The simulation models for the capacitor and inductor were generated from the layout dimensions of these components. Additionally, the interconnect model described in Chapter 2 was used, parameterized again by the layout dimensions. These models were combined to create the schematic of the whole filter. Two-port S-parameter simulation of the filter schematics were done in circuit simulator, Ansoft Designer.

The measurements of post-processed filter were performed using an Agilent E8364 Network Analyzer and Cascade Microtech 6” RF Probe Station with GSG probes. Short-Open-Load-Through (SOLT) on-chip calibration was performed to eliminate the pad and cable parasitics.

This chapter is partitioned into two sections, one for each of the previously designed filters. In each section, the dimensions, extracted model parameter values, measurement and best fitting simulation results of corresponding filter are described.

4.1 First Generation Filter

The first generation filter is a Butterworth π-network with DC biasing capacitors for -20 dB roll-off at lower frequencies. This filter employs two pairs of CMOS-MEMS tunable capacitors and a single micromachined inductor as shown in the SEM image in Figure 4-1 (a). The schematic of the filter with ideal circuit elements is given in Figure 4-1 (b). The model parameter values of MEMS capacitors and microma-



(a) (b)

Figure 4-1 (a) SEM picture (b) Schematic of π -filter with extracted model parameter values

chined inductors are calculated using the dimensions of tunable MEMS capacitors, micromachined inductor and wiring interconnects (numbers of interconnects are shown in Figure 4-1 (a)) which are given in Table 4-1 (a), Table 4-1 (b) and Table 4-1 (c), respectively. The calculated model parameters of MEMS capacitors and wiring interconnects are given in Table 4-2(a) and Table 4-2(b), respectively. The complete model of filter is generated by combining the MEMS capacitor, micromachined inductors and wiring interconnect models, and simulated in Ansoft Designer. As shown in

Table 4-1. (a) Dimensions of Capacitor in first generation filter

	Cd	**Ct**
lf	187 µm	217 µm
wf	3 µm	3 µm
tf	9.835 µm	9.835 µm
gmin	0.6 µm	0.6 µm
gmax	2.6 µm	2.6 µm
n	16	16
GMD	4 µm	4 µm
b	4	4
lb	180 µm	180 µm
wb	1.5 µm	1.5 µm
lint	320 µm	320 µm
wint	10 µm	10 µm
gint	8 µm	8 µm

Table 4-1. (b) Dimensions of inductor used in first generation filter (L=12nH)

Parameter	**Values**
n	6
Outer Dimension (O.D.)	298 µm
s	4 µm
w	8 µm

Table 4-1. (c) Dimensions of the interconnects shown in Figure 4-1 in first generation filter

	1	**2**	**3**
lint	190 µm	360 µm	130 µm
wint	12 µm	10 µm	10 µm
gint	8 µm	8 µm	8 µm
overlap	4 µm	1 µm	1 µm

Table 4-2. (a) Model parameter values of MEMS capacitors used in first generation filter

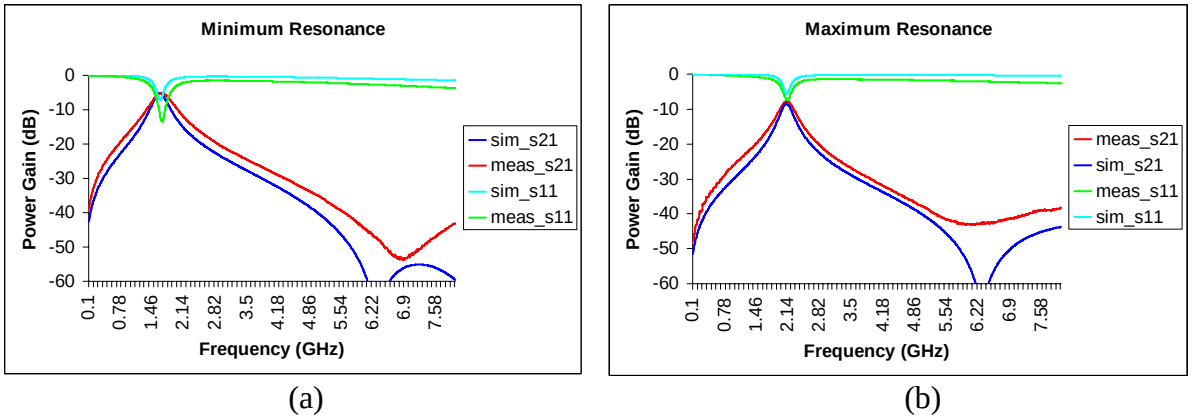
	Cd	Ct
Cmin	250 fF	291 fF
Cmax	479 fF	556 fF
L	576 pH	608 pH
R	1.5 Ω	1.6 Ω
Cgr	37 fF	37 fF
Cox	23 fF	23 fF
Rsub	1500 Ω	1500 Ω

Table 4-2. (b) Model parameter of wiring interconnects in first generation filter

	1	2	3
Lint	143 pH	326 pH	92 pH
Rint	0.16 Ω	0.36 Ω	0.13 Ω
Cgr	27 fF	37 fF	14 fF
Cox	5 fF	19 fF	7 fF
Rsub	1500 Ω	1500 Ω	1500 Ω

the MEMS capacitor model given in Section 2.1.3, the intended capacitance, C, changes with actuation. Hence, in order to match the measurement results of the filter, C of every MEMS capacitor model in the filter is tuned. Figure 4-2 shows best fitting simulation and measurement results for minimum and maximum resonance cases. According to best fitting simulation results demonstrated in Figure 4-2, the extracted capacitance values of MEMS reconfigurable capacitors are shown in Figure 4-1 (b). In this specific chip tested, one of the tank capacitors did not actuate until the minimum capacitance value, hence its minimum value obtained is 450fF as shown in Figure 4-1 (b).

As mentioned in Chapter 2, the substrate resistance value of each interconnect is very difficult to predict due to various locations of the substrate contact around the layout. For simplicity, R_{sub} for all the interconnects are approximated as same, 1500-Ω. Table 4-3 gives the simulation



(a) (b)

Figure 4-2 S_{21} and S_{11} responses of simulation and measurement results for (a) maximum and (b) minimum resonance cases

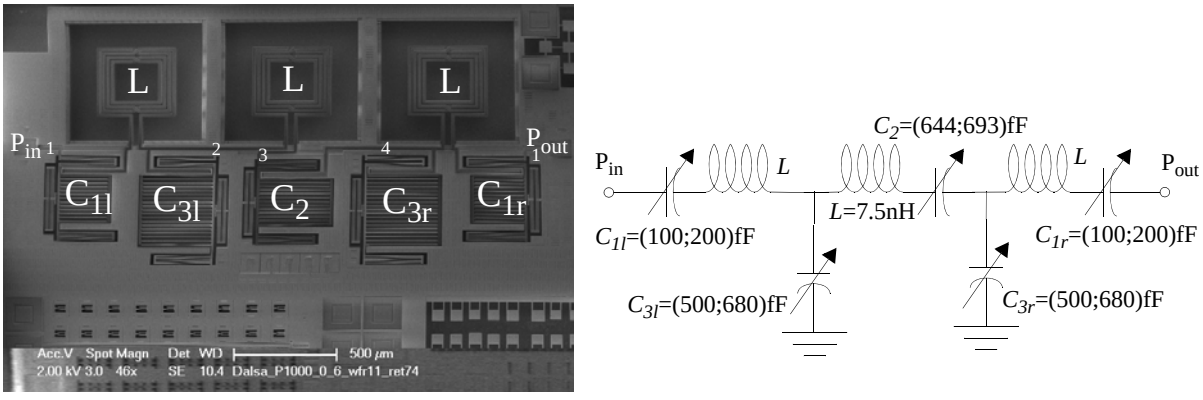
Table 4-3. Simulation and measurement results comparison of first generation filter

Minimum Resonance Frequency		**Maximum Resonance Frequency**	
Simulation Results	Measurement Results	Simulation Results	Measurement Results
w0=1.72 GHz	w0=1.66 GHz	w0=2.11 GHz	w0=2.13 GHz
IL=5.62dB	IL=5.24 dB	IL=8.5 dB	IL=7.78 dB
-3dB BW= 300M	-3dB BW= 450 MHz	-3dB BW= 280 MHz	-3dB BW= 360 MHz

and measurement results comparison for the first generation filter. As seen in Table 4-3, the best fitting simulation results have bigger quality factor than the measurement result. This is expected since the quality factors of models created for MEMS capacitor and micromachined inductors have slightly higher than the actual quality factors as was seen from the comparison presented in Chapter 2and Chapter 3, respectively.

4.2 Second Generation Filter

Second generation filter topology is capacitively-coupled series resonator filter in which three series LC resonators are coupled by two shunt capacitors. This filter topology is feasible for high frequency design in terms of the capacitance values which MEMS capacitor can have. Figure 4-3 shows the layout and the schematic of the capacitively-coupled series resonator filter with extracted model parameter values. The layout dimensions of MEMS capacitors, inductors and wiring interconnects are given in Table 4-4 (a), Table 4-4 (b) and Table 4-4 (c) and the model parameter values of MEMS capacitor and interconnects



(a) (b)

Figure 4-3 (a) SEM picture (b) Schematic of coupled resonator filter with extracted model parameter values

Table 4-4. (a) Dimensions of MEMS capacitors in second generation filter

	C1	C2	C3
lf	247 μm	357 μm	357 μm
wf	4 μm	4 μm	4 μm
tf	9.835 μm	9.835 μm	9.835 μm
gmin	0.6 μm	0.6 μm	0.6 μm
gmax	6.6 μm	6.6 μm	6.6 μm
n	12	12	16
GMD	5 μm	5 μm	5 μm
b	4	4	4
lb	280 μm	280 μm	280 μm
wb	2.6 μm	2.6 μm	2.6 μm
lint	440 μm	440 μm	440 μm
wint	10 μm	10 μm	10 μm
gint	9 μm	9 μm	9 μm

Table 4-4. (b) Dimensions of inductor used in second generation filter (L=7.5 nH)

Parameter	**Values**
n	4
Outer Dimension (O.D.)	400 μm
s	10 μm
w	14 μm

Table 4-4. (c) Dimensions of the interconnects shown in Figure 4-3 in second generation filter

	1	2	3	4
lint	100 μm	746 μm	220 μm	610 μm
wint	10 μm	10 μm	10 μm	10 μm
gint	10 μm	10 μm	10 μm	10 μm
overlap	1 μm	1 μm	1 μm	1 μm

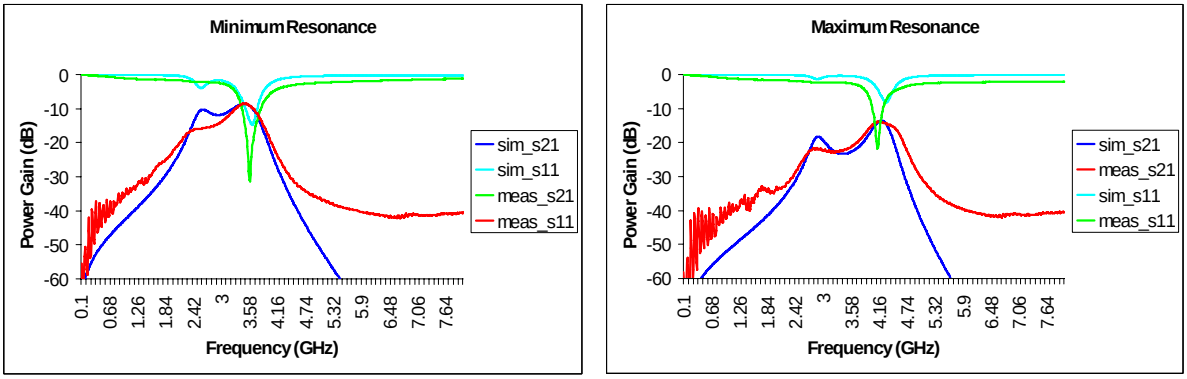
shown in Figure 4-3 (a) are given in Table 4-5(a) and Table 4-5(b). These model parameter values are obtained from the scripts described in Appendix A.2.5. As described for the first generation filter, the model for the second generation filter has been derived by combining the models of MEMS capacitors, micromachined inductors and wiring interconnects. The S-parameter simulation of the filter is performed in Ansoft designer. Figure 4-4 shows the measurement results and best fitting model simulation results of the second generation filter. In the second generation filter, the substrate contacts were placed closer to the interconnects, hence substrate resistance, R_{sub}, values for the interconnects are calculated as 20 Ω.

Table 4-5. (a) Model parameter values of MEMS capacitors used in first generation filter

	C1	C2	C3
Cmin	128 fF	185 fF	247 fF
Cmax	479 fF	692 fF	923 fF
L	795 pH	930 pH	917 pH
R	1.7 Ω	2 Ω	2 Ω
Cgr	46 fF	46 fF	46 fF
Cox	29 fF	29 fF	29 fF
Rsub	20 Ω	20 Ω	20 Ω

Table 4-5. (b) Model parameter of wiring interconnects in first generation filter

	1	2	3	4
Lint	65 pH	785 pH	178 pH	617 pH
Rint	0.1 Ω	0.75 Ω	0.22 Ω	0.61 Ω
Cgr	11 fF	77 fF	23 fF	63 fF
Cox	5 fF	40 fF	12 fF	32 fF
Rsub	20 Ω	20 Ω	20 Ω	20 Ω



(a) (b)

Figure 4-4 S_{21} and S_{11} responses of simulation and measurement results for (a) maximum and (b) minimum resonance cases

The extracted values of C1 given in Figure 4-3 are smaller than the model parameter values shown in Table 4-5. The reason for this difference is mainly the vertical and lateral curling of the interdigitated beams, which are not included as modeling parameters in Chapter 2, which were seen in this capacitor in the specific chip tested. As many MEMS structures are used on the same filter design, matching is seen as an emerging design issue. As the number of MEMS capacitors and micromachined inductors increases, the size of the filter gets bigger, and mismatch of components affects the fitting of simulation and measured results. The main reason for the mismatch of the measurement and best fitting curves at high frequencies is inaccurate modeling of inductors. As seen in Figure 4-4, although the resonant frequencies of the filter is fitted by model values, the lower peak insertion loss has difference for fitted and measured results. The reason for this difference is mismatch of the MEMS capacitors, $C1l$ and $C1r$, shown in Figure 4-3 (b).

4.3 Summary

In this chapter, the MEMS capacitor, micromachined inductor and wiring interconnect models were verified by modeling the previously designed filters. The modeling and design experience gained from these filters helped a better understanding of design issues such as topology choice and parasitic effects in RF-MEMS reconfigurable LC based filter design.

5 3rd Generation Filter Design

The third generation filter design is a RF pre-select filter that aims to meet many of the spectral specifications for the UWB communication standard, as they are feasible given the quality factor and tuning range characteristics of the MEMS L and C described in the previous chapters. Figure 5-1 shows the mandatory lower 3 bands in the Multi-Band Orthogonal frequency division multiplexing Alliance (MBOA) UWB frequency band and FCC spectral mask requirements [22]. The complete specifications of the new filter design are given in the following section.

5.1 Filter Design Specifications

5.1.1 Insertion Loss (IL)

IL of the front end filter should be as low as possible to minimize the overall receiver noise figure, however the bandwidth-insertion loss trade-off in every filter [23] causes IL increase as quality factor of the filter increases. Hence, the worst case IL needs to be **4 dB**

5.1.2 Bandwidth (BW) and Resonant Frequencies (ω_0)

BW of the three frequency bands between 3.1 GHz and 4.8 GHz needs to be **528 MHz**, and the **resonant frequencies** for the three frequency bands need to be **3.43 GHz**, **3.96 GHz** and **4.49 GHz**, consequtively.

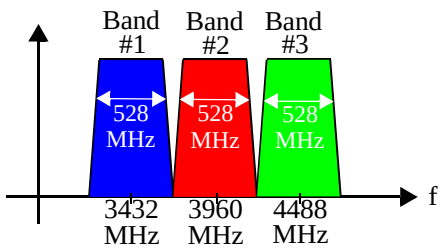


Figure 5-1 The first three frequency bands of the MBOA UWB spectral standard

5.1.3 Quality Factor

According to bandwidths and resonant frequencies of the filter, **the quality factor** of the filter needs to tune between **6.8, 7.8 and 8.8** which are achievable by the MEMS components.

5.1.4 Selectivity

The selectivity specification is left **undefined.** The attenuation of the out-of-band signals should be as much as possible, in order to increase the shape factor. However, this requires higher order filters increasing the number of MEMS capacitors and inductors as well as IL. Therefore, the selectivity is maximized within the constraints of IL and Q-factor specifications.

5.1.5 Switching time

For the scope of this thesis, switching time from one band to another is **undefined**. The switching time will be set by the thermal time constants of the electrothermal actuators used to tune the capacitors (typically on the order of milliseconds). The UWB standard requires 9.2 ns frequency band switching time. However, other standards, such as WiMAX, that require subsequent channel filtering after the RF pre-select filter, don't have such a stringent restriction on switching time for the pre-select filter.

5.2 Design

5.2.1 Topology

The topology of the filter was selected from the experience derived from the previously designed filters and the range of achievable component values and Q-factors of MEMS capacitors and inductors. MEMS capacitors can have values in the range of between 100 fF and 1 pF, while on-chip spiral inductors can have values between 1 nH and 15 nH. In order to understand the main trade-offs in RF-MEMS reconfigurable filter design, we consider a series RLC circuit to be a bandpass filter as shown in Figure 5-2. The loaded quality factor (Q-factor) of such as circuit is equal to $(\omega_0 L)/R_{total}$ or $1/(\omega_0 R_{total} C)$ where R_{total} is equal to $R + R_L + R_G$ [25]. With number of series resonators increases, while the equivalent

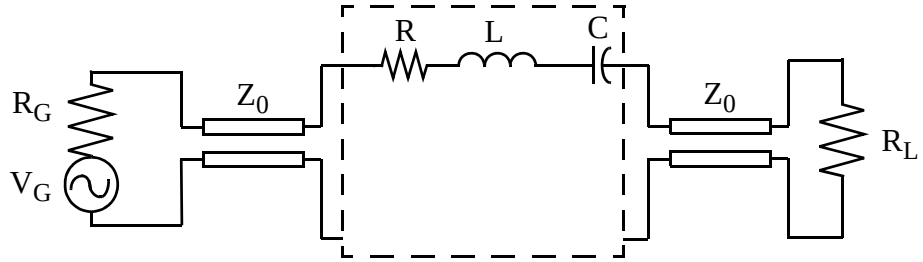


Figure 5-2 Representation of filter as a series RLC network

inductance increases and equivalent capacitance decreases. Hence, if number of series resonators increases, loaded Q-factor of the filter will increase. However, as the inductance increases, in order to get high resonant frequency ($\omega_0 = 1/(\sqrt{LC})$), the capacitance value needs to decrease. As mentioned above, MEMS capacitors have a constraint on the minimum achievable capacitance. Hence, as the resonant frequency of an MEMS LC resonator increases, the quality factor needs to decrease.

The first generation filter used a second order π-network with only one inductor. It led to low IL, however the resonant frequencies are low. The second generation filter used a sixth order capacitively coupled series resonator topology. This is a good topology for high frequency due to low achievable equal capacitance values. However usage of three inductors increased the IL and decreased the quality factor of the filter.

After studying these trade-offs, fourth order capacitively-coupled series resonator topology has been chosen as the new filter design to achieve the specifications described in Section 5.1. The schematic of the new filter design with ideal circuit elements is shown in Figure 5-3. The main reason to choose capacitive coupling is that on-chip capacitors have higher quality factors than on-chip inductors. In order to keep overall filter quality factor high, the number of the on-chips inductors is kept minimum. Thus only two inductors are needed in the two series LC resonators, leading to lower IL.

In addition to considering the MEMS capacitor and inductor as primary design components (as in the designs described in Chapter 4), this design also considers the interconnects as a primary design com-

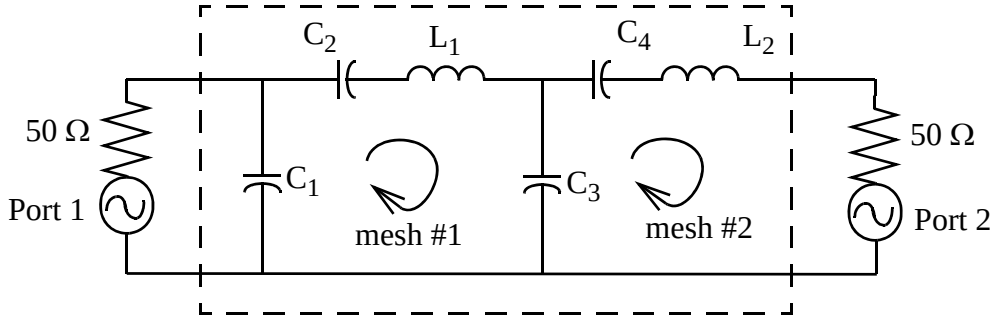


Figure 5-3 The schematic of the filter with ports

ponent. Additionally, this design procedure used the capacitor model described in Chapter 2 and the inductor model in Chapter 3. The interconnect design and model used in third generation filter is presented in Section 5.2.5.2. The design steps of the RF-MEMS reconfigurable LC-based filter are shown in the flowchart given in Figure 5-4. The next few subsections describes each of the steps in the flowchart.

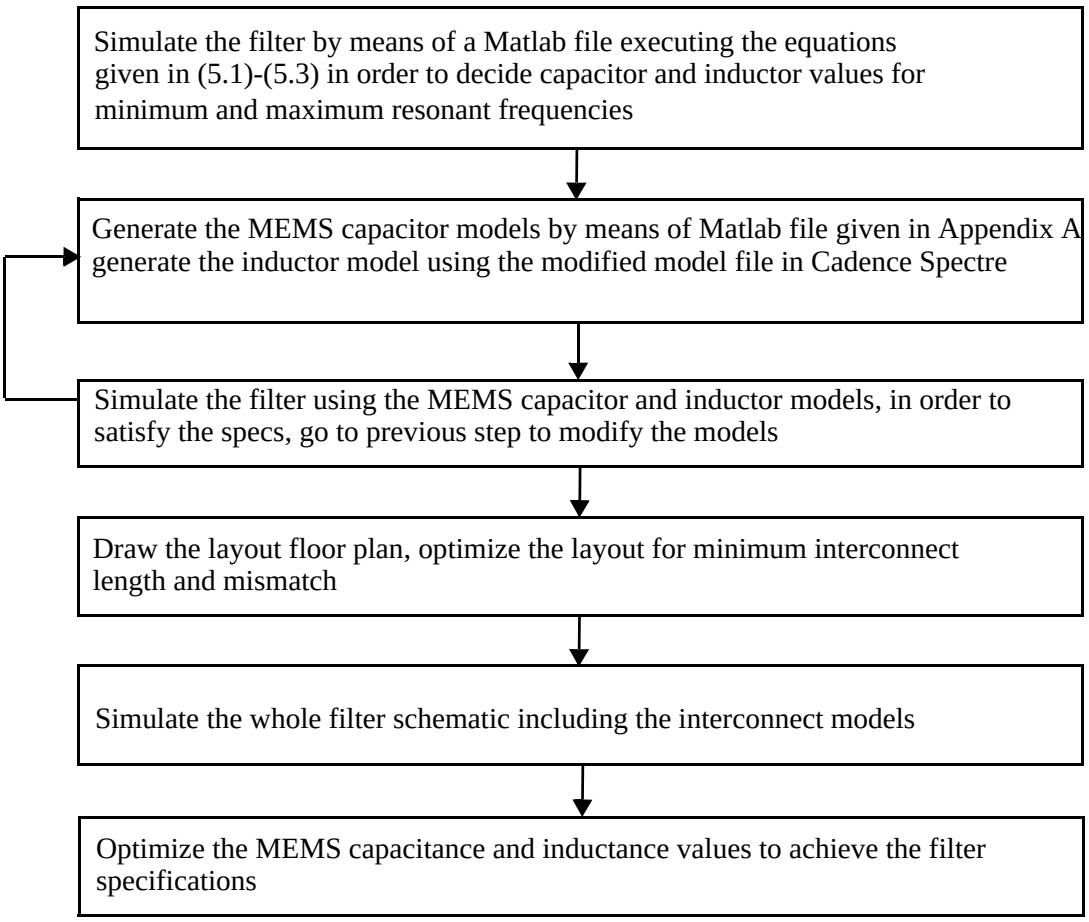


Figure 5-4 The design flow of the filter

5.2.2 Design with Ideal Components

In the design of the capacitively-coupled resonator filter, the main assumption is the coupling impedance, which is $1/(jwC)$, does not change with the frequency [24]. However, the impedance of a capacitor decreases as the frequency increases. In order to approach this assumption, the coupling capacitance should be increased. Hence, the slope of impedance decrease with frequency will be smaller but not zero anytime. In a capacitively coupled series resonator filter, if the coupling capacitance value is low, then the resonator poles split, deforming the shape of the filter and decreasing the quality factor.

As can be seen in Figure 5-3, the filter has four poles occurring due to two series LC resonators. In order to locate these poles at the same resonant frequency, the resonant frequencies of mesh1 and mesh2 shown in Figure 5-3, stated below in equation (5.1), should be same. The equivalent capacitance of mesh1 and mesh2 are given in (5.2) and (5.3), respectively.

$$\omega_{0_{mesh1}} = \omega_{0_{mesh2}} = \frac{1}{\sqrt{L_1 C_{mesh1}}} = \frac{1}{\sqrt{L_2 C_{mesh2}}} \tag{5.1}$$

$$C_{mesh1} = (C_1 \parallel C_2 \parallel C_3) = \frac{C_1 C_2 C_3}{C_1 C_2 + C_1 C_3 + C_2 C_3} \tag{5.2}$$

$$C_{mesh2} = (C_3 \parallel C_4) = \frac{C_3 C_4}{C_3 + C_4} \tag{5.3}$$

While starting the design of the filter with ideal components, the resonant frequency specifications have been revised. Considering the possible lateral and vertical curling of interdigitated beams which can cause an amount of variance in the minimum and maximum values of the MEMS capacitor, the design of the filter is done for 3GHz and 4.8GHz, with a 10% extended band than the performance specifications given in Section 5.1.2. The design procedure of the filter with ideal components is given below step by step:

1. In order to get a higher inductance value, start from the design for maximum resonant frequency, which is 4.8GHz,
2. Choose a realistic coupling capacitance value, C_1 and C_3, high enough for high quality factor considering the MEMS capacitance values range and area, $C_1 = C_3 = 2pF$

3. For matching, the capacitors should all be made out of unit cells, so integer ratios between C_2, C_4 and C_1, C_3 is selected as: $C_2 = C_4 = C_1/6 = C_3/6$,
4. Calculate the values of C_{mesh1} and C_{mesh2} using (5.2) and (5.3), and calculate the values of L_1 and L_2 using (5.1),
5. Then, design the filter for minimum resonant case with the inductance values found in step 4,
6. Increase the coupling capacitance value (while being within the range achievable by the on-off ratios for the MEMS capacitor) to decrease the resonant frequency, $C_1 = C_3 = 2.8pF$,
7. Decrease the ratio between resonator capacitance values and coupling capacitance values, hence $C_2 = C_4 = C_1/3 = C_3/3$,

A matlab script file, described in Appendix C, was used to perform the steps described above. This code outputs the resonant frequency, bandwidth, and quality factor of the filter from the design parameter inputs (the coupling capacitance values described in steps 2 and 5). The values of ideal components for both minimum and maximum resonant cases are given in Table 5-1. It should be mentioned that the coupling capacitance values, 2pF and 2.8pF, are out of the range that a MEMS capacitor can take. However, these capacitance values can be created by combining two or three MEMS capacitors in parallel.

Figure 5-5 shows the filter test bench schematic when the second port is terminated with 50 Ω. In the code, S_{21} response is derived using the expressions below for $R_G = R_L = 50\Omega$ [25]:

$$S_{21} = \frac{2V_2}{V_G} = \frac{2R_L}{R_L + Z_{out}} \tag{5.4}$$

In order to find Z_{out} in Figure 5-5, the signal source is short-circuited and the equation of Z_{out} is put into (5.4) to derive the transmission gain. The complex variable computation was done in Mathematica, the code and whole transfer function is given in Appendix C.2. As seen in transfer function, the filter has

Table 5-1. Filter characteristics and ideal component values

	Maximum Resonance	**Minimum Resonance**
C1	1.8 pF	2.8 pF
C2	305 fF	933 fF
C3	2 pF	2.8 pF
C4	342 fF	933 fF
L1	4.7 nH	4.7 nH
L2	3.77 nH	3.77 nH

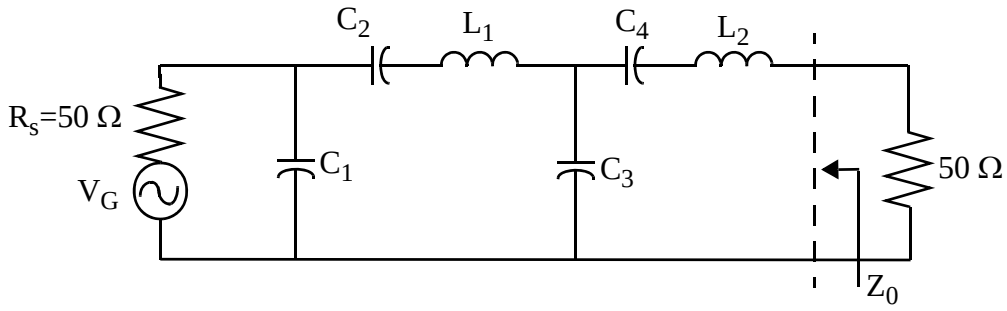


Figure 5-5 The filter schematic terminated with 50-ohm

one zero at dc caused by the capacitors between input and output, and it has five poles, four of them are caused by series resonators, and one of them is caused by R_s and C_1. Figure 5-6 and Table 5-2 shows the minimum and maximum resonance frequency characteristics obtained by the simulation using the ideal components. As shown in design procedure (Figure 5-4), after deciding the minimum and maximum values of capacitor should take, the design of the individual devices must take place. The following sections explain how MEMS capacitor, inductor and interconnects have been designed.

5.2.3 Design of MEMS Capacitor

As can be seen in Table 5-1, the capacitors can take a minimum capacitance value of 300 fF and a maximum capacitance value of 933 fF. The coupling capacitance values of C_1 and C_3 can be generated by combining several MEMS capacitors. For matching and for simplicity in the design, only one type of

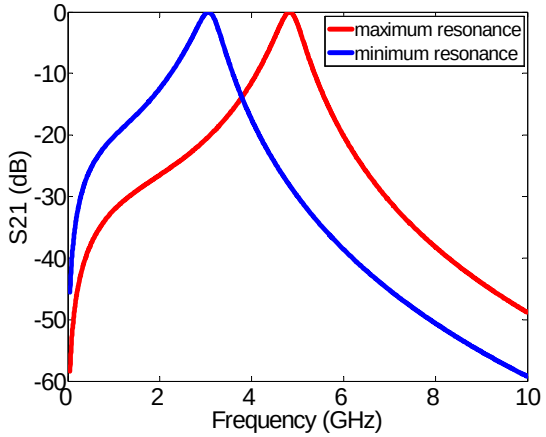


Table 5-2. Filter characteristics obtained by the simulations with ideal components

	Maximum Resonance	**Minimum Resonance**
Resonance Frequency (ω_0)	4.825 GHz	3.059 GHz
Bandwidth (BW)	474 MHz	501 MHz
Quality Factor (Q)	10.2	6.1

Figure 5-6 The filter frequency response of simulation with ideal components

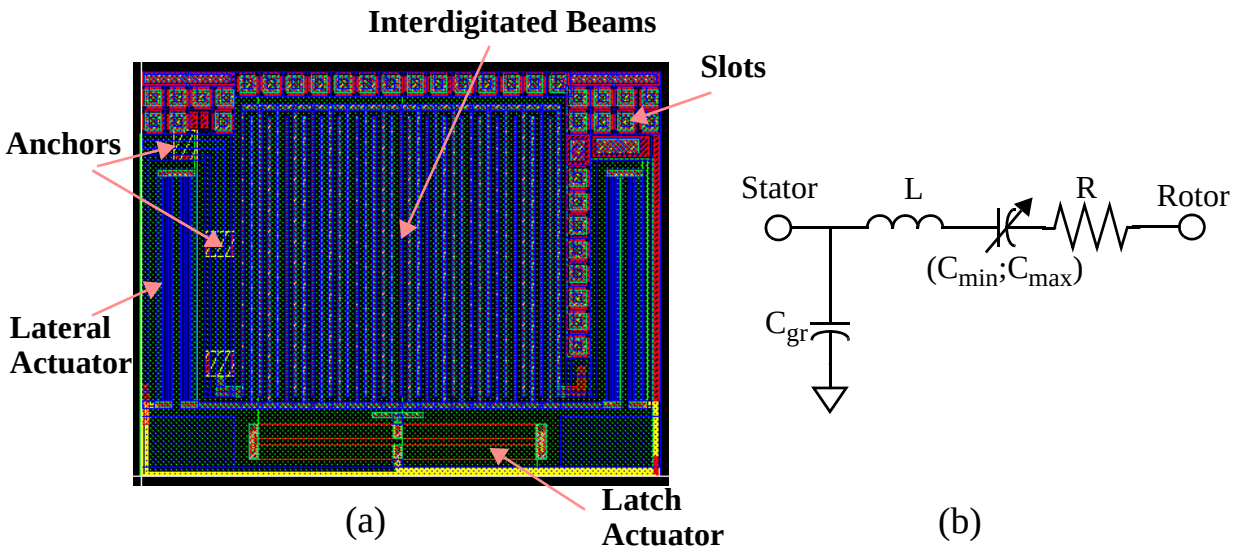


Figure 5-7 (a) The layout and (b) model schematic of MEMS capacitor

capacitor is used in the whole filter. Based on experience from capacitor test structures that were designed by Altug Oz [13] the stator interconnect of the MEMS capacitor was re-designed to reduce the effect of parasitics. The new design of stator interconnect will be discussed in Section 5.2.5.1, with the rest of the interconnect discussion. The layout and model of the new MEMS capacitor is shown in Figure 5-7.(a) and (b), respectively.

In the figure, C_{min} and C_{max} design parameters have already been decided in the previous section. The design of the MEMS capacitor is done by means of a MATLAB file (see Appendix A) which calculates the design parameters according to (2.1)-(2.4). In order to design the MEMS capacitor in ST Microelectronics 0.25 υm BiCMOS process, the process parameters within the code shown in Appendix are modified as shown in Table 5-2. The design of the actuators is identical to those in the capacitors used in the second generation filter. The dimensions of the MEMS capacitors is set to satisfy the required tuning range and to minimize parasitics for higher capacitor quality factor.

5.2.4 Design of MEMS Inductor

The foundry provides two types of inductors, single-ended and differential inductors. The differential inductors have higher quality factors compared to single-ended inductors as discussed in Chapter 3. The

Table 5-2. Dimensions and model parameter values of the MEMS capacitor

Inputs		**Outputs**	
lf	347 μm	Cmin	276 fF
wf	4 μm	Cmax	1 pF
tf	10 μm	L	858 pH
gmin	0.65 μm	R	1.9
gmax	6.6 μm	Cgr	18 fF
n	18		
GMD	5.7 μm		
b	4		
lb	280 μm		
wb	2.6 μm		
lint	320 μm		
wint	10 μm		
gint	8um		

differential inductors in the foundry-provided physical design kit have constant spacing, 10 μm, and can have different widths. The foundry supports inductors with different widths changing from 4 μm to 60 μm. In order to prevent the inductor having large area, the narrow width (10 μm-30 μm) differential inductors with the cell name ind_dif_nw_cu (nw stands for narrow width) are chosen. The top metal of the inductors is copper which has slightly lower resistivity than aluminum. The dimensions of L_1 and L_2 are given in Table 5-3.

As can be seen in the table, the inductance values of L_1 and L_2 are slightly different than the values obtained using the analytical filter performance equations with ideal components which are shown in Table 5-1. As can be seen in design flowchart in Figure 5-4, the inductance values are revised after the simulation of the filter with the models of MEMS capacitors and inductors without interconnect models. The layouts of the inductors L_1 and L_2 are given in Figure 5-8.

5.2.5 Design of Interconnects

As mentioned earlier, the modeling and design of interconnects are also very crucial to predict and optimize the filter response. In this section, the interconnect used in the capacitors, i.e., stator interconnects

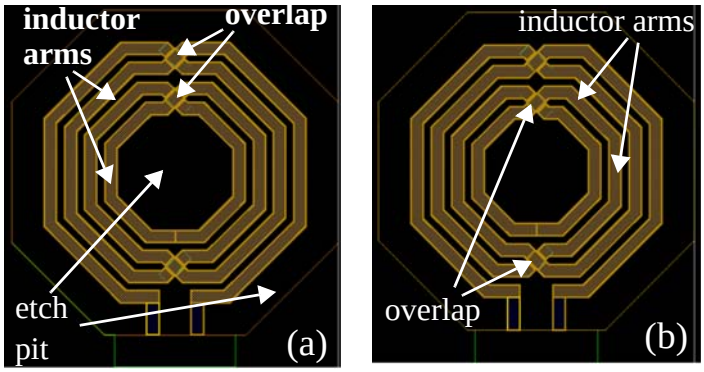


Table 5-3. Dimensions of the MEMS inductors

L1=4.3 nH	L2=3.86 nH
4	4
322 μm	307 μm
10 μm	10 μm
15 μm	14 μm

Figure 5-8 Layout of (a) 4.3nH inductor (b) 3.86nH inductor

and the wiring interconnects between the components are presented separately. The main difference between stator and wiring interconnects is that they have different parasitic capacitance due to the anchoring bridges to provide mechanical stability. In both capacitor and filter designs, the length of stator and wiring interconnects are minimized to reduce the parasitics.

5.2.5.1 Stator Interconnect Design

The stator interconnect must be designed to minimize the parasitics it introduces to the capacitor. Figure 5-9 shows the layout and cross-section view of the stator interconnect. As can be seen in the layout, ground shield metals are placed at a intervals of 100um. The square-shaped ($30\mu m \times 30\mu m$) metal shields form anchors to provide the mechanical stability. Since there is no shielding between the anchors, in the post

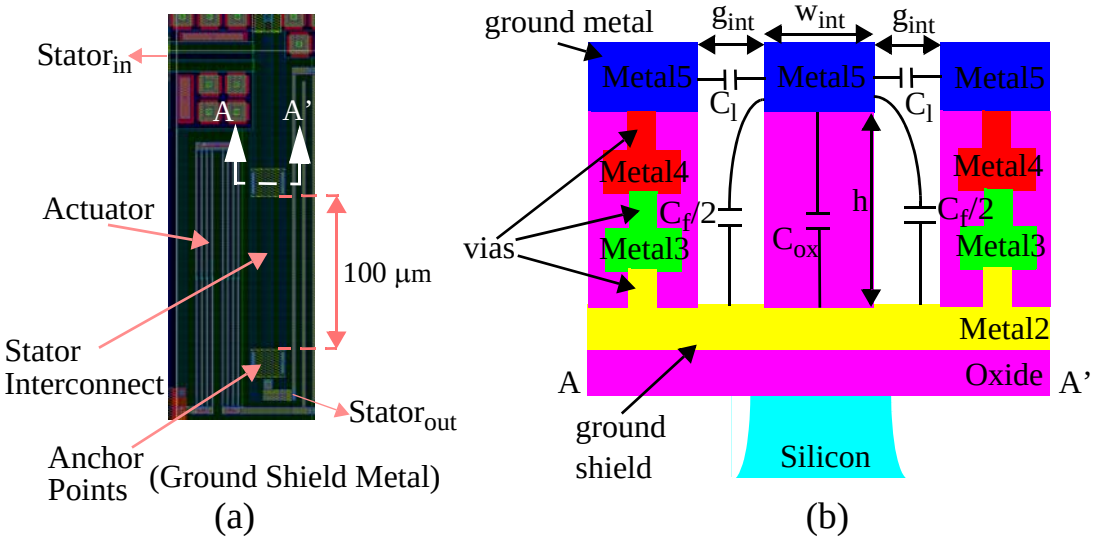


Figure 5-9 (a) layout (b) cross-section view of the stator interconnect

processing, the silicon under the interconnect is removed except at the anchor locations. Hence, the parasitic capacitive coupling between interconnect and substrate is minimized. The distance of 100um between pairs of anchors is chosen to minimize bending in the interconnect, and comes from curl test structures. The lowest metal layer is the most ideal for the shield metal, however, since metal1 in this process is not resistant to the etchant used to sacrificially remove the silicon, metal2 is used as shown in Figure 5-9.

The model of the new stator interconnect is shown in Figure 5-10 (a). The total parasitic capacitance of the stator interconnect, C_{gr1}, is composed of oxide capacitance, C_{ox}, side capacitance between signal line and ground metals, $2C_l$, and fringing capacitance, C_f as shown in (5.5). The capacitance values of these capacitors can be calculated by the expressions given in (2.11), (2.9) and (2.16), respectively. C_{ox} and C_f capacitance values are calculated for one anchor, and multiplied with the number of anchors to find the $C_{ox,\,total}$ and $C_{f,\,total}$. The parasitic inductance,L_{int} and resistance, R_{int} can be calculated expressions in (2.8). The width of the stator interconnect, w_{int} and side gap, g_{int} shown in Figure 5-9 (b) are chosen as 10 μm and 8 μm, respectively.

$$C_{gr1} = C_{ox} + 2C_l + C_f \tag{5.5}$$

5.2.5.2 Wiring Interconnect Design

The interconnects used between the MEMS capacitors and inductors are also designed to minimize parasitic capacitance, while at the same time being mechanically anchored. Unlike the stator interconnects, the wiring interconnects are routed at the edge of a MEMS etch-pit. They are anchored by cantilever bridges connected to an adjacent ground line. These bridges have a width of 5 μm, which is low enough to not create an important coupling. Figure 5-11 shows the layout and the cross-section view of the wiring interconnects.

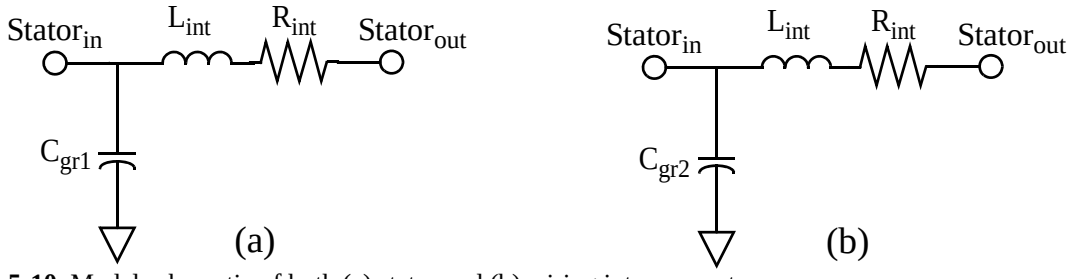


Figure 5-10 Model schematic of both (a) stator and (b) wiring interconnect

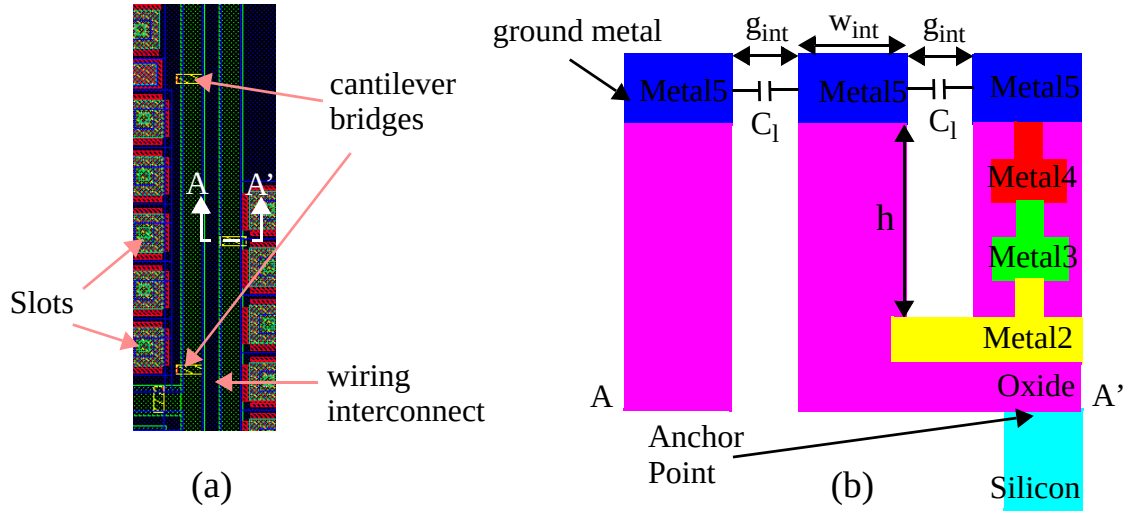


Figure 5-11 (a) layout (b) cross-section view of the wiring interconnect

The model schematic for wiring interconnect is the same with the stator interconnect model shown in Figure 5-10 (b). However, the oxide capacitance, C_{ox}, and fringing capacitance, C_f, in the stator interconnect model can be neglected. Hence the total parasitic capacitance, C_{gr2}, is equal to $2C_l$. The parasitic inductance and resistance values in Figure 5-10 (b) can be calculated using (2.8). The width of the wiring interconnect, w_{int} and side gap, g_{int} shown in Figure 5-11 (b) are chosen as 10 μm and 8 μm, respectively

As can be guessed, a stator interconnect has more parasitic capacitance than the wiring interconnect which has the same length with the stator interconnect, whereas they have same parasitic inductance and resistance. After design of MEMS capacitor, inductor and interconnects, the layout of the filter is drawn. The next section describes the physical layout design and optimization of the layout.

5.2.6 Filter Layout

Before starting to draw the floor plan, one final circuit simulation regarding to the topology is performed. As seen in Figure 5-5, there are two series LC resonators in the filter. These two inductor-capacitor resonator models are replaced in four combinations (CLLC, CLCL, LCCL, LCLC) in four different filters and two-port simulation are performed to find the best IL. At the end, the CLLC combination is decided to be drawn. In order to make an efficient physical design, before drawing the layout, a floor plan is generated to minimize the interconnect, hence minimize the parasitics of the filter. After placing the components, the

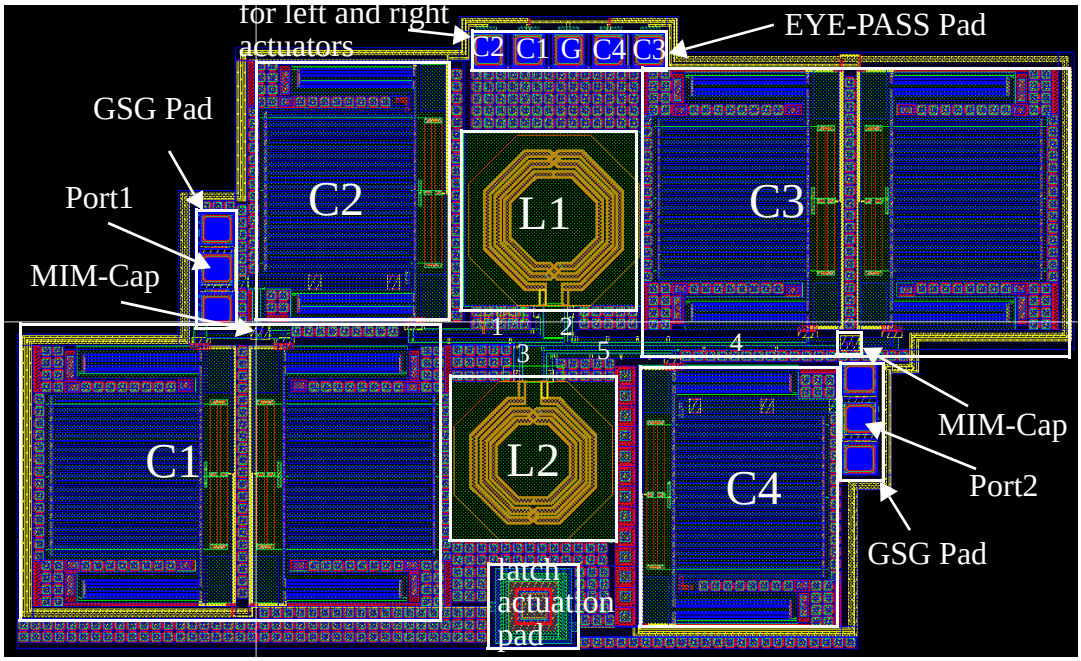


Figure 5-12 Layout of the ST7RF filter

interconnects are drawn in the layout. The layout of the complete filter is shown in Figure 5-12. As shown in Table 5-2, the designed capacitor is predicted to take values between 276 fF and 1 pF, and coupling capacitors need to take values between 1.8 pF and 2.8 pF as declared in Table 5-1. Hence, the coupling capacitors, C_1 and C_3, are generated by connecting two MEMS capacitors and one MIM capacitor with a value of 600 fF in parallel in order to achieve the tuning range. By this way, the quality factor is increased, since the Q-factor of MIM capacitor is greater than that of the MEMS capacitor. Furthermore, in order to increase the quality factor of C_1 and C_3 more, since one terminal of coupling capacitors is grounded, the stator interconnect is replaced with a wide ground metal. Hence, MEMS capacitors used in C_1 and C_3 have much less parasitics than those for C_2 and C_4.

In order to actuate the 4 MEMS capacitors, 4 independent actuation voltages plus a common latch actuation voltage and a common ground are needed. A 5-probe eye-pass pad array and a single probe pad are used as shown in Figure 5-12. As used in previously designed filters described in Chapter 4, two GSG pads are used to perform two-port S-parameter simulations.

RF-MEMS reconfigurable LC-based filter layout design has some rules that should be taken into account. First of all, as in RF design, the coupling between substrate and signal path should be minimized, since the field characteristic in the substrate is difficult to predict. Secondly, the length of the interconnects should be minimized to reduce the IL of the filter. Furthermore, the layout is drawn symmetric to minimize the mismatch between the identical components in the circuit. Since the filter is post-processed to release the capacitors, inductors and even the interconnects, the etch openings in the filter must have the same oxide thickness. In order to achieve this, all the etch openings need to be covered by active region mask. Finally, to have less stress, the layer density requirements can be satisfied by using slots with every layer.

After finalizing the layout, the complete schematic of the filter including the interconnect models has been generated. Next section presents two-port S-parameter simulation and measurement of final schematic of the filter.

5.2.7 Simulation and Measurement Results

Figure 5-13 shows the complete schematic of the third generation filter including MEMS capacitor, MIM capacitor, micromachined inductor and wiring interconnect models. In order to create wiring interconnect models, the length of every wiring interconnect is measured. Each interconnect is numbered uniquely in the layout shown in Figure 5-12 and on the schematic in Figure 5-13. The width and side gap values of every wiring interconnect are 10 μm and 8 μm, respectively, as declared in Section 5.2.5.2. The inductor models are created by modified model file as explained in Section 5.2.4. The MEMS capacitor models used

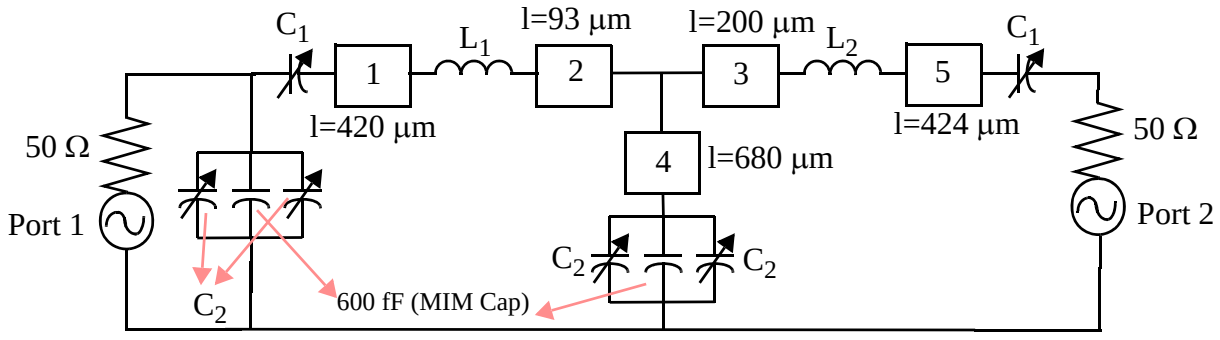


Figure 5-13 Final schematic of the filter including wiring interconnect models

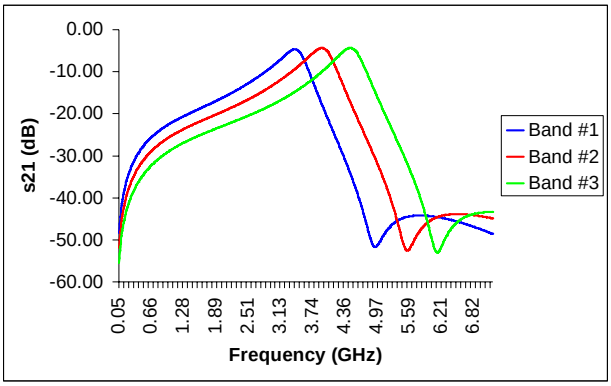


Table 5-3. Filter Characteristic and Component Values

Band #1	Band #2	Band #3
C1=670 fF	C1=480 fF	C1=350 fF
C2=670 fF	C2=480 fF	C2=350 fF
L1=3.6 nH	L1=3.6 nH	L1=3.6 nH
L2=3 nH	L2=3 nH	L2=3 nH
ω_0=3.424 GHz	ω_0=3.94 GHz	ω_0=4.494 GHz
IL=4.66 dB	IL=4.37 dB	IL=4.36 dB
BW=522 MHz	BW=535 MHz	BW=528 MHz

Figure 5-14 The frequency response of the filter for three frequency bands

in the schematic are shown in Table 5-2 and 600 fF MIM capacitors models are supplied by foundry. After combining every model, two-port S-parameter simulations are performed and the MEMS capacitors values are tuned to satisfy the resonance frequency and bandwidth specifications for three bands shown in Figure 5-1. For all three bands, third generation filter component values and filter characteristics are shown in Table 5-3. The frequency response of the filter for all three bands are shown in Figure 5-14.

As seen in Table 5-3, the resonant frequency and bandwidth specifications are achieved by tuning the MEMS capacitors, however IL of the filter is not lower than 4.3 dB. Hence, in the final simulations, IL specification which is given in Section 5.1.1 is not satisfied. In order to decrease the IL of the filter without changing ω_0, C_2 values need to be decreased while C_1 values are increased. However, this modification will increase the bandwidth and decrease the quality factor (Q) of the filter. Hence, as mentioned earlier, there is a trade-off between IL and Q of the filter.

The pole generated by R_s and C_1 in Figure 5-5 causes the right arms of the frequency response of the filter to be steeper than left arm. This enables the filter to reject the signals in the higher bands than the lower bands. The filter rejects the signals in the lower bands with 5-6 dB loss, while it rejects the signals in higher bands with 10-11 dB. The switching time characteristic of the filter can be obtained after making the measurement.

The first measurement results of the filter is given in Appendix E. Unfortunately, the improper post processing of the filter led to unreliable result of third generation filter. The filter measurement results are expected to match the post-layout simulation results after removing the silicon under the signal lines without any polymerization.

In this chapter, the complete design process of the third generation RF-MEMS reconfigurable LC-based bandpass filter is presented. In the filter, wiring interconnects have been modeled and designed as major design components like the MEMS capacitors and micromachined inductors. The stator interconnect in the MEMS capacitor has been designed to minimize the parasitics. For improving matching and simplicity, a unit MEMS capacitor is used in the filter. Micromachined inductors have been modeled and designed from the foundry inductor models provided by the ST Microelectronics process. The complete schematic of the filter is generated by combining the wiring interconnect, the MEMS capacitor and micromachined inductor models. The post-layout simulation results are presented at the end of the chapter. The filter covers the lowest three frequency bands of UWB with an insertion loss of 4.5 dB.

6 Conclusions and Future Work

This thesis presents the models of CMOS-MEMS tunable capacitor [13], micromachined inductors and wiring interconnects designed, and fabricated in Jazz 0.35 μm BiCMOS and ST Microelectronics 0.25 μm BiCMOS processes. It describes the complete design of a third generation RF-MEMS reconfigurable LC-based bandpass filter using the MEMS circuit component models along with simulation and measurement results.

The CMOS-MEMS tunable capacitor model includes the analysis of parasitic effects such as self inductance, substrate coupling, fringing capacitance and micromachining effects such as metal bloating and polymer deposition due to CMOS-MEMS post processing. The model not only helps the understanding the importance of the parasitics but also enables the prediction and optimization of RF-MEMS reconfigurable filter specifications such as quality factor, insertion loss and tuning range. One test capacitor was designed, fabricated and tested. The capacitance value at DC obtained from simulations of proposed capacitor model and measurement results match with an error of less than 7%. The measurement results show that the parasitic inductance of the proposed capacitor model is overestimated by %90. Although this overestimation has been taken into account in the new filter design using the experience from previous measurements (the inductance values are decreased by the ratio of estimated inductance value to extracted one), in order to predict the self resonance frequency and quality factor of the capacitor more accurately, some HFSS simulations with subparts of the MEMS capacitor need to be done. In order to increase the quality factor of the capacitor, the length of the stator interconnect and the actuator beams need to be minimized, however the displacement of the interdigitated beam decreases as the actuator beams gets shorter. Hence, there is a trade-off between quality factor and tuning range of the MEMS capacitor.

One of the most important problem with the MEMS capacitor is that post-processed capacitor interdigitated beams show lateral and vertical curling which decrease the tuning range considerably. In order to achieve higher reconfiguration, new capacitor designs are needed to improve curl matching. The highest tuning range measured for a single MEMS capacitor so far is 230 fF:520 fF, and the quality factor is 35 and 25 at 4 GHz for minimum and maximum capacitance cases, respectively. Although the MEMS capacitors with higher tuning range have been designed and fabricated, since they were used in the filter, they could not be measured indivually. The largest gap between the interdigitated beams is 7 μm, while longest interdigitated beam and actuator beam lengths are 347 μm and 280 μm, respectively. In order to design the MEMS capacitor with longer beams and larger gap, the electrothermal actuator characterization needs to be done accurately to provide the necessary displacement. For the third generation filter, the MEMS capacitor with tuning range of 230 fF:1 pF, and quality factor of 70 and 18 at 4 GHz for minimum and maximum capacitance cases, respectively was designed. It is important to mention that these tuning range and quality factor values were calculated assuming that there is no lateral or vertical curling in the interdigitated beams. In order to characterize the test capacitors in the ST Microelectronics process more accurately, test capacitors need to be designed, fabricated and tested in future.

The micromachined inductor models are generated using the models supplied by two different foundries. The micromachined inductor model simulation and measurement results matched well. The 12 nH and 4 nH test inductors have quality factors of 15 and 18 at 2.8 GHz in the Jazz process. The 4 nH test inductor has an extracted quality factor of 25 at 4 GHz from simulation results. In order to verify the inductor models generated in the ST Microelectronics process, individual inductor test structures need to be designed, fabricated and tested.

The models for the MEMS capacitors, micromachined inductors and wiring interconnects have been verified by modeling the previous filters designed in Jazz process. The simulation results of models matched well with measured results. The extracted capacitor and inductor values used in both first and second generation filters have been given in Chapter 4. After measuring the second generation filter, it is

concluded that since the post-processing steps affect the matching of MEMS capacitor interdigitated beams with different dimensions, in the third generation filter design, one capacitor should be used as a unit cell to improve the matching.

In the third generation filter design, the wiring interconnects have been treated as main design components along with the MEMS capacitors and micromachined inductors. Many specifications of the filter are borrowed from UWB standards considering MEMS circuit components quality factors and tuning range. The topology of the filter was selected using the experience gained in previous filter designs and the range of MEMS circuit component values. The design of the filter is based on the models generated for individual circuit elements. The post-layout simulations show that the filter has approximately 4.5 dB insertion loss for the lowest three frequency bands of UWB with resonance frequencies of 3.3GHz, 3.8 GHz and 4.3 GHz and bandwidth of 528 MHz. The reliable measurement results of the third generation filter could not be obtained because of the improper post-processing steps which caused substantial substrate coupling. With the proper post-processing, the filter is expected to give the measurement results matching with the simulation results given in Chapter 5.

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APPENDIX A

A.1 Background

A.1.1 DC Self Inductance of a Wire

The DC self inductance of a wire with a rectangular cross-section area, L_{self}, and the mutual inductance between two parallel wires, M, can be expressed as below [15], respectively:

$$L_{self} = 2 \times l \times \left(ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{w+t}{3l}\right) \tag{A.1}$$

$$M = 2lQ,\ Q = ln\left(\frac{l}{GMD} + \sqrt{1+\left(\frac{l}{GMD}\right)^2}\right) - \sqrt{1+\left(\frac{GMD}{l}\right)^2} - \frac{GMD}{l} \tag{A.2}$$

where L_{self} is the self inductance in nH, l is the wire length in cm, w is the wire width in cm, t is the wire thickness in cm, Q is the mutual inductance parameter and GMD denotes the geometric mean distance between two wires which is approximately equal to the pitch of the wires. It should be mentioned that (A.2) is not valid for wires having cross-section dimension greater than approximately twice their length.

A.1.2 Fringing Capacitance of Interconnect Wires

In [17], it is stated that when the conductor with a rectangular cross-section, as shown in Figure A-1, is considered, the fringing capacitance of the rectangular conductor could be closely approximated by removing a section of width $t/4$ from each end of the rectangle and replacing it with a semiconductor session of radius $t/2$. The total perimeter of the semiconductor ends is πt while the total perimeter removed from the rectangle is $3t$. Thus, there is a close match. When $w \geq t/2$, the total fringing capacitance per unit length can be calculated as follows:

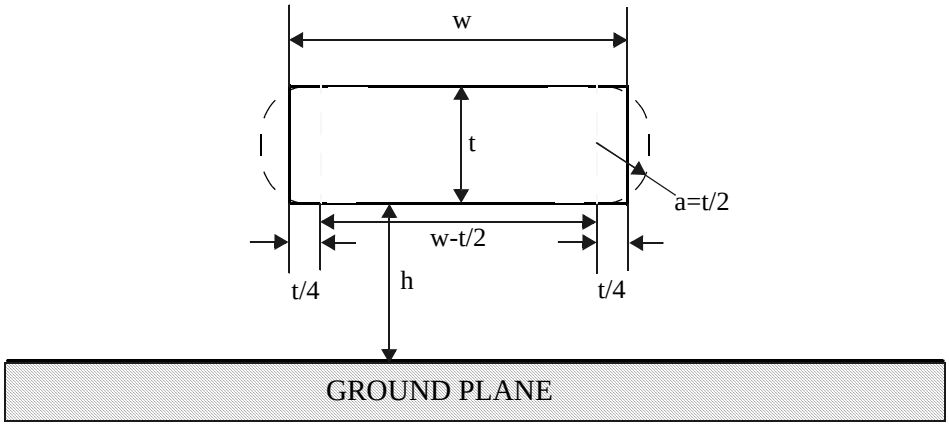


Figure A-1 Cross-section of modeled finger group

$$C_f = \frac{2\pi\varepsilon}{ln\left(1 + \frac{2h}{t} + \sqrt{\frac{2h}{t} \times \left(\frac{2h}{t} + 2\right)}\right)} \tag{A.3}$$

A.1.3 Capacitance of Interdigitated Fingers

In order to model the capacitance between the interdigitated fingers, the capacitance modeling of comb actuators without ground plane is used [14]. Figure A-2 shows the top view and cross section of one finger group with the model parameters. The charge on one of the fingers is approximated as the uniform

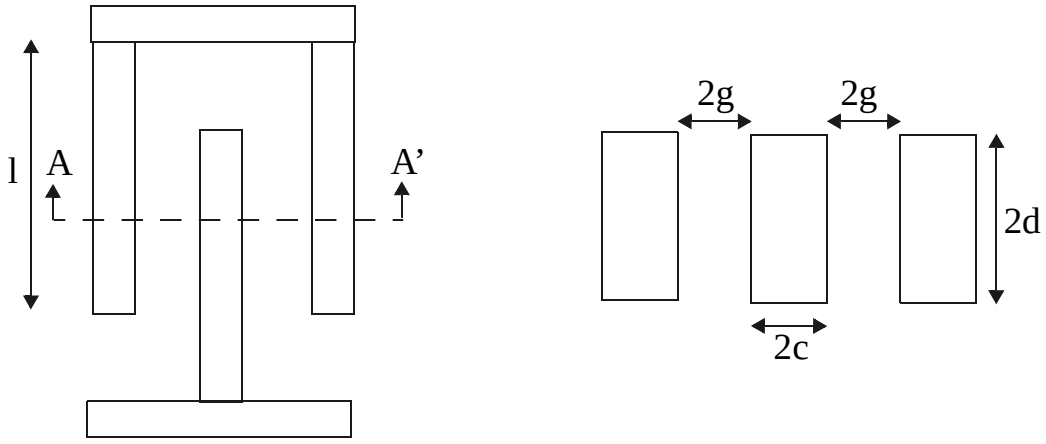


Figure A-2 (a) top view (b) cross-section of finger groups

field charge on the vertical sides of the rotor finger plus a fringe field charge due to the top and bottom sides of the rotor finger. Hence, the total capacitance which is derived by conformal mapping is below:

$$C \approx \frac{\varepsilon_0 \times 2d \times l}{g} + 2\varepsilon_0 l \times K\left(sin\left(\frac{\pi c}{2(c+g)}\right)\right) / K\left(sin\left(\frac{\pi c}{2(c+g)}\right)\right) \tag{A.4}$$

$$K(x) = \int_0^{\pi/2} \frac{1}{\sqrt{1 - x^2 (sin(\theta))^2}} d\theta \tag{A.5}$$

where $K(x)$ is the complete elliptic integral of the first kind. If d/g is much larger than $\frac{1}{2\pi}$, the capacitance can be expressed more accurately as follows:

$$C \sim \frac{\varepsilon_0 \times 2d \times l}{g} + \frac{2\varepsilon_0}{\pi} ln\left(\left(\left(\frac{c}{g}+1\right)^2 - 1\right) \times \left(1 + \frac{2g}{c}\right)^{\left(1+\frac{c}{g}\right)}\right) \tag{A.6}$$

When the interdigitated fingers are considered, the minimum capacitance can be modeled using (A.4), whereas the maximum capacitance can be expressed by using (A.6).

A.1.4 Mutual Inductance Effect

Figure A-3 shows a pair of coils placed closely to have an interaction between their magnetic fields. The magnetic flux in one coil depends on the currents passing through both coils. The magnetic flux of the first coil, $\Phi_1(i_1, i_2)$ and the magnetic flux of the second coil $\Phi_2(i_1, i_2)$ can be expressed as:

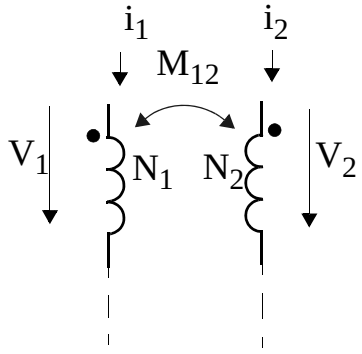


Figure A-3 A pair of coils placed closely

$$\Phi_1(i_1,i_2) = \Phi_{11}(i_1) + \Phi_{12}(i_2) \quad \text{(A.7)}$$

$$\Phi_2(i_1,i_2) = \Phi_{21}(i_1) + \Phi_{22}(i_2) \quad \text{(A.8)}$$

If all the N_1 and N_2 turns of the coils are linked by the magnetic flux Φ_1 and Φ_2, the flux linkage of the first and second coil can be calculated as $\lambda_1 = N_1\Phi_1$ and $\lambda_2 = N_2\Phi_2$, respectively. Assuming that the magnetic fluxes are linear functions of the coil currents, λ_1 and λ_2 can be written as below:

$$\lambda_1(t) = L_{11}i_1(t) + L_{12}i_2(t) \quad \text{(A.9)}$$

$$\lambda_1(t) = L_{21}i_1(t) + L_{22}i_2(t) \quad \text{(A.10)}$$

where L_{11} and L_{22} are self inductances, L_{12} and L_{21} are the mutual inductances of the inductors. By energy considerations, it is established that in general $L_{12} = L_{21} = M$. In the case $i_1 = i_2$, the equivalent inductance will be equal to $L = L_{11} \pm M$. The sign of the equation depends on the direction of the current on the coils.

A.2 Capacitance and Quality Factor Derivations

The capacitance and quality factor derivations of the capacitor models used in Jazz and ST processes are given in this section.In order to simplify the derivations, series RLC network to parallel RLC network transformation is also presented.

A.2.1 Series RLC to Parallel RLC Transformation

Figure A-4 shows the series and parallel RLC networks, in order to derive the parallel component values, R_p, L_p and C_p in terms of R_s, L_s and C_s, the impedance of two networks have been equalized as seen in (A.11). Since in the derivation of quality factor, series to parallel transformation is used, the expressions for parallel to series transformation are not given. However, the equations for parallel to series transformation can be derived using the same method. In order to derive the equations of R_p, the real part of the input impedance of the both networks are equalized, than R_p can be written explicitly as shown in (A.12). Equaling imaginary parts of both input impedances is not enough to derive C_p and L_p, since there

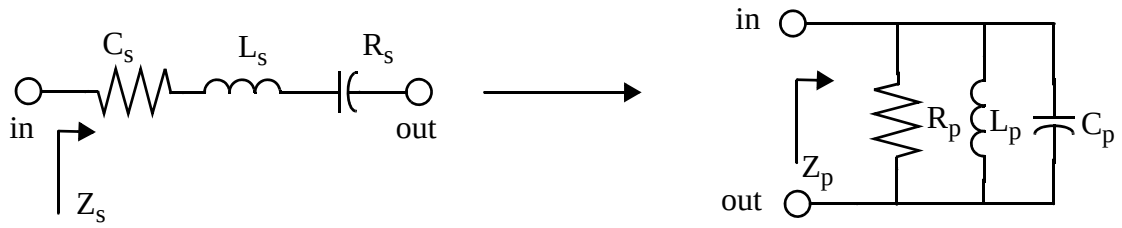


Figure A-4 Series RLC to Parallel RLC Transformation

is only one expression for unknown variables. Hence another independent equation is needed. Regardless of series of parallel representation, both networks needs to have same resonance frequency, i.e., $1/(\sqrt{C_s L_s}) = 1/(\sqrt{C_p L_p})$. By using the imaginary parts and self resonance frequency expression, L_p and C_p are derived as shown in (A.13) and (A.14), respectively.

$$Z_s = Z_p, R_s + jwL_s + \frac{1}{jwC_s} = \frac{1}{\frac{1}{R_p} + \frac{1}{jwL_p} + jwC_p} \tag{A.11}$$

$$R_p = R_s\left(1 + \frac{1}{w^2 C_s^2 R_s^2}(1 - w^2 L_s C_s)^2\right) \tag{A.12}$$

$$L_p = -R_s^2 C_s\left(1 + \frac{1}{w^2 C_s^2 R_s^2}(1 - w^2 L_s C_s)^2\right) \tag{A.13}$$

$$C_p = \frac{-L}{R_s^2\left(1 + \frac{1}{w^2 C_s^2 R_s^2}(1 - w^2 L_s C_s)^2\right)} \tag{A.14}$$

A.2.2 Quality factor of a Capacitor

Quality factor of a capacitor is generally defined as the ratio of the stored energy to the energy loss in one cycle as shown below:

$$Q_{cap} = 2\pi \frac{E_{stored}}{E_{loss-one-cycle}} \tag{A.15}$$

However, this expression does not take the negative effect of the parasitic inductance of a non-ideal capacitor into account. In this section, the quality factor of a capacitor is defined as similar to the definition of inductor proposed in [26]. The quality factor of a capacitor with parasitic inductance can be defined as the ratio of the difference of the peak electrical energy and peak magnetic energy to the energy loss in one oscillation cycle as shown in (A.16).

$$Q_{cap} = 2\pi \frac{E_{peak-electrical} - E_{peak-magnetic}}{E_{loss-one-cycle}} \tag{A.16}$$

If the capacitor is modeled as a parallel RLC network as shown in Figure A-5, peak electrical energy, peak magnetic energy and energy loss in one cycle can be expressed as in (A.17), (A.18) and (A.19), respectively. If these expressions are inserted into (A.16), the quality factor of a capacitor modeled as a parallel RLC network can be derived as below:

$$Q_{cap} = 2\pi \frac{\frac{CV_0^2}{2} - \frac{V_0^2}{2w^2L}}{\frac{\pi V_0^2}{wR}} = -\frac{R}{wL}(1 - w^2LC) \tag{A.20}$$

A.2.3 Quality Factor Derivation of Capacitor Model in Jazz Process

The capacitor model proposed for Jazz 0.35μm BiCMOS process in Section 2.1.3 can be transformed to a parallel RLC network using the method shown in Section A.2.1 if the rotor terminal of the capacitor is grounded as shown in Figure A-5. As seen in this figure, the parasitic RC on the shunt branch and series RLC network are transformed to parallel RLC circuit. R_p, L_p and C_p can be derived using

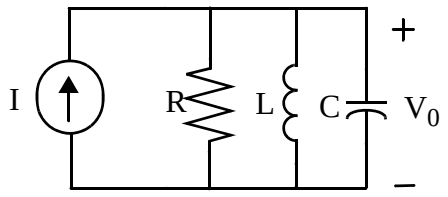


Figure A-5 Parallel RLC network with current source

$$E_{peak-electrical} = \frac{CV_0^2}{2} \tag{A.17}$$

$$E_{peak-magnetic} = \frac{V_0^2}{2w^2L} \tag{A.18}$$

$$E_{loss-one-cycle} = \frac{\pi V_0^2}{wR} \tag{A.19}$$

(A.12), (A.13) and (A.14) in terms of R_s, L_s, and C_s shown in Figure A-5, respectively. At the end, the complete model is a parallel RLC network. Hence, (A.20) can be used to find the quality factor of the capacitor model. The equivalent R, L and C are given below:

$$R_{subp} = R_{sub}\left(1 + \frac{1}{w^2 C_{ox}^2 R_{sub}^2}\right), C_{oxp} = C_{ox}\left(\frac{1}{1 + w^2 C_{ox}^2 R_{sub}^2}\right) \tag{A.21}$$

$$R = \left(\frac{1}{R_{subp}} + \frac{1}{R_p}\right)^{-1}, L = L_p, C = C_{gr} + C_{oxp} + C_p \tag{A.22}$$

The complete equation for the quality factor is derived by replacing R, L and C given in (A.22) into (A.20). There are three main terms in the quality factor expression shown in (A.23), series resistive loss factor, substrate loss factor and self resonance loss factor.

$$Q_{cap} = -\frac{R}{wL}(1 - w^2 LC) = -\frac{\left(\frac{1}{R_{subp}} + \frac{1}{R_p}\right)^{-1}}{wL_p}(1 - w^2 L_p(C_{gr} + C_{oxp} + C_p)) \tag{A.23}$$

$$Q_{cap} = \frac{1}{wR_s C_s} \times substrate - loss \times self - res - loss \tag{A.24}$$

$$substrate - loss = \frac{R_{subp}}{R_{subp} + R_s\left(1 + \frac{1}{w^2 C_s^2 R_s^2}(1 - w^2 L_s C_s)^2\right)} \tag{A.25}$$

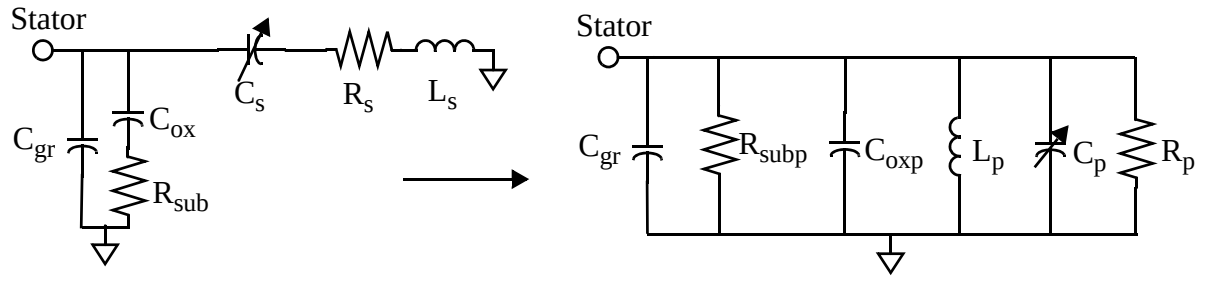


Figure A-5 Capacitor model parallel RLC network transformation

$$self-res-loss = 1-w^2C_s\left(L-(C_{gr}+C_{oxp})R_s^2\left(1+\frac{1}{w^2C_s^2R_s^2}(1-w^2L_sC_s)^2\right)\right) \quad \text{(A.26)}$$

The expressions above are implemented in the MATLAB model file to generate the graph for qualify factor vs. frequency. As mentioned before, the expressions given in this section belong to the model generated for capacitors implemented in Jazz process.

A.2.4 Capacitance Derivation of Capacitor Model in Jazz Process

In order to derive the capacitance equation in terms of frequency and model components, it is assumed that the imaginary part of the input impedance of the capacitor model is caused by only capacitance, i.e., the parasitic inductance is neglected. The input impedance of the model schematic can be found by using Figure A-5.

$$Z_{in} = \left(\frac{1}{R_p}+\frac{1}{R_{subp}}+jw(C_{gr}+C_{oxp}+C_p)+\frac{1}{jwL_p}\right)^{-1} \quad \text{(A.27)}$$

$$Im(Z_{in}) = \frac{-1}{wC} \Rightarrow C = \frac{-1}{wIm(Z_{in})} \quad \text{(A.28)}$$

The equation of the input impedance and capacitance are very difficult to simplify by hand analysis, hence these expressions are implemented in MATLAB model file to generate the graph of capacitance vs. frequency.

A.2.5 Capacitor MATLAB Model File for Jazz Process

```
function capacitor_model()
global lb lf wb b w wf tf t u0 e0 h1 h2

%Constants and Process Parameters
t=2.81e-6;%thickness of m4
tm1=0.635e-6;%thickness of m1
u0=4*pi*10^(-7);%permeability constant
e0=8.82*10^(-12);%permitivity constant
hf=5.17e-6;%height from top of m1 to bottom of m4
h1=7.025e-6;%height of metal4 from substrate
h2=280e-6;%height of substrate
```

```
h=h1+h2;%total height
sh_m4=10e-3;%sheet resistance of m4
er=3.9;%relative dielectric constant of siliconoxide

%Dimensions of the Interdigitated Fingers
lf=247e-6;%length of fingers
wf=4e-6;%width of fingers
tf=9.835e-6;%thickness of metal stack
g_max=4.6e-6;%minimum gap between fingers
g_min=0.6e-6;%maximum gap between fingers
n=12;%number of finger groups
GMD=5e-6;

%Model Parameters for Interdigitated Fingers
Cfin_min=n*lf*(e0*2*tf/g_max+2*e0*K(sin(pi*wf/4/(wf+g_max)))/K(cos(pi*wf/4/
(wf+g_max))));%minimum capacitance
Cfin_max=n*lf*(e0*tf/g_min+(e0/pi*log(((wf/g_min+1)^2-1)*(1+2*g_min/wf)^(1+wf/
g_min))));%maximum capacitance
Q=log(lf/GMD+sqrt(1+(lf/GMD)^2))-sqrt(1+(GMD/lf)^2)+GMD/lf;
Lfin=1/n*2*lf*((n+1)*(log(2*lf/(wf+tf))+0.5+(wf+tf)/3/lf)+Q)*10^-7;%worst case
inductance of fingers
Rfin=(n+2)/n*sh_m4*lf/wf;%worst case resistance of fingers


%Dimensions of the Thermal Actuator
b=4;%number of beams
lb=200e-6;%length_of_beams
wb=2.6e-6;%width_of_beams

%Model Parameters of the Thermal Actuator
Lact=2/b*2*lb*(log(2*lb/(wb+t))+0.5+(wb+t)/3/lb)*10^-7;%worst case inductance
Ract=2/b*sh_m4*lb/wb;%worst case resistance of actuator

%Dimensions of the Stator Interconnect
lint=350e-6;%length of interconnect
w=10e-6;%width of interconnect
gint=8e-6;%lateral gap between interconnect and the ground layer

%Model Parameters of the Stator Interconnect
Cfrng1=e0*(2*pi/log(1+2*hf/t+sqrt(2*hf/t*(2*hf/t+2))))*lint;%fringing capaci-
tance in air
Cfrng2=e0*3.9*(2*pi/log(1+2*hf/tm1+sqrt(2*hf/tm1*(2*hf/tm1+2))))*lint;%fring-
```

```
ing capacitance in oxide
Cf=Cfrng1+Cfrng2;
Cs=e0*lint*t/gint;%capacitance between signal line and ground metal4
Cv=e0*er*lint*1e-6/hf;%capacitance between signal line and m1 ground(parallel
plate)
Cgr=2*Cs+Cf+2*Cv%total ground capacitance
Cox=e0*er*lint*w/hf%total oxide capacitance between signal line and substrate
Rsub=300%silicon resistance
Lint=2*lint*(log(2*lint/(w+t))+0.5+(w+t)/3/lint)*10^-7;
Rint=sh_m4*lint/w;%resistance of interconnect


%Capacitor Model Parameters
C_min=Cfin_min
C_max=Cfin_max
L=Lfin+Lint+Lact
R=Rfin+Ract+Rint

%---quality factor
freq=[45e6:10e6:20e9];
u=freq*2*pi;
Cp=Cgr+Cox./(1+(u.^2*Cox^2*Rsub^2));
Rsubp=Rsub*(1+1./(u.^2*Cox^2*Rsub^2));
ideal_Q_min=1./(u*R*Cfin_min);
Subst_Loss_min=Rsubp./(Rsubp+R.*(1+1./(u.^2*Cfin_min^2*R^2).*((1-
u.^2*L*Cfin_min).^2)));
Self_Res_Loss_min=1-u.^2.*(L.*Cfin_min-Cp*R^2*Cfin_min.*(1+(1./
(u.^2*R^2*Cfin_min^2).*((1-u.^2*L*Cfin_min).^2))));
Quality_Factor_min=ideal_Q_min.*Subst_Loss_min.*Self_Res_Loss_min;
ideal_Q_max=1./(u*R*Cfin_max);
Subst_Loss_max=Rsubp./(Rsubp+R.*(1+1./(u.^2*Cfin_max^2*R^2).*((1-
u.^2*L*Cfin_max).^2)));
Self_Res_Loss_max=1-u.^2.*(L.*Cfin_max-Cp*R^2*Cfin_max.*(1+(1./
(u.^2*R^2*Cfin_max^2).*((1-u.^2*L*Cfin_max).^2))));
Quality_Factor_max=ideal_Q_max.*Subst_Loss_max.*Self_Res_Loss_max;
figure;
plot(freq,Quality_Factor_min,'b',freq,Quality_Factor_max,'r');
legend('min','max');
xlabel('Frequency');
ylabel('Quality Factor');
axis([45e6 20e9 0 200]);
plottools on;
```

```
%---min_capacitance
Csp_min=-(L./(R^2))./(1+1./(u.^2*Cfin_min^2*R^2).*((1-u.^2*L*Cfin_min).^2));
Rp_min=R.*(1+1./(u.^2*Cfin_min^2*R^2).*((1-u.^2*L*Cfin_min).^2));
Lp_min=-(R.^2).*Cfin_min.*(1+1./(u.^2*Cfin_min^2*R^2).*((1-
u.^2*L*Cfin_min).^2));
C_final_min=Cp+Csp_min;
R_final_min=(1./Rp_min+1./Rsubp).^-1;
L_final_min=Lp_min;
Z_final_min=(1/i./u./L_final_min+1./R_final_min+i.*u.*C_final_min).^-1;
Cap_min=1./(i.*u.*Z_final_min);

%---max_capacitance
Csp_max=-(L./(R.^2))./(1+1./(u.^2*Cfin_max^2*R^2).*((1-u.^2*L*Cfin_max).^2));
Rp_max=R.*(1+1./(u.^2*Cfin_max^2*R^2).*((1-u.^2*L*Cfin_max).^2));
Lp_max=-(R.^2).*Cfin_max.*(1+1./(u.^2*Cfin_max^2*R^2).*((1-
u.^2*L*Cfin_max).^2));
C_final_max=Cp+Csp_max;
R_final_max=(1./Rp_max+1./Rsubp).^-1;
L_final_max=Lp_max;
Z_final_max=(1/i./u./L_final_max+1./R_final_max+i.*u.*C_final_max).^-1;
Cap_max=1./(i.*u.*Z_final_max);

figure;
plot(freq,Cap_min,'b',freq,Cap_max,'r');
legend('min','max');
xlabel('Frequency');
ylabel('Capacitance');
axis([45e6 20e9 0 1.5e-12]);
plottools on;

function y=K(x)
global lb lf wb b w wf tf t u0 e0 h1 h2
y=quadl(@(k)integrand(k,x),0,0.5);
function y=integrand(k,x)
global lb lf wb b w wf tf t u0 e0 h1 h2
      y=1./sqrt(1-(x.^2).*(sin(k)).^2);
```

A.2.6 Quality Factor Derivation of Capacitor Model in ST Process

The model proposed for the capacitor design in ST process can be transformed into parallel RLC circuit as done in the previous section (see Figure A-7). The quality factor of this capacitor model is derived

using equation (A.20). The main difference of this model, there is no substrate coupling, hence in the expression of quality factor, there is no substrate loss factor. In this specific model, the ground resistance is neglected.

$$Q_{cap} = -\frac{R}{wL}(1 - w^2 LC) = -\frac{R_p}{wL_p}(1 - w^2 L_p(C_{gr} + C_p)) \tag{A.29}$$

$$Q_{cap} = \frac{1}{wR_s C_s} \times self - res - loss \tag{A.30}$$

$$Q_{cap} = \frac{1}{wR_s C_s}\left(1 - w^2 C_s\left(L - C_{gr}R_s^2\left(1 + \frac{1}{w^2 C_s^2 R_s^2}(1 - w^2 L_s C_s)^2\right)\right)\right) \tag{A.31}$$

A.2.7 Capacitance Derivation of Capacitor Model in ST Process

The capacitance expression in terms of frequency and the other model parameters is derived using the same method in Section A.2.4. The input impedance of the circuit given in Figure A-6 is derived in (A.32). the equations (A.31) and (A.32) are implemented in Matlab script file created for the model of MEMS capacitor designed in ST process.

$$Z_{in} = \left(\frac{1}{R_p} + jw(C_{gr} + C_p) + \frac{1}{jwL_p}\right)^{-1} \tag{A.32}$$

$$Im(Z_{in}) = \frac{-1}{wC} \Rightarrow C = \frac{-1}{wIm(Z_{in})} \tag{A.33}$$

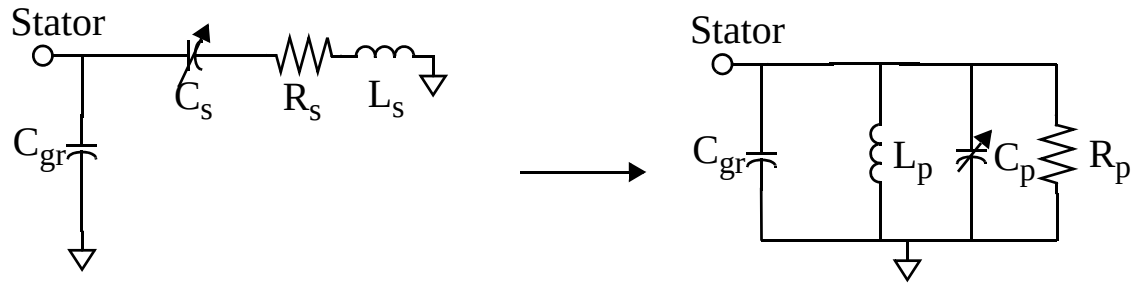


Figure A-6 ST Capacitor model parallel RLC transformation

A.2.8 Capacitor MATLAB Model File for ST Process

```
function capacitor_model()
global lb lf wb b w wf tf t u0 e0 h1 h2

%Constants and Process Parameters
t=2.81e-6;%thickness of m4
tm1=0.635e-6;%thickness of m1
u0=4*pi*10^(-7);%permeability constant
e0=8.82*10^(-12);%permitivity constant
hf=3.92e-6;%height from top of m2 to bottom of m5
sh_m5=11.6e-3;%sheet resistance of m5
er=3.9;%relative dielectric constant of siliconoxide

%Dimensions of the Interdigitated Fingers
lf=247e-6;%length of fingers
wf=4e-6;%width of fingers
tf=10e-6;%thickness of metal stack
g_max=4.6e-6;%minimum gap between fingers
g_min=0.6e-6;%maximum gap between fingers
n=12;%number of finger groups
GMD=5e-6;

%Model Parameters for Interdigitated Fingers
Cfin_min=n*lf*(e0*2*tf/g_max+2*e0*K(sin(pi*wf/4/(wf+g_max)))/K(cos(pi*wf/4/
(wf+g_max))));%minimum capacitance
Cfin_max=n*lf*(e0*tf/g_min+(e0/pi*log(((wf/g_min+1)^2-1)*(1+2*g_min/wf)^(1+wf/
g_min))));%maximum capacitance
Q=log(lf/GMD+sqrt(1+(lf/GMD)^2))-sqrt(1+(GMD/lf)^2)+GMD/lf;
Lfin=1/n*2*lf*((n+1)*(log(2*lf/(wf+tf))+0.5+(wf+tf)/3/lf)+Q)*10^-7;%worst case
inductance of fingers
Rfin=(n+2)/n*sh_m5*lf/wf;%worst case resistance of fingers


%Dimensions of the Thermal Actuator
b=4;%number of beams
lb=200e-6;%length_of_beams
wb=2.6e-6;%width_of_beams

%Model Parameters of the Thermal Actuator
Lact=2/b*2*lb*(log(2*lb/(wb+t))+0.5+(wb+t)/3/lb)*10^-7;%worst case inductance
Ract=2/b*sh_m5*lb/wb;%worst case resistance of actuator
```

```
%Dimensions of the Stator Interconnect
lint=350e-6;%length of interconnect
w=10e-6;%width of interconnect
gint=8e-6;%lateral gap between interconnect and the ground layer

%Model Parameters of the Stator Interconnect
Cf=e0*30e-6*w/hf+e0*(2*pi/log(1+2*hf/t+sqrt(2*hf/t*(2*hf/t+2))))*30e-6;%total
capacitance between shield and interconnect,30um is the shield length
Cs=e0*lint*t/gint;%capacitance between signal line and ground metal4
Cgr=2*Cs+2*Cf%total ground capacitance, there are two m2 shields
Lint=2*lint*(log(2*lint/(w+t))+0.5+(w+t)/3/lint)*10^-7;
Rint=sh_m5*lint/w;%resistance of interconnect


%Capacitor Model Parameters
C_min=Cfin_min
C_max=Cfin_max
L=Lfin+Lint+Lact
R=Rfin+Ract+Rint

%---quality factor
freq=[45e6:10e6:20e9];
u=freq*2*pi;
Cp=Cgr;
ideal_Q_min=1./(u*R*Cfin_min);
Self_Res_Loss_min=1-u.^2.*(L.*Cfin_min-Cp*R^2*Cfin_min.*(1+(1./
(u.^2*R^2*Cfin_min^2).*((1-u.^2*L*Cfin_min).^2))));
Quality_Factor_min=ideal_Q_min.*Self_Res_Loss_min;
ideal_Q_max=1./(u*R*Cfin_max);
Self_Res_Loss_max=1-u.^2.*(L.*Cfin_max-Cp*R^2*Cfin_max.*(1+(1./
(u.^2*R^2*Cfin_max^2).*((1-u.^2*L*Cfin_max).^2))));
Quality_Factor_max=ideal_Q_max.*Self_Res_Loss_max;
figure;
plot(freq,Quality_Factor_min,'b',freq,Quality_Factor_max,'r');
legend('min','max');
xlabel('Frequency');
ylabel('Quality Factor');
axis([45e6 20e9 0 200]);
plottools on;

%---min_capacitance
Csp_min=-(L./(R^2))./(1+1./(u.^2*Cfin_min^2*R^2).*((1-u.^2*L*Cfin_min).^2));
```

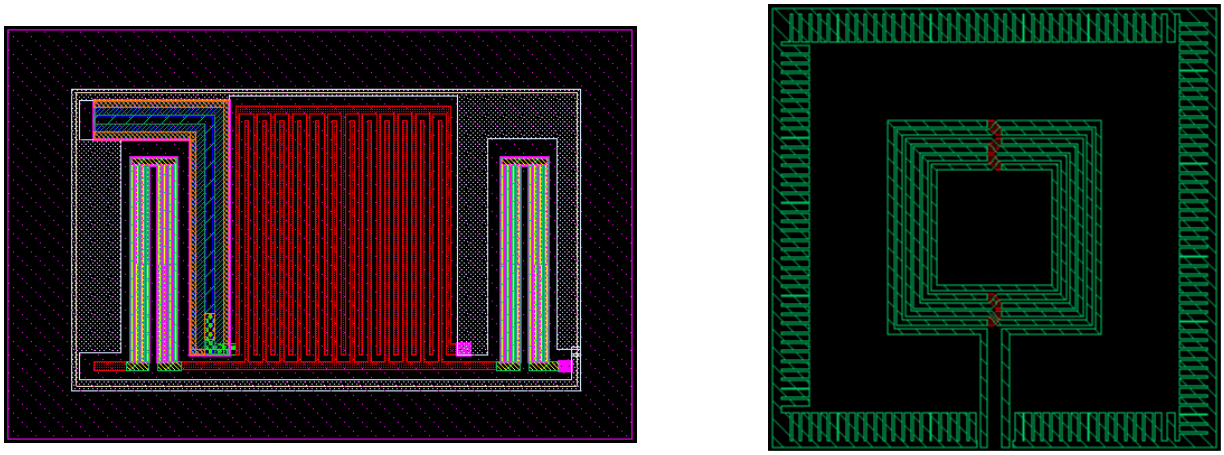
```
Rp_min=R.*(1+1./(u.^2*Cfin_min^2*R^2).*((1-u.^2*L*Cfin_min).^2));
Lp_min=-(R.^2).*Cfin_min.*(1+1./(u.^2*Cfin_min^2*R^2).*((1-
u.^2*L*Cfin_min).^2));
C_final_min=Cp+Csp_min;
R_final_min=Rp_min;
L_final_min=Lp_min;
Z_final_min=(1/i./u./L_final_min+1./R_final_min+i.*u.*C_final_min).^-1;
Cap_min=1./(i.*u.*Z_final_min);

%---max_capacitance
Csp_max=-(L./(R.^2))./(1+1./(u.^2*Cfin_max^2*R^2).*((1-u.^2*L*Cfin_max).^2));
Rp_max=R.*(1+1./(u.^2*Cfin_max^2*R^2).*((1-u.^2*L*Cfin_max).^2));
Lp_max=-(R.^2).*Cfin_max.*(1+1./(u.^2*Cfin_max^2*R^2).*((1-
u.^2*L*Cfin_max).^2));
C_final_max=Cp+Csp_max;
R_final_max=Rp_max;
L_final_max=Lp_max;
Z_final_max=(1/i./u./L_final_max+1./R_final_max+i.*u.*C_final_max).^-1;
Cap_max=1./(i.*u.*Z_final_max);

figure;
plot(freq,Cap_min,'b',freq,Cap_max,'r');
legend('min','max');
xlabel('Frequency');
ylabel('Capacitance');
axis([45e6 20e9 0 1.5e-12]);
plottools on;

function y=K(x)
global lb lf wb b w wf tf t u0 e0 h1 h2
y=quadl(@(k)integrand(k,x),0,0.5);
function y=integrand(k,x)
global lb lf wb b w wf tf t u0 e0 h1 h2
      y=1./sqrt(1-(x.^2).*(sin(k)).^2);
```

APPENDIX B

B.1 HFSS Two-port S-parameter Simulation

Two port S-parameter simulation of CMOS-MEMS tunable capacitors and micromachined inductors have been performed in Ansoft high frequency structure simulator, HFSS. HFSS can recognize the layout or .gds file by means of a technology file for simulation. In order to gain some basic experience in HFSS, it is recommended to follow the steps in [27] before simulating capacitor or inductor. In this section, two-port HFSS simulation process is described step by step.

- **Draw the simplified layout for HFSS simulation.** The layouts of MEMS capacitor and inductors consist of many layers, while transferring the layout into HFSS does not recognize the layer colors, hence all the layers need to be fixed in terms of color and material property. In order to simplify the layout transferring into HFSS, simplified layouts for both MEMS capacitor and inductor are drawn specifically for HFSS simulations. (see Figure 1)
- **Create the technology file.** In order HFSS recognize the different structures, a technology file needs to be created with .gds file. This .tech file consists of the information of layer number, label, color, elevation and the thickness. The technology file for the capacitor HFSS layout is given in Figure 2. The layers and the descriptions are given in Table 2-1.
- **Import the .gds file and .tech file into HFSS.**



(a) (b)

Figure B-1 (a) Capacitor (b) Inductor layouts created for HFSS model

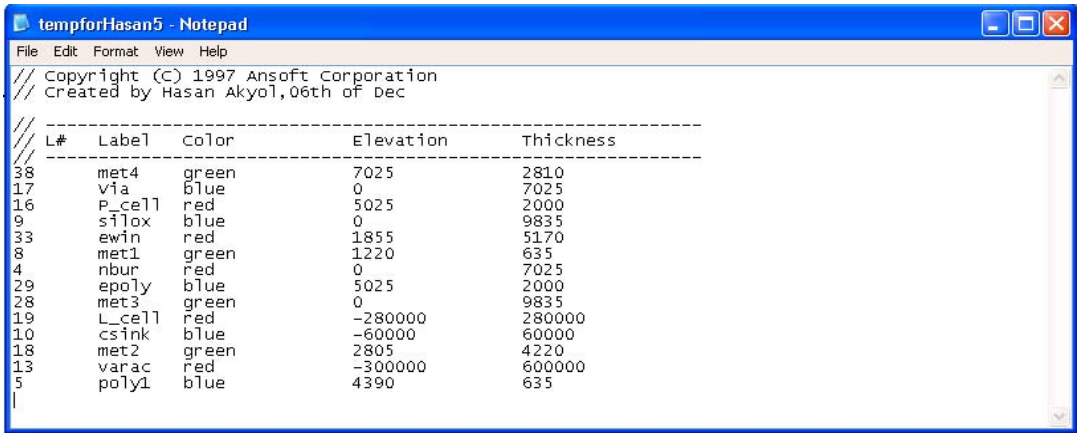


Figure B-2 Technologu file used to import the MEMS capacitor layout into HFSS

Table 2-1. Layers and their descriptions in Capacitor technology file

Layers	**Descriptions**
met4	interconnect and top ground metal
via	oxide between metal4 and silicon (at the end, subtract metal1 layer from via layer)
p_cell	oxide between metal3 and metal4
silox	metal4 layer for ground ring
ewin	oxide between metal1 and metal4
met1	ground layer under interconnect
nbur	oxide under metal4 to metal3 via (at the end, do via-nbur-metal3-epoly)
epoly	via between metal3 and metal4
met3	metal1-metal4 stacks (interdigitated beams)
L_cell	substrate
csink	substrate etch
met2	metal2-metal3 stack in the actuators
varac	air
poly1	metal3 layer used between fingers and stator interconnect

- **Fix the material properties and the colors of layers.** Since HFSS does not recognize the color layers, they need to be fixed manually, How to change the properties of the layers is shown in [27]. After fixing the layers, use subtract function to finalize the layout layers described in Table 2-1.
- **Modify the options as shown in [27] to make a two-port s-parameter analysis.**
- **Do the analysis.**
- **Create the report.**

APPENDIX C

C.1 Matlab Code for Filter Simulation with Ideal Components

```
% Filter Topology1 Matlab Simulation File
c1=2.8e-12;
c2=c1/3;
%c2=305.408e-15;
c3=c1;
c4=c2;
%c4=342e-15;
%l1=1/(4.7e+9*2*pi)^2/c1*8
%l2=1/(4.7e+9*2*pi)^2/c1*7
l1=4.7e-9;
l2=3.7655e-9;
r=50;
f=linspace(45e+6,10e+9,3000);
w=f.*2.*pi;
vin1=1./(1+j*r.*w.*c1);
z1=r./(1+j*r.*w.*c1)+j.*w.*l1+1./(j.*w.*c2);
zc3=1./(j.*w.*c3);
vin2=vin1.*zc3./(zc3+z1);
z2=z1.*zc3./(z1+zc3)+j.*w.*l2+1./(j.*w.*c4);
s21_mag=abs(2*r./(z2+r).*vin2);%equation given (5.4)
s21_dB=20*log10(s21_mag);
plot(f,s21_dB,'g');
k1=find(s21_dB==max(s21_dB));
k2=find(s21_dB>-3.02 & s21_dB<-2.98);
f0=f(k1)%resonant frequency
BW=f(k2(2))-f(k2(1))%bandwidth
quality_factor=abs(imag((z2+r)./vin2))./abs(real((z2+r)./vin2));
      quality_factor3=f(k1)/BW%quality factor
```

C.2 Mathematica Code for 3rd Generation Filter

Figure 1 shows the code used to derive the transfer function of the filter topology shown in Figure 5-5. Firstly, the node equations are written in terms of the branch impedances. Secondly, the output voltage (Vout) is expressed in terms of input voltage (Vin) and other circuit components. The simplified and expanded transfer function equations are presented in Figure 1.

The denominator of the transfer function could not be simplified, hence, the code can not give the poles locations in terms of circuit components, explicitly. As shown in the figure, in the transfer function, there is only one zero, which is generated by the capacitors, C_2 and C_4, shown in Figure 5-5.

Figure C-1 Mathematica code used to derive filter transfer function

APPENDIX D

In this chapter, the test setups for MEMS capacitor, micromachined inductor test structures and third generation filter are described separately. The measurement procedure for every device is presented step by step.

D.1 MEMS Capacitor Measurement

Figure D-1 shows the test setup for MEMS capacitor test structure. One-port S-parameter test is performed by steps given below:

- The probes, cables and necessary connections are done properly as taught in the orientation of using probes station and network analyzer,
- GSG and EyePass probes are planarized by using contact substrate,
- SOLT calibration is performed using the calibration standard substrate kit (Network Analyzer Calibration Kit is used after defining the GSG probe standards as described in [28])
- One-port S-parameter data of open GSG pad is obtained by probing open GSG pad on the test chip, since the inductance of GSG pads are negligible, short GSG pad is not measured.

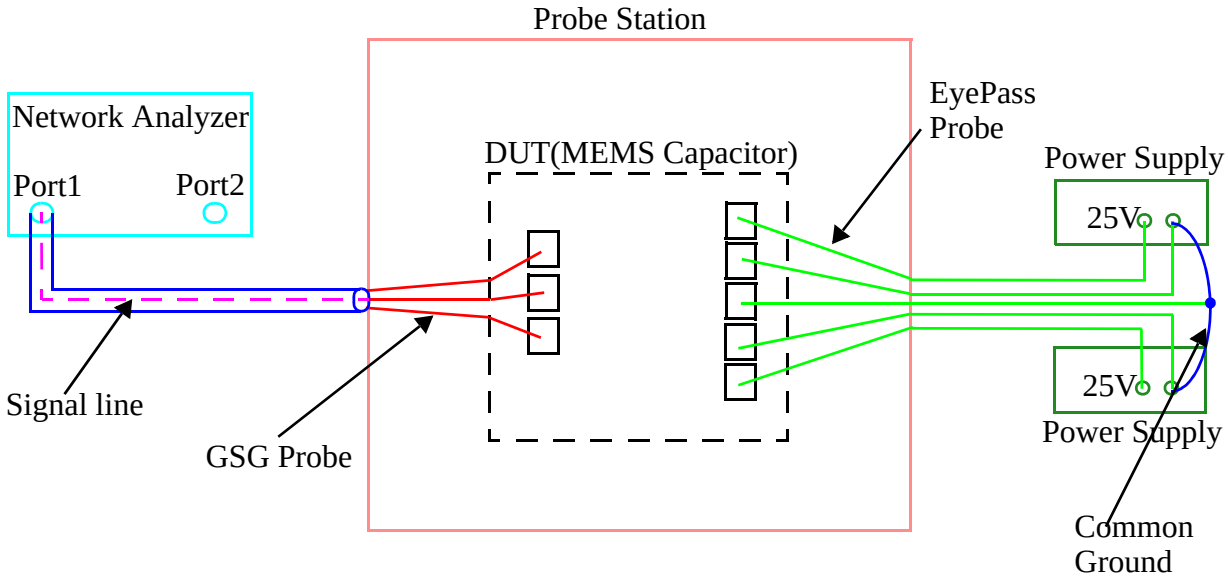


Figure D-1 MEMS Capacitor Measurement Setup

- GSG probe is landed on GSG pad, and EyePass Probe is landed on EyePass pads on MEMS capacitor test structure,
- The latch actuator is actuated by giving between 6-9V,
- One-port S-parameter data is obtained for both maximum and minimum capacitor conditions,
- The capacitance and quality factor of the MEMS capacitor tested is extracted using the code written in MATLAB,

D.1.1 MATLAB Code used to extract C and Q

```
[freq,s11_max1,s11arg_max1,s21_max1,s21arg_max1,s12_max1,s12arg_max1,s22_max1,
s22arg_max1]=textread('C:\Hasan\Capacitor\007_Test\De-Embed\pad_2_mat.txt',...
'%n %f %f %f %f %f %f %f %f',1601);
[freq,s11_min1,s11arg_min1,s21_min1,s21arg_min1,s12_min1,s12arg_min1,s22_min1,
s22arg_min1]=textread('C:\Hasan\Capaci-
tor\007_Test\007_Rel_Test5\min_mat.txt',...
'%n %f %f %f %f %f %f %f %f',1601);
s11_open=10.^(s11_max1/20).*cos(s11arg_max1/180*pi)+j*10.^(s11_max1/
20).*sin(s11arg_max1/180*pi);
s21_open=10.^(s21_max1/20).*cos(s21arg_max1/180*pi)+j*10.^(s21_max1/
20).*sin(s21arg_max1/180*pi);
s12_open=10.^(s12_max1/20).*cos(s12arg_max1/180*pi)+j*10.^(s12_max1/
20).*sin(s12arg_max1/180*pi);
s22_open=10.^(s22_max1/20).*cos(s22arg_max1/180*pi)+j*10.^(s22_max1/
20).*sin(s22arg_max1/180*pi);
y11_open=1/50*((1-s11_open).*(1+s22_open)+s12_open.*s21_open)./
((1+s11_open).*(1+s22_open)-s12_open.*s21_open);
y21_open=1/50*(-2*s21_open)./((1+s11_open).*(1+s22_open)-s12_open.*s21_open);
y12_open=1/50*(-2*s12_open)./((1+s11_open).*(1+s22_open)-s12_open.*s21_open);
y22_open=1/50*((1+s11_open).*(1-s22_open)+s12_open.*s21_open)./
((1+s11_open).*(1+s22_open)-s12_open.*s21_open);
s11_cap=10.^(s11_min1/20).*cos(s11arg_min1/180*pi)+j*10.^(s11_min1/
20).*sin(s11arg_min1/180*pi);
s21_cap=10.^(s21_min1/20).*cos(s21arg_min1/180*pi)+j*10.^(s21_min1/
20).*sin(s21arg_min1/180*pi);
s12_cap=10.^(s12_min1/20).*cos(s12arg_min1/180*pi)+j*10.^(s12_min1/
20).*sin(s12arg_min1/180*pi);
s22_cap=10.^(s22_min1/20).*cos(s22arg_min1/180*pi)+j*10.^(s22_min1/
20).*sin(s22arg_min1/180*pi);
y11_cap=1/50*((1-s11_cap).*(1+s22_cap)+s12_cap.*s21_cap)./
((1+s11_cap).*(1+s22_cap)-s12_cap.*s21_cap);
y21_cap=1/50*(-2*s21_cap)./((1+s11_cap).*(1+s22_cap)-s12_cap.*s21_cap);
y12_cap=1/50*(-2*s12_cap)./((1+s11_cap).*(1+s22_cap)-s12_cap.*s21_cap);
```

```
y22_cap=1/50*((1+s11_cap).*(1-s22_cap)+s12_cap.*s21_cap)./
((1+s11_cap).*(1+s22_cap)-s12_cap.*s21_cap);
y11_do=y11_cap-y11_open;
y21_do=y21_cap-y21_open;
y12_do=y12_cap-y12_open;
y22_do=y22_cap-y22_open;
z11=y22_do./(y11_do.*y22_do-y12_do.*y21_do);
z21=-1*y21_do./(y11_do.*y22_do-y12_do.*y21_do);
z12=-1*y12_do./(y11_do.*y22_do-y12_do.*y21_do);
z22=y11_do./(y11_do.*y22_do-y12_do.*y21_do);
y11=z22./(z11.*z22-z12.*z21);
y21=-1*z21./(z11.*z22-z12.*z21);
y12=-1*z12./(z11.*z22-z12.*z21);
y22=z11./(z11.*z22-z12.*z21);
go=1/50;
s11=((go-y11).*(go+y22)+y12.*y21)./((go+y11).*(go+y22)-y12.*y21);
s21=(-go*2*y21)./((go+y11).*(go+y22)-y12.*y21);
s12=(-go*2*y12)./((go+y11).*(go+y22)-y12.*y21);
s22=((go+y11).*(go-y22)+y12.*y21)./((go+y11).*(go+y22)-y12.*y21);
z11_num_max1=1+s11;
z11_denum_max1=1-s11;
z11_max1=50*z11_num_max1./z11_denum_max1;
Q_cap_max=-imag(z11_max1)./real(z11_max1);
C_max=-1./imag(z11_max1)./(2*pi*freq);
figure;
plot(freq,C_max,'r')
legend('Min 15.9v');
xlabel('Frequency');
ylabel('Capacitance');
figure;
plot(freq,Q_cap_max,'r')
legend('Min 15.9v');
xlabel('Frequency');
      ylabel('Quality Factor');
```

In this MATLAB code, the S-parameter data is saved for magnitude and phase mode. If the data is saved for real and imaginary mode, the code needs to be modified.

D.2 Micromachined Inductor Measurement

Figure D-2 shows the micromachined inductor measurement test setup. Two-port S-parameter test of inductor test structure is done by following the steps below:

- The probes, cables and necessary connections are done properly as taught in the orientation of using probes station and network analyzer,
- GSGSG probe tips are planarized by using contact substrate,
- SOLT calibration is performed using the on-chip calibration pads (short-open-load-through pads). Network Analyzer Calibration Kit is used after defining the GSGSG probe standards as described in [28]. The schematic of on-chip calibration pads are shown in Figure D-3. Since the calibration is performed by using on-chip open, short, load and through pads, it is not necessary to deembed the parasitics of the pads after making the measurement.

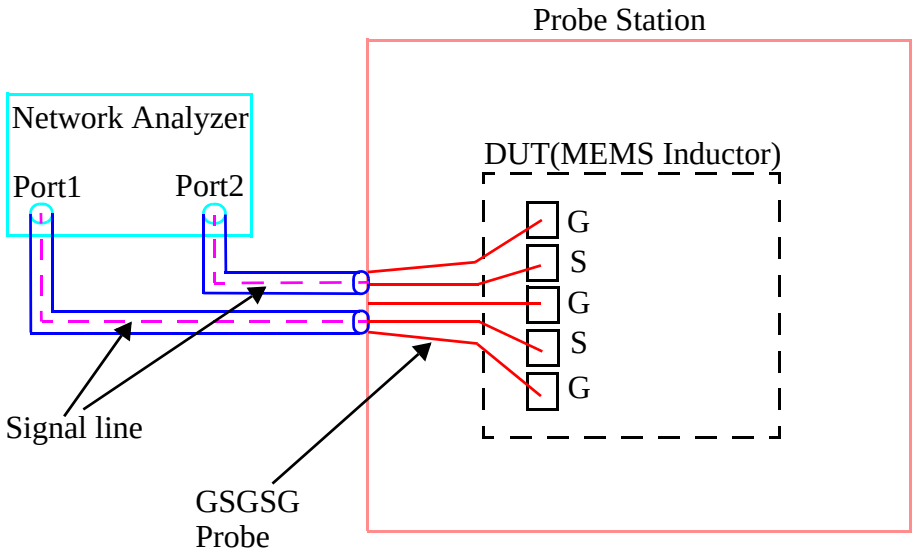


Figure D-2 MEMS Capacitor Measurement Setup

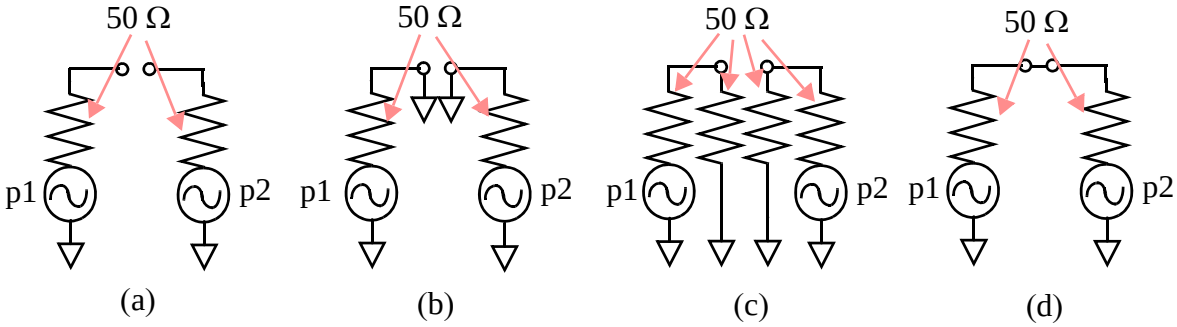


Figure D-3 (a) open (b) short (c) load (d) through schematic configurations of pads

- S-parameter data is obtained by landing GSGSG probe on GSGSG pads on micromachined inductor test structure.
- The inductance and quality factor characteristics are extracted using the Matlab code given in section.

D.2.2 Matlab Code used to extract L and Q

```
[freq,s11_1_real,s11_1_imag,s21_1_real,s21_1_imag,s12_1_real,s12_1_imag,s22_1_
real,s22_1_imag]=textread('C:\Documents and Settings\hakyol\My Docu-
ments\Hasan\Inductor\4nH_meas_all\4nh_ch1_mat.txt',...
'%n %f %f %f %f %f %f %f %f',1601);
[freq,s11_2_real,s11_2_imag,s21_2_real,s21_2_imag,s12_2_real,s12_2_imag,s22_2_
real,s22_2_imag]=textread('C:\Documents and Settings\hakyol\My Docu-
ments\Hasan\Inductor\4nH_meas_all\4nh_ch2_mat.txt',...
'%n %f %f %f %f %f %f %f %f',1601);
[freq,s11_3_real,s11_3_imag,s21_3_real,s21_3_imag,s12_3_real,s12_3_imag,s22_3_
real,s22_3_imag]=textread('C:\Documents and Settings\hakyol\My Docu-
ments\Hasan\Inductor\4nH_meas_all\4nh_ch3_mat.txt',...
'%n %f %f %f %f %f %f %f %f',1601);
s11_1=s11_1_real+j*s11_1_imag;
s21_1=s21_1_real+j*s21_1_imag;
s12_1=s12_1_real+j*s12_1_imag;
s22_1=s22_1_real+j*s22_1_imag;
sd_1=s11_1-s21_1;%for differential inductors
zd_1=2*50*(1+sd_1)./(1-sd_1);
Q_1=imag(zd_1)./real(zd_1);
L_1=imag(zd_1)./2/pi./freq;
s11_2=s11_2_real+j*s11_2_imag;
s21_2=s21_2_real+j*s21_2_imag;
s12_2=s12_2_real+j*s12_2_imag;
s22_2=s22_2_real+j*s22_2_imag;
sd_2=s11_2-s21_2;%for differential inductors
zd_2=2*50*(1+sd_2)./(1-sd_2);
Q_2=imag(zd_2)./real(zd_2);
L_2=imag(zd_2)./2/pi./freq;
s11_3=s11_3_real+j*s11_3_imag;
s21_3=s21_3_real+j*s21_3_imag;
s12_3=s12_3_real+j*s12_3_imag;
s22_3=s22_3_real+j*s22_3_imag;
sd_3=s11_3-s21_3;%for differential inductors
zd_3=2*50*(1+sd_3)./(1-sd_3);
Q_3=imag(zd_3)./real(zd_3);
L_3=imag(zd_3)./2/pi./freq;
```

```
figure;
plot(freq,L_1,'b',freq,L_2,'r',freq,L_3,'g')
legend('4nH chip1','4nH chip2','4nH chip3');
xlabel('Frequency');
ylabel('Inductance');
figure;
plot(freq,Q_1,'b',freq,Q_2,'r',freq,Q_3,'g')
legend('4nH chip1','4nH chip2','4nH chip3');
xlabel('Frequency');
ylabel('Quality Factor');
```

In this code, the inductance and quality factor characteristics of three different devices are extracted.

The code is written for real and imaginary mode S-parameter data.

D.3 Filter Measurement

Figure D-4 shows the third generation filter measurement setup. The steps given below describes the filter measurement procedure:

- The probes, cables and necessary connections are done properly as taught in the orientation of using probes station and network analyzer,
- GSG and EyePass probe tips are planarized by using contact substrate,
- SOLT calibration is performed using the on-chip calibration pads (short-open-load-through pads). Network Analyzer Calibration Kit is used after defining the GSG probe standards as described in [28]. The schematic of on-chip calibration pads are shown in Figure D-3.
- The validation of calibration can be checked by probing the open pad. When the pad is open, S11 data should be 0dB magnitude, and 0 degree phase. The calibration quality highly depends on the frequency range of the measurement and how well the contact was between probes and pads while doing the calibration.
- If the magnitude of S11 is lower than 0.05dB and the phase of S11 is lower than 1 degree when the probes are on the air, the calibration can be expected to be good enough.

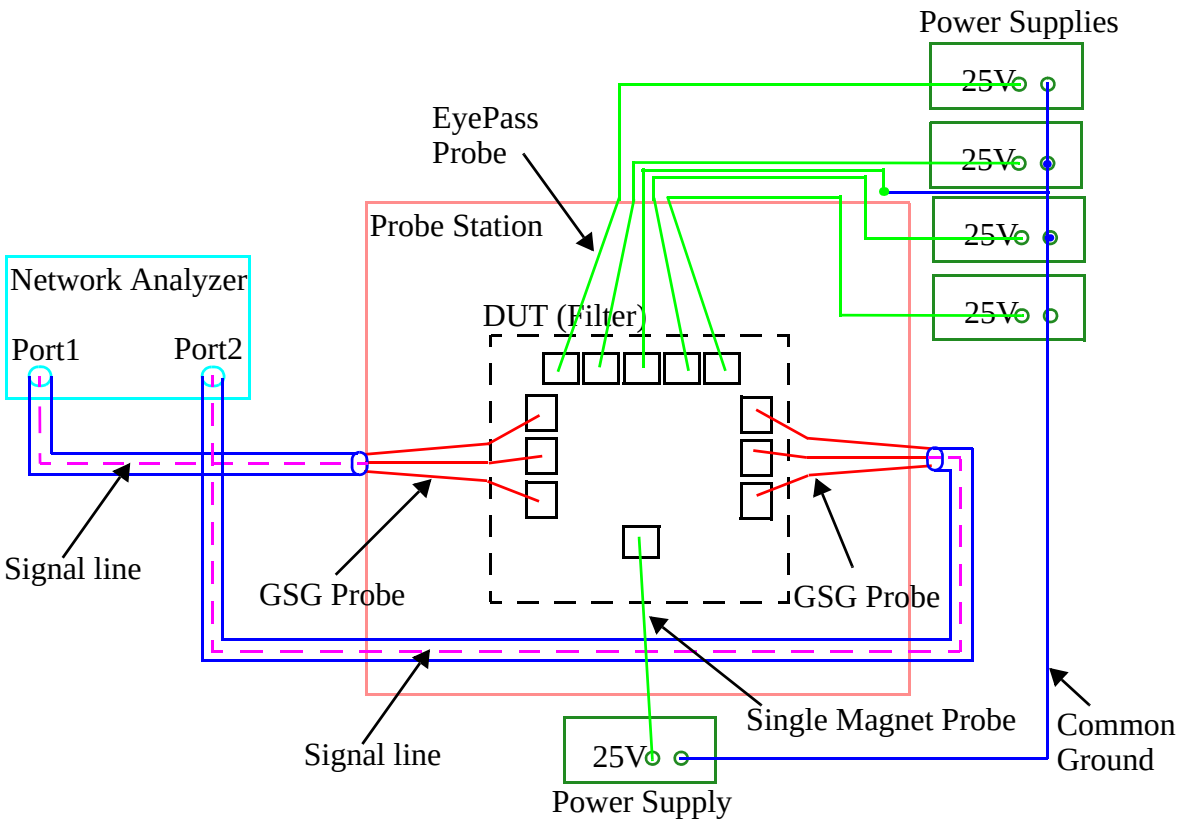


Figure D-4 MEMS Capacitor Measurement Setup

- After the calibration, the GSG probes can be landed on GSG pads of the filter, and EyePass probes can be landed on EyePass pads.
- Latch actuator for every capacitor is opened to move the fingers,
- S-parameter data for three frequency bands shown in Figure 5-1 can be obtained by moving the capacitor fingers to expected capacitance values,
- It has been experienced that the same chip can give different measured results by 2 dB with different calibration qualities.

APPENDIX E

In this chapter, the first measurement results third generation filter is presented with the SEM pictures taken from several locations of the filter. The measurement setup is shown in Figure D-3. The chip of which results are presented in this chapter is post processed in partially Carnegie Mellon University (oxide etch) and partially University of Florida (silicon etch).

E.1 Measurement Results

After the chip fabricated in the ST Microelectronics process is post-processed, some SEM pictures were taken. Figure E-1 shows SEM photos taken from the several locations of the filter. The photos show that there is considerable amount of polymer under all the structures and some silicon anchors under the

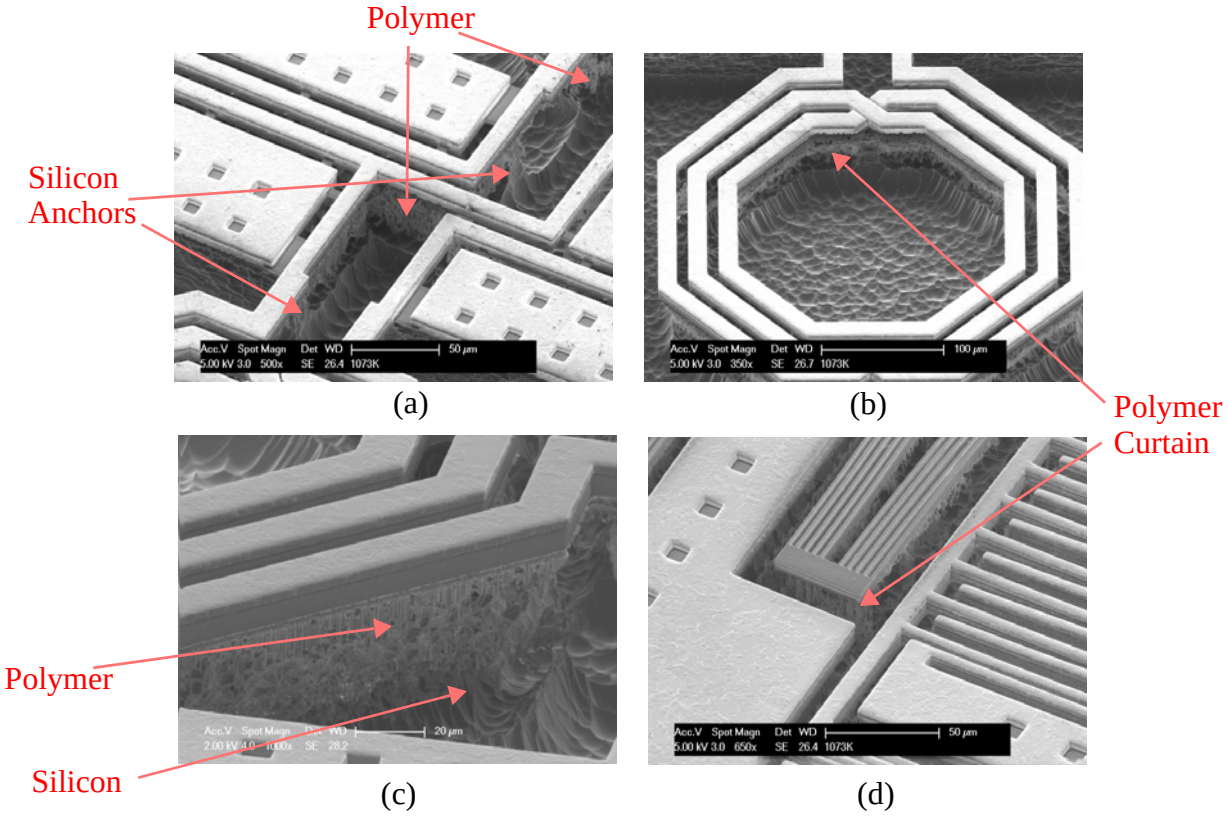


Figure E-1 SEM Pictures of (a) wiring interconnects (b) 3 nH inductor (c) arms of 3 nH inductor and (d) clutch actuator of the MEMS capacitor

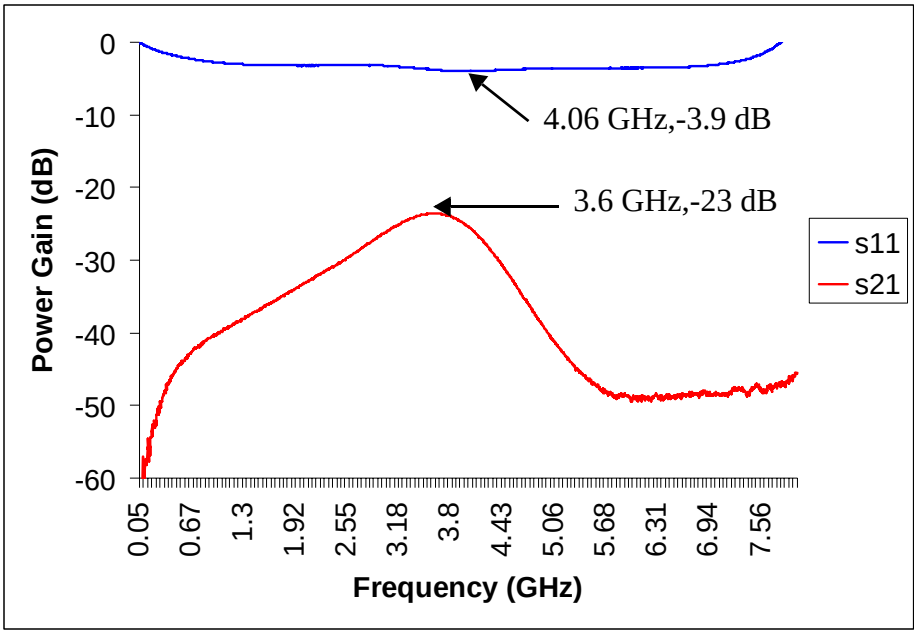


Figure E-2 SEM Pictures of (a) wiring interconnects (b) 3 nH inductor (c) arms of 3 nH inductor and (d) clutch actuator of the MEMS capacitor

signal lines which may cause crucial substrate coupling. Polymer curtains look sticked to the silicon substrate. Furthermore, the top metal surface is rough which may cause non-uniform resistivity along the signal lines. A two-port S-parameter measurement of the specific filter was performed using the network analyzer. Figure E-2 shows the measured S21 and S11 data. Although the actuation voltage is applied, the clutch and lateral actuators did not move. As seen in Figure E-2, the resonant frequency occur at 3.6 GHz, which means that the capacitance and inductance values are in the estimated range. However, the return loss of the filter is very big compared to expected value. The substrate coupling caused by polymer and silicon under the signal lines affect the insertion loss considerably. As the SEM pictures are considered, the measured results shown in Figure E-2 is much different than post layout simulations results shown in Chapter 5 and not reliable. After proper post-processing, the measurement results are expected to match the simulation results.