Large Angle Micro-Mirror Arrays in CMOS-MEMS

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Dedicated to my wife Elizabeth and my daughters Corinna, Vivienne and Xanthe. Their love and support made this possible.

Abstract

A 5 x 5 array of 800 μm x 800 μm micro-mirrors was designed and fabricated in CMOS-MEMS. Electrothermal bimorphs with embedded high resistivity polysilicon resistors were used as open loop actuators. The length of the actuators was set to 430 μm to achieve a maximum mirror mechanical rotation angle of ±45°, based on previously measured bimorph radii of curvature. Mirror deflection angles up to -23° and +15° were demonstrated at up to 15 V DC on individual array elements. Resonant modes were observed at 63 Hz, 183 Hz and 286 Hz compared with 51 Hz, 192 Hz and 263 Hz by simulation. Characterization of a full array of mirrors was not performed due to the mechanical fracture of the actuators under manual handling. Subsequent designs will address mechanical robustness and fill factor by decoupling the design of the actuator and the mirror.

Modal analysis of the design was performed using the finite element method. Thermal conductances of structural elements were determined using finite element analysis and then simulated as lumped parameter elements in equivalent thermal circuits using Spectre. DC and AC simulations were performed to assess the time constants and cross-talk of the actuators.

Post-CMOS processing of the mirrors consisted of direct write backside lithography, backside DRIE-Si etch with optical endpoint to target mirror thickness, frontside oxide etch and front-side silicon release etch. The structural dimensions resulted in a mechanically weak chip structure after silicon release etch. To compensate for this weakness a post-CMOS process compatible chip carrier was designed and fabricated. The mirror-array chip was mounted in the chip carrier prior to front-side silicon release etch and secured using SU8 epoxy. The chip remained in the carrier for final packaging and test.

1 Introduction

"There is no permanently wise <person>, but <people> capable of wisdom, who, being put into certain company, or other favorable conditions, become wise for a short time, as glasses rubbed acquire electric <charge> for a while."

Ralph Waldo Emerson (1870)

1.1 Motivation

Leucippus, in the 5th century before the Common Era, is generally accepted in the Western tradition as having opened the field of rational enquiry into the realm of the imperceptibly small[1], although the origination is often attributed to the more familiar Democritus. In more recent times it was recognized that an atomist tradition, documented in the Vaisesika, arose independently in classical Indian philosophy, possibly prior to the Greek[2]. This ancient co-origination demonstrates the allure of the microscopic world on the human imagination and that these early atomists can be credited with sparking the desire of humanity to gain direct knowledge of the world within our own.

The invention of the microscope in the 17th century opened a window of observation into the microscopic world, but it was not until the 20th century that the technologies were invented which enabled humanity to directly sense and interact with matter on the this scale. It was Richard Feynman in his famous 1959 lecture at Caltech, "There's Plenty of Room at the Bottom,"[3] who illustrated some of the benefits to gain from making machines that operate on the scale of "mites". In this talk, Prof. Feynman described in notional terms how such mite-sized machines could be made using tech-

nology within the reach of his audience and in doing so inspired the generation of engineering leaders who began the development of MEMS (**M**icro**E**lecto**M**echanical **S**ystems) technology. His audience went on to use the planar technology of the developing microelectronics industry to produce devices, such as the resonant gate transistor[4] and the gas chromatograph[5], that used size reduction to gain an advantage over the existing technology. The pioneers in the field demonstrated the richness of devices the technology could produce and its ability to perform actuation as well as sensing[6][7], while later investigators devised a methodology to explore and demonstrate the scaling benefits of MEMS in terms of speed, energy density and force[8].

Since the days of Feynman's talk MEMS have found application where small size, weight and intrinsic speed are critical system enablers, or where advantageous power and force scaling makes possible the detection and transmission of signals outside the range of macroscopic systems. To realize the full potential of MEMS it is necessary to explore the limits of device and fabrication technology and to understand where the advantages and disadvantages of MEMS lie. The motivation for the work described in this report was to push the boundary on array size for large angle, electrothermally actuated micromirrors in CMOS-MEMS (**C**omplementary **M**etal-**O**xide-**S**emiconductor **MEMS**) using the 0.35 μm JAZZ Semiconductor foundry CMOS Si-Ge technology and to maximize mirror fill factor while maintaining a minimum of video-rate scanning speeds.

The goal of the project described in this report was to design an 800 μm x 800 μm rigid, optically flat mirror that could be actuated through a deflection angle of ±45° about its centroid and tiled in a 5 x 5 array to achieve a fill factor goal of 80%. The specification for actuation voltage was less than 15 V.

1.2 Historical Perspective on Optical MEMS

Mirrors and gratings are the basic building blocks with which an assortment of optical systems can be built. The optical sub-family of MEMS is called MOEMS (**M**icro-**O**pto **E**lectro**M**echanical **S**ystems), a term that encompasses all MEMS devices that interact with the optical and infrared regions of the electromagnetic spectrum. MOEMS today can be found in medical imagers[9], projection displays[10], adaptive optics[11], optical scanners[12], beam steering applications[13] and free-space optical communications systems[14]. The following section will present the development of optical MEMS components and show the evolutionary path to the work described in this report.

In 1969, Preston[15] demonstrated a 1600 pixel "membrane light modulator" (MLM) for optical computing that consisted of a 0.1 μm thick, metallized polymer film suspended on a 1 μm thick SiO_2 film with 10 μm diameter "perforations" on a 100 μm pitch over Au/Cr stripes patterned on a glass substrate. In 1970, van Raalte[16] demonstrated a "new Schlieren light valve" for projection displays, similar in cross-section to the MLM but using a 0.2 μm Ni film suspended on a 5 μm thick Al grid.

Optical devices that are now regarded as MEMS devices first appeared later in the 1970's under the impetus of the interest in projection displays and coherent optical data processing. They were based on post-mounted, deformable reflective plates[17] and cantilever beams[18], respectively. A parallel research path was opened in 1980 when Petersen[19] fabricated a single, bulk-Si torsional scanning mirror. In 1982, Hornbeck reported on an electronically addressable, pixelated membrane[20] and several years later with Wu, et al.[21] on an improved device that replaced the flexible membrane with a hinged, rigid tilting mirror that evolved into Texas Instrument's DLP (Digital Light Processor). Solgaard, et al. in 1992 reported a final canonical form, the deformable grating optical modulator[22], that comprised an array of fixed-fixed, Al coated silicon nitride beams suspended ~0.20 μm over a continuous lower electrode. The seminal devices listed above were electrostatically actuated, with deflections < 5 μm and scanning angles < 6°, a wide range of resonant frequencies (30 Hz to 6 MHz), array sizes (standalone devices up to arrays of 200 000 devices) and actuation voltages (3.2 V to 5000 V).

The use of bimorph and multimorph actuators (i.e. single beams consisting of two or more thin film materials with a mismatch in physical properties) in optical MEMS devices was introduced in 1989 by Ono[23] when he reported 1-D and 2-D, 3 mm x 3 mm optical beam deflectors using piezoelectric bimorphs that achieved ~1° angular displacement at ~3 kHz. In 1992, Buser, et al.[24], used mismatch in temperature coefficient of expansion between Al and Si to actuate a biaxial scanning mirror for a keratotomy system. They employed a custom-process multimorph that comprised a top layer of 6 μm of Al on 0.15 μm of silicon nitride, 0.38 μm of silicon dioxide and 10 μm of single crystal silicon attached in various configurations to ~1 mm x 1 mm Al coated Si mirrors. Joule heating in the Al and Si layers of the multimorph, henceforth referred to as electrothermal actuation, was used to stimulate the actuator leading to a 4° deflection angle at 15 Hz resonant frequency.

Buhler, et al.[25], in 1995, following the approach of Buser, et al. demonstrated electrothermally actuated mirrors using foundry CMOS processing as the base fabrication technology, while releasing the mirrors and actuators using post-CMOS surface micromachining. Buhler's devices used Al and silicon dioxide bimorphs with embedded polysilicon heaters attached to 35 μm x 40 μm mirror plates formed of silicon dioxide and Al and achieved up to 4.6° static deflection angles at 5 mW. Xie, et al.[26], refined the design of electrothermally actuated CMOS-MEMS mirrors using concepts described by Lammel, et al.[27], to produce 1 mm x 1 mm, Al coated, bulk-Si mirrors with static angular deflections[1] up to 15° at 350 mW for use in optical coherence tomography imaging systems. The work described in this paper follows directly from Xie's, thus the conceptual evolution from the seminal work in the field to that of the author is charted.

1.The literature variously uses the terms scanning angle, optical scanning angle, mechanical scanning angle, rotation angle, deflection, angular deflection and angular displacement to describe the rotational motion of a mirror under actuation. In the remainder of this report, the terms deflection angle, static deflection angle and dynamic deflection angle will be used to refer to the angle through which a mirror has rotated.

1.3 Actuation and Application

The devices discussed in section 1.2 can be categorized according to the motion they exhibit: piston, rotation or a weighted combination of both. In adaptive optics, piston motion is required to modify the phase of an optical wavefront without affecting its direction, and is thus also known as phase-only motion. In free-space optical communication and beam steering applications centroidal rotational motion is desired to change the direction in which a beam of light is moving while minimizing the effect on its phase. In imaging applications, a combination of phase and direction modification may be desired. Electrostatic and electrothermal actuation are the most common methods of optical MEMS actuation, but piezoelectric, electromagnetic[28] and electrocapillary[29] actuation have also been reported in the literature and are the subjects of active research. Electrostatic actuation is the preferred method when small motions (< 5° scanning or < 5 μm piston) are acceptable and operating frequencies > 10 kHz are required. For applications that require larger motions, electrostatic actuation becomes impractical as the actuation voltage increases with electrode separation. Electrothermal actuation is chosen for large motions and when operating frequencies less than ~3 kHz are acceptable.

1.4 CMOS-MEMS

CMOS is currently the dominant technology for producing integrated circuits (IC's). Over the past 46 years increasing commoditization of IC's drove down unit cost and propelled circuit density according to Moore's law[30], and forced improved reproducibility and robustness in the manufacturing processes used to fabricate the devices. Statistical process control (SPC) techniques were introduced in the 1980's to improve production yield and device reliability[31] for process flows that typically numbered several hundred unit-process steps. Advanced equipment and process control (AEC/APC) emerged in the 1990's, enabled by improved data acquisition, storage and processing capabilities. It was introduced into volume processor and DRAM production[32] in the late 1990's and early 2000's. The change in fabrication paradigm also led to the integration of new sensing modali-

ties[33] to address non-process based yield and reliability detractors. The evolved stability and robust-ness of CMOS processing are leveraged to rapidly prototype MEMS devices integrated with electronics in a device technology called CMOS-MEMS.

CMOS-MEMS denotes the use of CMOS back-end thin film layers to form MEMS structures. Fol-lowing completion of CMOS fabrication, typically performed by foundries using standardized pro-cesses, MEMS devices are made monolithically from the CMOS dielectric and passivation layers. These structures are then "released" from the substrate in what is known as post-CMOS processing by selectively removing the films surrounding the MEMS device, then undercutting it using a wet or dry etch process. This concept was first described by Parameswaran, et al.[34] for the formation of two types of homogeneous structures: polysilicon structures, for which the underlying dielectric was the release layer, and dielectric structures, for which the silicon substrate was the release layer. Parameswaran's structures consisted of a single material and did not lead to patterning of the underly-ing materials, which were completely removed from under and around the MEMS structures. At CMU, in contrast to Parameswaran's structures, metal interconnect layers serve both as etch masks and struc-tural layers of the MEMS devices, while the silicon substrate acts as the release layer. By selective, anisotropic silicon dioxide and silicon etching, the uppermost metal layer in the stack masks the under-lying dielectric, polysilicon and silicon layers, which are retained as part of the final structure. The presence of materials of widely differing physical properties provides the designer with additional degrees of freedom in mechanical compliance and electrical and thermal conductivity, enabling the creation of a rich diversity of devices.

1.5 Outline of This Report

In Chapter 2, the principles of operation and the design of electrothermally actuated mirrors will be discussed. Analytical equations, finite element analyses and lumped parameter simulations will be pre-sented.

Chapter 3 provides detailed technical information about CMOS-MEMS device fabrication. It covers the fabrication of the mirrors, a novel process control method for backside silicon etch depth and the design and fabrication of a carrier chip needed to enable full scale mirror deflection angle. CMOS processing will not be discussed and it will be assumed that a diced CMOS chip is the starting substrate. The post-CMOS process flow will be discussed in some detail.

Chapter 4 contains experimental data showing the performance of the devices. DC and AC tests were performed on mirrors from two different device designs: (a) working mirrors from two 5 x 5 arrays of 800 μm x 800 μm mirrors and (b) a 2 x 2 array of a reproduced design from Xie[26].

Chapter 5 discusses the conclusions of this work and the future directions that will be followed to explore the design and fabrication space for arrays of large, electrothermally actuated mirrors.

2

Principles of Operation and Design

2.1 Electrothermally Actuated Mirror Design

In this chapter the design considerations for an electrothermally actuated micromirror in CMOS-MEMS will be discussed. The concept for the actuation of the mirror and its operation are shown in Figure 2.1. The SEM images of the mirror show it in its rest state, so note the actuators are curled in the absence of stimulation. The mirror is connected to the actuators at its midpoint to minimize non-rotational motion during operation. On each side of the mirror there is an actuator for positive angular motion and a second actuator for negative angular motion. The positive and negative actuators are thermally isolated from each other so that when one is heated it will flatten while the other remains curled. In this way, the angle at the tip of the unactuated beam is converted to a mirror deflection angle.

The design elements to achieve the project objectives stated in Section 1.1 are the geometry and composition of the electrothermal actuators, the geometry and composition of the thermal isolation, the resistance and location of the embedded heaters and the layout of the mirror within the frame. Analytic expressions based on the physics governing the behavior of the elements, finite element analysis and lumped parameter analysis will be used to develop the design.

FIGURE 2.1 *(a) Plan view of the micromirror schematic showing a mirror connected to the anchor region on two sides by a pair of series connected electrothermal actuators. The tip angle of an actuator is converted to mirror rotation by a mismatched thermal expansion in the layers of the actuator beam when Joule heating occurs in resistors embedded in the beam. (b) SEM of a single mirror pixel of the fabricated array. (c) Close-up SEM of the actuators.*
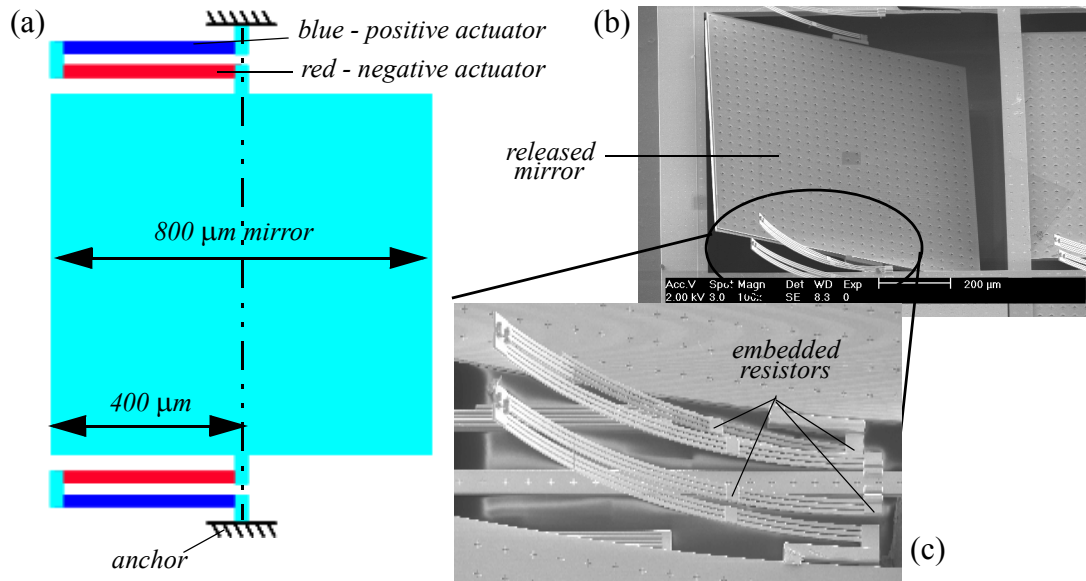
2.2 Actuator Mechanical Design

2.2.1 MEMS Beam Descriptions

Beams, plates, anchors and gaps are parameterized, reusable "atomic" elements in composable MEMS design[35] analogous to resistors, capacitors and other standard circuit elements in electrical design. The behavioral characteristics of an atomic element can be extracted from coupled, multiphysics finite element analysis[36] or derived analytically from the domain-specific physics of the element. In MEMS, typical domains include electromagnetic, mechanical and thermal but can also include chemical, optical and fluidic domains. Coupling of domains in an atomic element suggests movement of energy from one domain to another. For example, in the electrothermal actuators that will be discussed in this chapter, current passing through a resistor converts electrical energy to the thermal

domain, and the thermal energy causes bending in the bimorph, indicating movement of energy from the thermal to the mechanical domain.

Once the behavioral characteristics of an atomic element are described mathematically, they can be encoded in an analog hardware description language (AHDL) such as Verilog-AMS[37]. The atomic elements so constructed can be interconnected, or composed, into network schematics representing a complex system, arranged hierarchically into components and subsystems and simulated using a simulator such as Spectre or Spice to evaluate DC, AC and transient performance[38]. Iteration on this process and comparison of simulation results with test structure characterization prior to fabrication comprises a structured design methodology that increases the probability of generating a functional device. This approach will be utilized to perform equivalent thermal simulations to analyze dynamic thermal response of electrothermally actuated micromirrors, although the step of model validation with test structures was not performed due to project constraints.

In order to begin the discussion of MEMS design using atomic elements it is necessary to define a standard representation for them. Jing[35] initially defined mechanical and electrical beam and plate models in NODAS at CMU using Verilog-A. Wong[39] extended the capability of the NODAS beam model, based on analyses by Iyer[40] and Lakdawala[41], to account for in-plane bending under the action of thermal stresses arising due to laterally offset members in the beam. The model was validated against devices produced by Oz[42]. The author redefined the geometric representation of the beam model in Verilog-AMS for the four conductor JAZZ Semiconductor technology to accommodate unconventional beam cross-sections and to model out-of plane bending due to thermally induced and residual stresses. The new model was validated against the devices produced by Oz[42] according to the method applied by Wong[39] for in-plane bending.

Schematic transverse cross-sections of a conventional MEMS beam and an unconventional MEMS beam after structural release etch are shown in Figure 2.2. The geometric parameters that uniquely define the beam in NODAS are shown in Figure 2.3. This representation and the geometric parameters

FIGURE 2.2 *(a) Transverse schematic cross-section of a conventional MEMS beam after release etch formed from metal 4, metal 3, metal 2 and metal 1 with embedded polysilicon on gate oxide. It is conventional in the respect that the top layer of metal fully defines the geometry of the beam. A titanium-based barrier metal exists under metal 3, metal 2 and metal 1, but is not shown here. (b) Transverse cross-section of an unconventional beam after release etch formed by the same four metal layers. The beam is formed over field oxide.In this case the widths and relative locations of the various metal members of the beam define its geometry. Designers in CMOS-MEMS have at their disposal the combination of metal layers within the beam, their respective widths, relative locations and beam length. (c) Boolean description of MEMS beam in (b). "1" indicates the presence of a layer, "0" indicates the absence of a layer. Absence of field oxide implies presence of gate oxide if poly is present.*
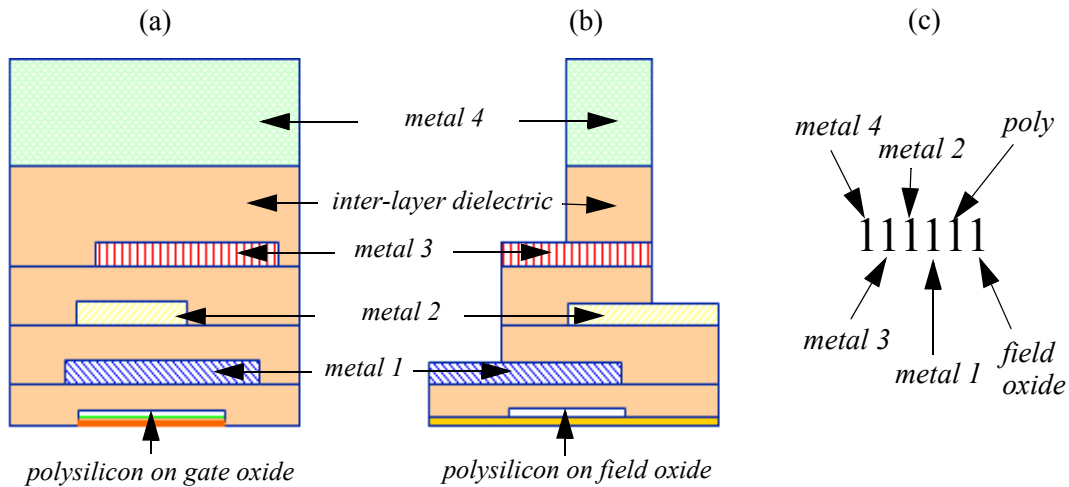
shown in the figure will be used throughout the report. Additionally, the term "member" will be used to refer to a distinct section of a single material within a layer of the beam. For example, at the level of the metal 1 layer in the conventional beam of Figure 2.2 (a) there is a metal member, and one oxide member both to the right and left of the metal. A shorthand notation for describing a beam's composition is to list the metal layers within it. For example, the beams in Figure 2.2 would both be described as metal-4321 beams with embedded poly on active and field, respectively (or using a Boolean notation as 111110 and 111111). Discussion of the model code is beyond the scope of this report but note that the geometric parameters, specified by the user and defined in Figure 2.3, and a flag parameter for field oxide are used to determine the presence, absence and relative positions of each member of a beam. A titanium-based barrier metal layer is present underneath the metal 3, metal 2 and metal 1 layers. This layer is not shown in Figure 2.2, or Figure 2.3, as its thickness is on the order of 10's of

nanometers and its effect on the mechanical and thermal behavior of the beam is considered negligible

in comparison to the aluminum and oxide layers.

FIGURE 2.3 *The total footprint width, w, of a beam, the width of the individual metal members of the beam, w_m*, and the offsets of the metal members, ol_m*, from the left reference edge are sufficient design parameters to uniquely describe a MEMS beam. In CMOS-MEMS, the thickness of each metal and dielectric layer is fixed by the foundry and the designer has control only over the layers included in the beam. The thickness parameters for the other metal, ILD and field and gate oxide are not shown in the diagram in order to reduce clutter but, follow the same naming convention as metal 4 thickness and metal4-3 ILD. The axes overlaid on the cross-section define the orientation of a beam for the purpose of subsequent analytical expressions.*
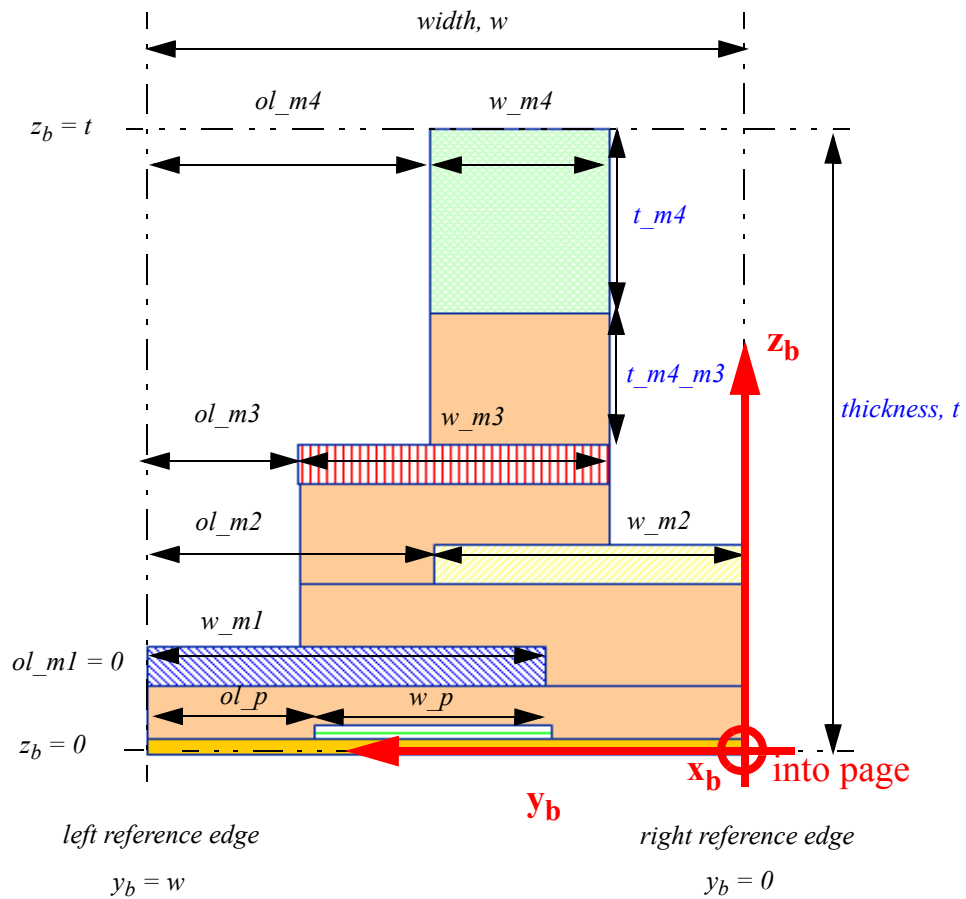
2.2.2 Electrothermal Bimorph Actuators

Timoshenko[43] developed a general theory for bending in bi-metal strips, or bimorphs, subjected to uniform heating from an initial temperature, T_0, to a final temperature, T, which related the in-plane film stresses due to thermal expansion to an unbalanced moment about an intersection of orthogonal longitudinal planes that define the neutral axis of the beam along its length. For out-of-plane bending about the y-axis, the position, z_c, of the neutral axis with respect to the base of the beam is

$$z_c = \frac{\int_0^w \int_0^t E z_b \, dy_b dz_b}{\int_0^w \int_0^t E \, dy_b dz_b} \tag{2.1}$$

A directly analogous expression exists for the position of the neutral axis in y. To simplify the analysis, the members are assumed discrete, the material of a member homogeneous and its properties uniform. These assumptions reduce (2.1) to a summation over the individual members of the beam.

The thermally induced radius of curvature, ρ_{th}, of the heated (or cooled) beam is

$$\rho_{th} = \frac{\frac{t}{2} + 2\frac{(E_{ox}I_{y,ox} + E_{Al}I_{y,Al})}{wt}\left(\frac{1}{E_{ox}t_{ox}} + \frac{1}{E_{Al}t_{Al}}\right)}{(\alpha_{ox} - \alpha_{Al})(T - T_0)} \tag{2.2}$$

where α is the thermal coefficient of expansion (TCE), E is the Young's modulus, and $I_y = \frac{wt^3}{12}$ is the bending moments of inertia of each layer in the bimorph for bending in the z-direction. The layers of the bimorphs in this report are aluminum and silicon dioxide and will be denoted by the subscripts "Al" and "ox". This equation contains the kernel of the design consideration for an electrothermal actuator in which it can be seen that the thermomechanical gain of the beam is proportional to the difference in the TCE's of the beam members.

With reference to Figure 2.4, Euclidean geometry and (2.2) enable the MEMS designer to relate tip angle $\theta_{th} = \frac{L}{\rho_{th}}$ and tip displacements in-plane $(x_{tip} = L - \rho_{th}\sin\theta_{th})$ and out-of-plane $(z_{tip} = \rho_{th}(1 - \cos\theta_{th}))$ to temperature change and thermal coefficient of expansion (TCE) of the

materials of the bimorph. For example, consider a 100 μm long CMOS-MEMS bimorph formed from metal 1 and the underlying oxide layers, with $\alpha_{ox} = 0.5$ x 10^{-6} K^{-1}, $\alpha_{Al} = 23.1$ x 10^{-6} K^{-1}, $E_{ox} = E_{Al}$ [44], and $t_{Al} = t_{ox}/2 = 0.5$ μm. To achieve a tip angle of ~ -30° and assuming no other sources of in-plane stress, the bimorph must be cooled by ~ 230 K.

FIGURE 2.4 *Radius of curvature and tip displacement of a two member cantilevered electrothermal beam. L is the length of the beam. The beam is anchored at $x_b = 0$. The center of curvature, z_o defines the sign convention for (2.2) such that ρ_{th} is signed positive for positive z_o. Deflection angles follow a right hand rule about the y_b axis such that the sign of θ_{th} is negative for the configuration shown.*
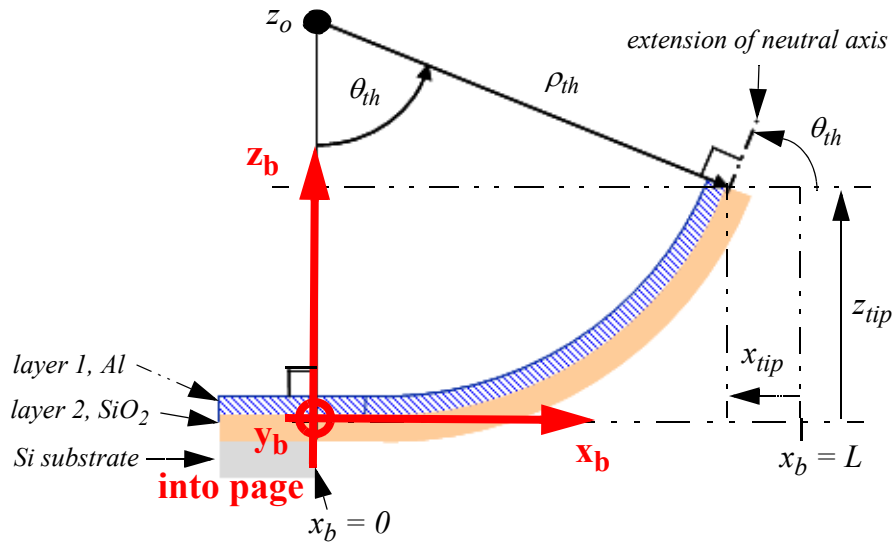
2.2.3 Residual Stress and Self-Assembly

CMOS fabrication processes lead to in-plane film stresses arising from the thermal characteristics of the deposition or growth of the materials and/or the respective materials' structural and chemical properties[48]. These stresses are "locked" into the films by the rigid silicon substrate on which they are deposited. During MEMS post-CMOS processing the rigid silicon substrate is selectively removed and the actuator structures are completely undercut (i.e. all structural silicon is removed from under them). At the moment of structural release, the residual stresses are relieved by bending under the action of the moment arising from the residual stress gradient in the structure[45]. MEMS terminology

for the phenomenon of actuation due to intrinsic physical mechanisms without direct human intervention is known as "self-assembly".

Timoshenko's theory of bending in a bimorph mentioned in Section 2.2.2, and the extension to multimorphs[45], can be applied directly to obtain an analogous expression for the bending in a beam due to residual stress. In general beam theory, when a beam is subjected to an applied moment it will bend until the applied moment is balanced by the internal moment due to flexural rigidity. Thus, the radius of curvature of a beam is related to the applied moment, M, and the effective stiffness, $(EI)_{eff}$, of the beam by $\frac{1}{\rho} = \frac{M}{(EI)_{eff}}$. Similar to thermally induced moments, the moment arising due to a residual stress distribution, $\sigma_{res}(y,z)$, is taken about the neutral axis. Out-of-plane bending is caused by a moment about the y-axis, $M_{y,res}$,

$$M_{y,res} = \int_{-z_c}^{t-z_c} \sigma_{res}(z)z\,dz\,dy. \tag{2.3}$$

As the Young's moduli for SiO_2 and Al are approximately equal (i.e. $E_{Al} = E_{ox} = E$), (2.1) places the neutral axis at the geometric center of the beam (i.e. $z_c = t/2$). The assumption that the stress distribution within a discrete member is constant, (2.3) for the bimorph in Figure 2.4 leads to

$$M_{y,res} = \frac{w t_{Al}(t - t_{Al})}{2}(\sigma_{res,Al} - \sigma_{res,ox}) \tag{2.4}$$

where $\sigma_{res,ox}$ and $\sigma_{res,Al}$ are the residual stresses in the SiO_2 and Al, respectively. Analysis of (2.4) shows that the maximum moment is obtained when the dimensions of the aluminum member and the silicon dioxide member of the bimorph are equal. In general, for maximum mechanical response, the members of the bimorph should be confined to opposite sides of the neutral axis.

The radius of curvature of the bimorph after release due to residual stress is

$$\rho_{res} = \frac{(EI)_{eff}}{M_{y,res}} = \frac{Et^3}{6t_{Al}(t - t_{Al})(\sigma_{Al} - \sigma_{ox})}. \tag{2.5}$$

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The reader should note the reversal in sign of the moment in the derivation of the radius of curvature between (2.5) and (2.2). The reason for this is that in the residual stress case, the substrate applies an external moment on the beam which is balanced by an internal moment of equal magnitude, whereas in the case of thermal stress, the internal moment develops in response to the applied thermal moment. For the bimorph of Figure 2.4 the thermal moment is given by

$$M_{y,th} = \frac{wt_{Al}(t-t_{Al})E}{2}(\alpha_{Al} - \alpha_{ox})\Delta T, \tag{2.6}$$

and the thermally induced radius of curvature, derived for completeness by substituting σ_{res} in (2.3) with the expression for thermal stress, $\sigma_{th} = \alpha E(T-T_0) = \alpha E \Delta T$ is

$$\rho_{th} = \frac{-(EI)_{eff}}{M_{y,th}} = \frac{t^3}{6t_{Al}(t-t_{Al})(\alpha_{ox}-\alpha_{Al})\Delta T}. \tag{2.7}$$

The tip displacement, $z(L)$, and tip angle, $\theta(L)$ as a function of the moments applied to the beam were derived using a polynomial shape function, $z(x) = Ax^2 + Bx + C$, with cantilever boundary conditions leading to

$$z(L) = z_{tip} = \frac{3t_{Al}(t-t_{Al})(\sigma_{res,Al}-\sigma_{res,ox})}{Et^3}L^2, \text{ and} \tag{2.8}$$

$$\theta(L) = \frac{6t_{Al}(t-t_{Al})(\sigma_{res,Al}-\sigma_{res,ox})}{Et^3}L. \tag{2.9}$$

Rearranging (2.8) enables extraction of radius of curvature from tip displacement measurements on test structures by $\rho = \frac{L^2}{2z_{tip}}$. These equations show that the designer of out-of-plane electrothermal CMOS-MEMS actuators has one parameter, the beam length, with which to select a tip displacement or a tip angle.

Table 2.1 contains derived radii of curvature for a variety of compositions of conventional MEMS beams. For the purposes of this project, an m1 on field oxide beam was chosen for the actuator as it has the smallest radius of curvature, which led to the shortest beam for a desired tip angle and hence improved fill factor. This is a trade-off with mechanical robustness as a m1 beam is the least stiff of all

the possible configurations. Figure 2.5 shows a white light interferometer scan (WYCO NT3300) of a conventional MEMS beam after structural release. A fitting function was used to determine the radius of curvature of the beam. Using this radius of curvature, a 432 μm beam was required to achieve a tip angle of 45°.

TABLE 2.1 *100 μm long JAZZ process cantilever beam test structure tip displacements measured using WYCO white light interferometer. (The structures were formed on jz60_p012a in cell ts_vcurl.)*

beam type	boolean	z_{tip} (μm)	ρ_{res} (μm)
metal 1 on field oxide	000101	8.5	590
metal 1 on field with poly	000111	7.3	685
metal 1 on active	000100	2.0	2500
metal 1 on active with poly	000110	-2.1	-2380
metal 1 on active with diffusion contacts	000100	1.5	3335
metal 21 on field with poly and vias	001111	2.7	1850
metal 21 on field with poly	001111	2.5	2000
metal 21 on field with vias	001101	3.8	1315
metal 21 on field	001101	3.6	1390

FIGURE 2.5 *The graph shows a line scan of an m1 beam on field oxide (000101) formed using the JAZZ Semiconductor foundry process. The scan data was obtained using a WYCO NT3300 white light interferometer. A fitting function was used to derive a radius of curvature of 550 μm. Courtesy G. K. Fedder.*
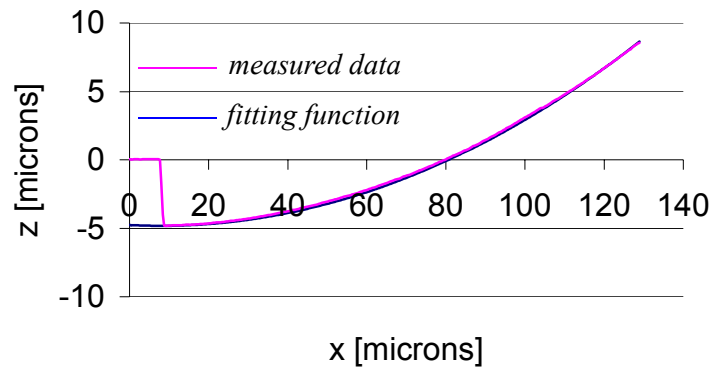
2.3 Thermal Stimulation and Isolation

2.3.1 Temperature Change for Full Scale Deflection

To actuate the mirror in Figure 2.1, it is necessary to raise the temperature of the bimorph to induce the thermal moment that bends the beam. Due to residual stress in the bimorph layers, the beams are bent with constant curvature at room temperature according to (2.5). When the actuators are heated, the total moment on the beam is the sum of the moment due to residual stress and the thermally induced moment. The radius of curvature, ρ, of the beam at a given temperature is given by $\frac{1}{\rho} = \frac{1}{\rho_{res}} + \frac{1}{\rho_{th}}$, which Xie, et al.[47] showed holds for the average beam temperature, thus accounting for non-uniform temperatures along a beam. To reach the designed deflection angle, the actuator must have an infinite radius of curvature, so $\rho_{th} = -\rho_{res}$. The temperature change, ΔT, to achieve this condition is given by

$$\Delta T = \frac{t^3}{6\rho_{res,\,meas}t_{Al}(t - t_{Al})(\alpha_{Al} - \alpha_{ox})}. \tag{2.10}$$

Using the measured value of ρ_{res}, the previously reported TCE's, $t_{Al} = 0.65$ μm and $t = 1.2$ μm, the temperature change for full scale deflection is $\Delta T = 65°$ C. The reader should note that by increasing the temperature beyond this value, the mirror will rotate through a deflection angle greater than the designed value.

2.3.2 Heat Flow

"Heat is thermal energy in transit due to temperature difference."[46] Heat flows by conduction, convection and radiation in relative quantities determined by the physical properties and states of the materials between which a temperature difference exists. For solid MEMS devices, conduction is the predominant mode of heat transfer. Heat transfer by conduction is governed by

$$\nabla \bullet (\kappa \nabla T) + \dot{Q} - \rho C_p \frac{\partial T}{\partial t} = 0, \tag{2.11}$$

where ρ is density in this context, κ is the thermal conductivity, C_P is the specific heat capacity at constant pressure and $\dot{Q}$ is the rate of heat generation per unit volume. Solution of (2.11) gives the temperature distribution within a volume as a function of space and time[46]. For the purpose of this report, 1-D analysis will be used and it will be assumed that κ and C_P are constant over the temperature ranges of interest. Thus, (2.11) simplifies to

$$\rho LwtC_p\frac{\partial T}{\partial t} + \frac{\kappa wt}{L}\Delta T + \frac{2\kappa_{air}L(w+t)}{L_{air}}\Delta T = P \tag{2.12}$$

for the beam in Figure 2.6. The energy storage and dissipative qualities of the beam are lumped into the equivalent circuit parameters: beam element thermal resistance, $R_{b,x}$, beam element thermal resistance to surrounding air, $R_{a,x}$, and beam element thermal capacitance, $C_{b,x}$, given by

$$R_{b,x} = \frac{L}{N\kappa wt} \tag{2.13}$$

$$R_{a,x} = \frac{L_{air}}{2N\kappa_{air}L(w+t)} \tag{2.14}$$

$$C_{b,x} = \frac{\rho LwtC_p}{N}. \tag{2.15}$$

The number of elements, N, sets the accuracy of the lumped simulation.

FIGURE 2.6 *(a) Schematic of beam element for lumped thermal analysis. (b) Equivalent RC thermal circuit element representation for dynamic thermal simulation. $R_{a,x}$ is the equivalent thermal resistance to the air for a characteristic conduction length. Based on finite element analysis, a reasonable assumption for the characteristic length for conduction through air is 10 μm. $R_{b,x}$ is the thermal resistance of the element and $C_{b,x}$ is the thermal capacitance.*

(a)

(b)
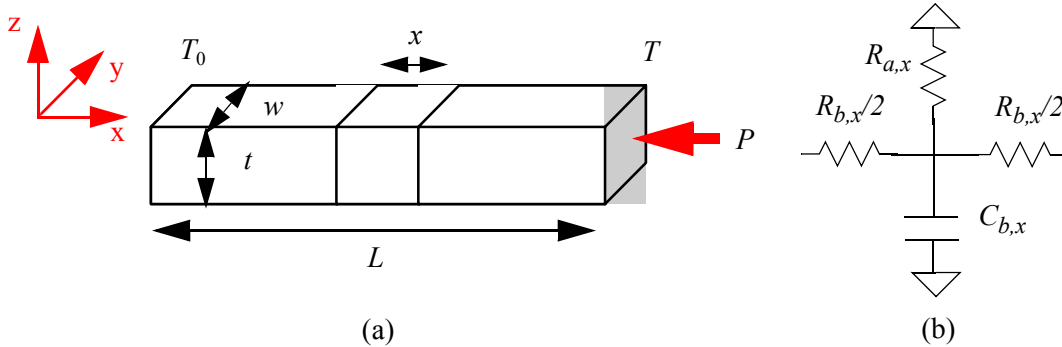
2.3.3 Heat Generation

Heat must be generated in or conducted to the electrothermal actuators to give rise to the bending moments that actuate the mirrors. Joule heating is employed in electrothermal MEMS actuators. The rate at which heat is dissipated in a resistor of resistance, R, due to an applied voltage, V, or current, I, is given by $P = I^2 R = \dfrac{V^2}{R}$. Two types of heater can be used: low resistivity polysilicon film embedded along the entire length of the actuator for distributed heat generation and high resistivity polysilicon resistors placed at discrete locations along the length of the actuators. Embedded polysilicon along the entire length of the beam was not used for this design because of the fill factor requirement. If such an embedded polysilicon heater were used, a 540 μm m1-poly beam would be required to achieve the 45° deflection angle, based on the data from Table 2.1.

Two discrete resistors were used as heaters in each beam as shown in Figure 2.7. Resistors were placed at the end of the beam and at a position in the middle of the beam. The end-beam resistor was 1540 Ω, the mid-beam resistor was 350 Ω. The beam lengths were L_a = 140 μm and L_b = 290 μm.

FIGURE 2.7 *Electrical and thermal beam schematic showing discrete resistors location within each actuator.*
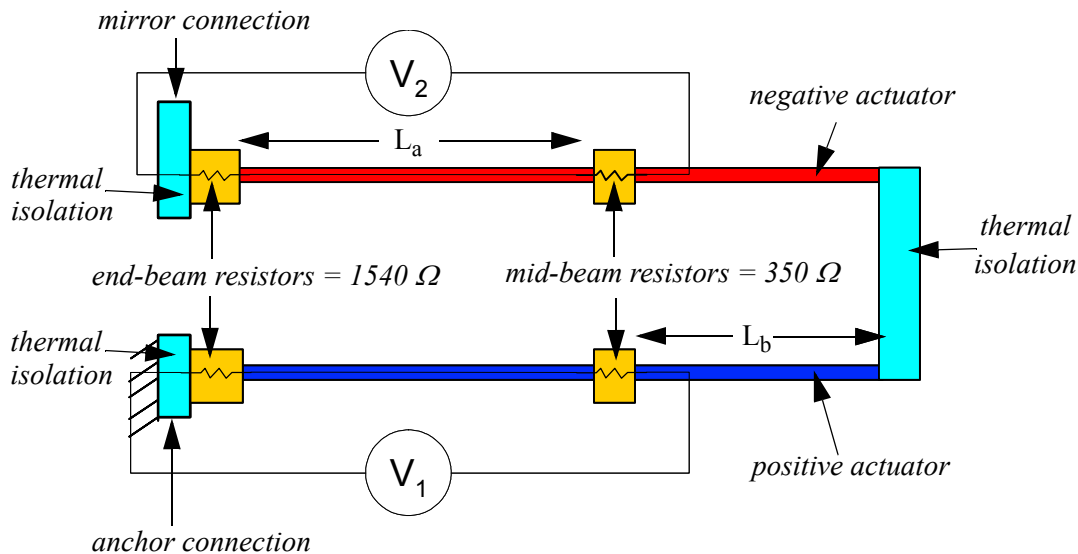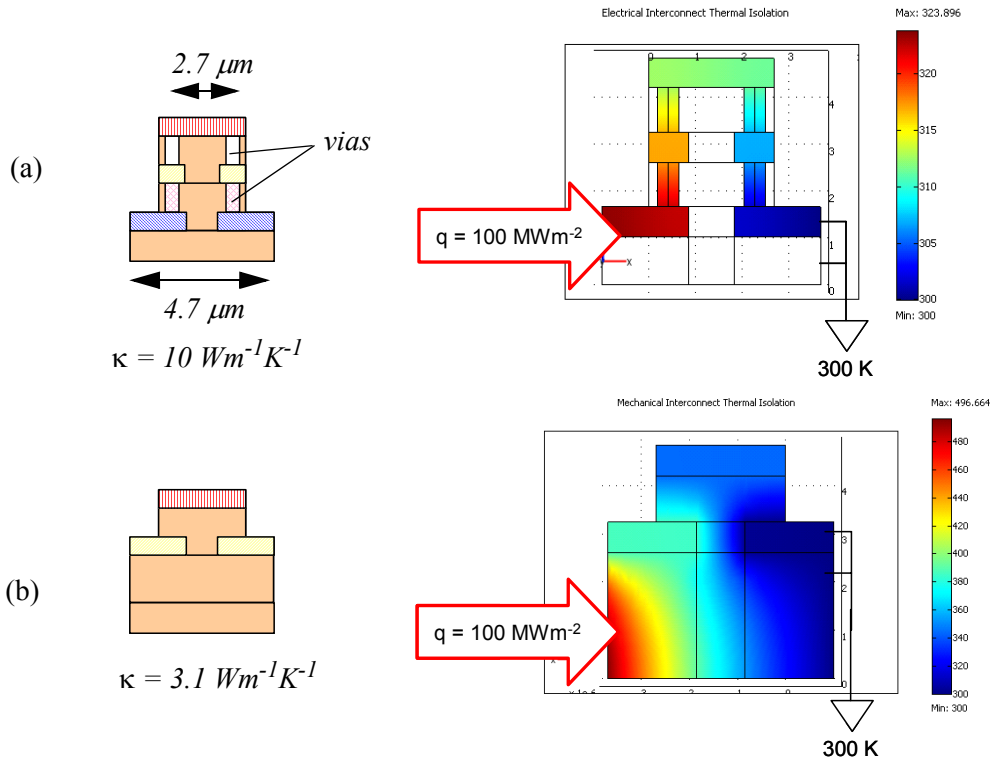
FIGURE 2.8 *Femlab simulation to determine lumped parameter estimates for the thermal conductivity of various configurations of thermal isolation for later simulation. (a) electrical interconnect with SiO$_2$ suppressed to show vias. (b) m2 slotted mechanical interconnect.*


2.3.4 Thermal Isolation and Simulated Response

Overall power consumption is reduced by minimizing the conduction of thermal power to the anchors, substrate, mirror and surrounding air. For the actuator topology in this report, the overall angular motion is optimized by minimizing the thermal cross-talk between actuators. This design consideration suggests the thermal isolation of the actuators should be maximized and the surface to volume ratio of the actuator minimized. There is a trade-off here as the thermal time constant is increased by increasing the thermal resistance to ground and increasing the heat capacity of the actuator.

Figure 2.8 shows the results of a Comsol Multiphysics 3.2 (Femlab) finite element analysis to determine lumped parameter estimates for thermal conductivity of isolation elements. The 3-D heat conduction application mode was used to accurately model the effect of circular tungsten vias in elec-

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trical interconnects. Thermal conductivity was approximated by passing a known heat flux into a known area and calculating the temperature difference to ground arising from the heat flow. The lumped parameter conductivity values derived from simulation were used to generate thermal schematics for simulation using Spectre. The beams were modeled as series connections of the circuit element shown in Figure 2.6. Figure 2.9 shows the simulated DC and AC response of the positive actuator to an input thermal power. The simulation results indicate cross-talk is not an issue limiting performance, but losses to the anchor and mirror do impact performance.

FIGURE 2.9 *(a) DC thermal response of the positive actuator. The tip of the actuator does not increase in temperature, indicating the resistor placement and sizes are not optimized, but leads to the conclusion that thermal cross-talk is not the limiter of mirror angular deflection. (b) AC thermal response of the positive actuator.*
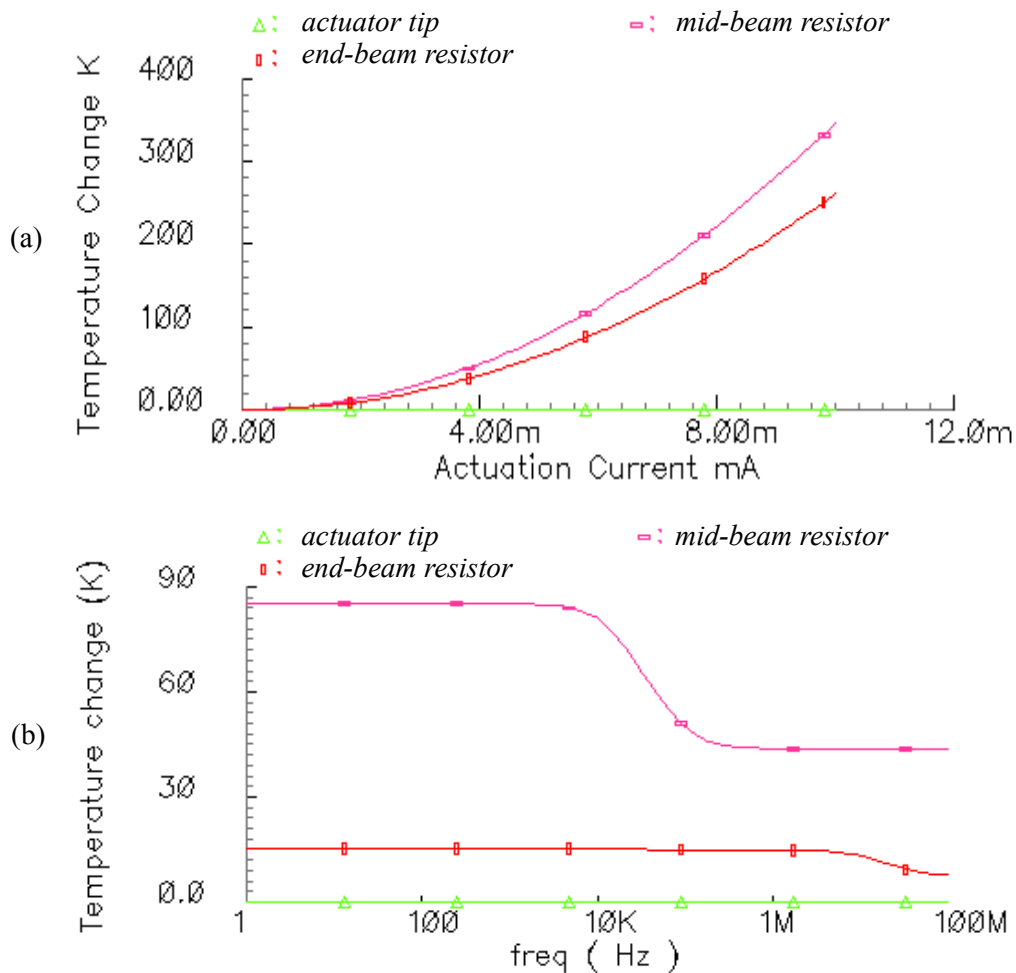
2.4 Modes

To first order, an undamped mass, *m*, in 1-D motion on a spring with spring constant, *k*, will have a single resonant frequency given by $\omega = \sqrt{k/m}$. Thus, it can be seen that when *m* is large and *k* is small the resonant frequency will be low. As the motion of the mass becomes more complex and coupled with the motion of the spring, higher modes, degenerate modes and non-linearities must be considered, but analytical derivation of expressions defining the mode frequencies becomes intractable.

Designing the position of the first mode was beyond the scope of this stage of the project but finite element analysis was performed using Femlab to identify the mode shapes and their frequencies for comparison with the fabricated device. A mechanical model of the mirror was constructed in Femlab using the solid, stress-strain application mode of the Structural Mechanics module. The full mirror, each actuator comprised of three individual beams and strut connecting the negative actuator to the mirror were included in the solid model for display purposes, even though symmetry could have been exploited to reduce the mode size and speed up simulation. As such, the simulation time for the first fifteen modes was less than 2 min. The eigenfrequency solver was used to simulate the mode shapes.

Figure 2.10 shows the first mode at 51 Hz and the third mode at 261 Hz. The first and second modes are both "pitching" modes, in that the mirror rotates about the centroidal axis in the desired sense. The difference between these modes lies in the motion of the actuator beams; in the first mode only one actuator beam is in motion, while in the second mode both actuator beams are in motion. The third mode is a "rolling" mode in which the mirror rotates about an in-plane axis perpendicular to the centroidal axis of designed rotation. The third mode is an undesirable mode. Its proximity to the second pitch mode indicates further redesign of the actuator beams is necessary.

FIGURE 2.10 *Femlab simulation geometry comprised the mirror with a 6 μm CMOS stack on a 50 μm silicon plate connected on opposite sides at the level of the CMOS to a pair of series connected sets of beams. (a) Mode 1 (pitch 1) - 51 Hz. (b) Mode 3 (roll) - 263 Hz. Mode 2 (pitch 2) at 192 Hz is not shown as its form is similar to mode 1 with different beam coupling.*

(a) *Mode 1 - 51 Hz*

(b) *Mode 3 - 263 Hz*
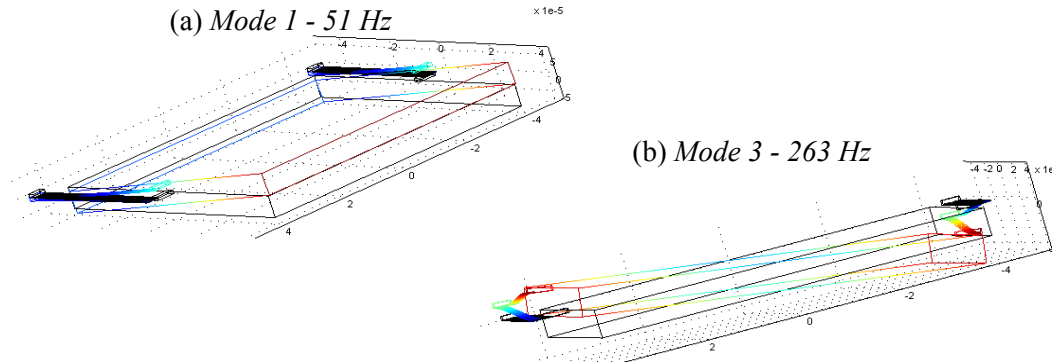
2.5 Geometric Considerations for Large Mirrors and Motions

Foundry CMOS uses as a substrate highly polished (single-sided) silicon wafers that are much thicker than the circuitry formed on their surface[49]. Thick wafers are more mechanically robust and hence more likely to survive the manufacturing process, which can consist of several hundreds of manual and robotic handling operations. The back-side of the silicon substrate also acts to getter contaminants, such as heavy metals, that could adversely affect the high performance electronics formed on the front-side of the wafer. After the CMOS processing is completed, the wafers are ground down to a predefined thickness, in a process called lapping, prior to cutting the wafer into individual chips for packaging. For example, a standard 8" silicon wafer has a thickness of ~700 μm but can be lapped to as thin as 250 μm. The current JAZZ process yields an ~280 μm chip thickness. For most MEMS devices, the mechanical structures have in-plane motion, small out-of plane motions on the order of 10's of μms or large out-of-plane motions above the plane of the surface so chip thickness is not an issue. However, with large, centroidally rotating mirrors and large motions, chip thickness is a constraint that must be addressed as the frame (chip) thickness may not accommodate the range of motion of the mirror, as shown in Figure 2.11. A post-CMOS compatible, intermediate packaging technique will be introduced

in Section 3.3 that decouples the out-of-plane rotational motion of the mirror from the thickness of the

CMOS chip. The minimum separation between the backside of the plate and the package base is

$$z_{edge} = \frac{L_m}{2}\sin\theta_{max} + t_p\cos\theta_{max}. \tag{2.16}$$

FIGURE 2.11 *(a) Plan view of mirror with anchor and frame. (b) Cross-section view showing mirror edge z displacement at full scale deflection angle.*
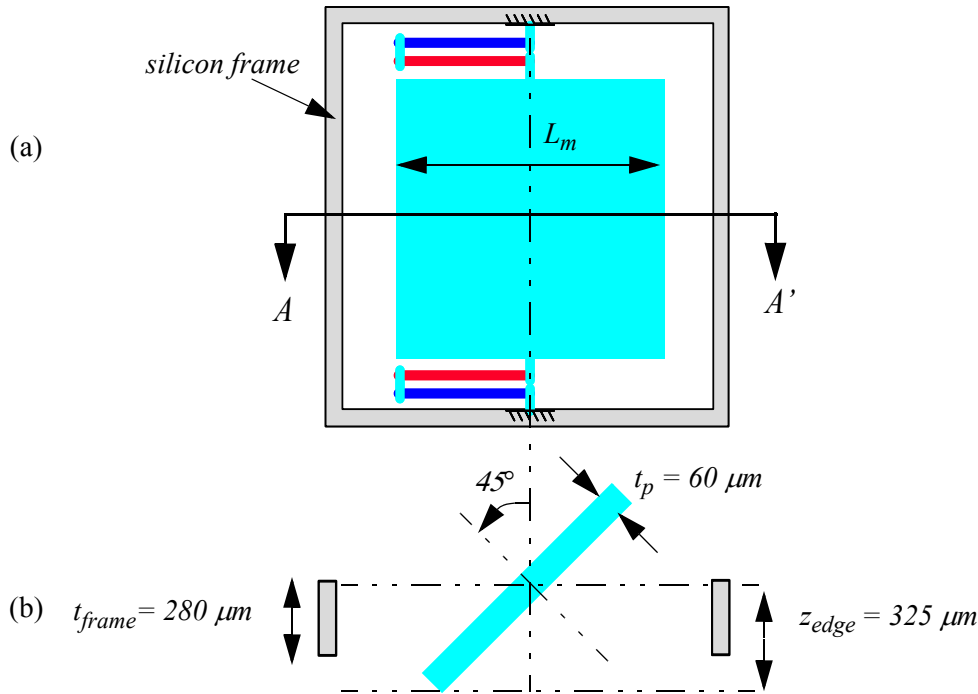

2.6 Mirror Backside Plate

The masks for fabricating the mirror backside plate were generated using a Heidelberg DWL 66 direct write laser lithography system and were designed to optimize the uniformity of plate thickness. Silicon plate thickness is the biggest driver of final mirror mass, and hence the resonant frequency of the first mode and its uniformity is critical to the avoidance of undesired rotational modes. Aspect ratio dependent etching (ARDE) and microloading was utilized to control the plate uniformity and modulate the silicon thickness under the actuators and the profile of the sidewalls. A grating pattern and mask geometry was developed in [51] and used to generate the mask shown in Figure 2.12. Trench width

under the actuators was increased to reduce the thickness of the silicon and thereby the frontside aniso-

tropic etch time in that region.

FIGURE 2.12 *Backside mask utilizing sections of variable width to control the uniformity of the etch process by aspect ratio dependent etching.*
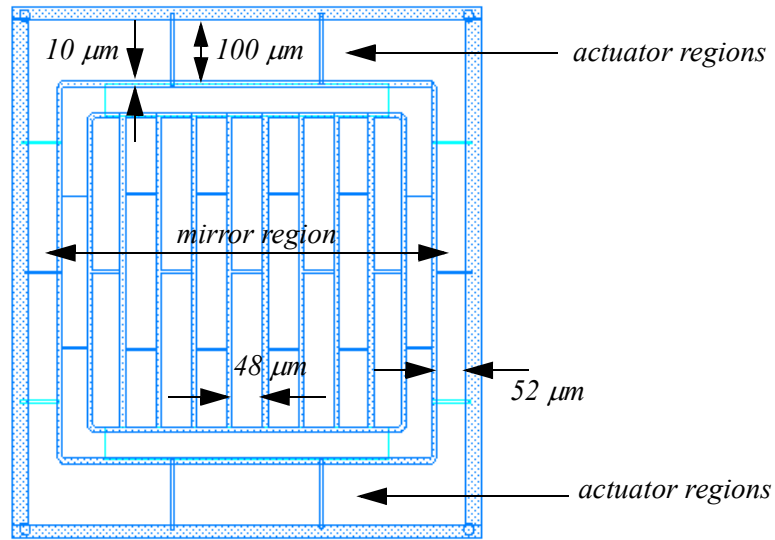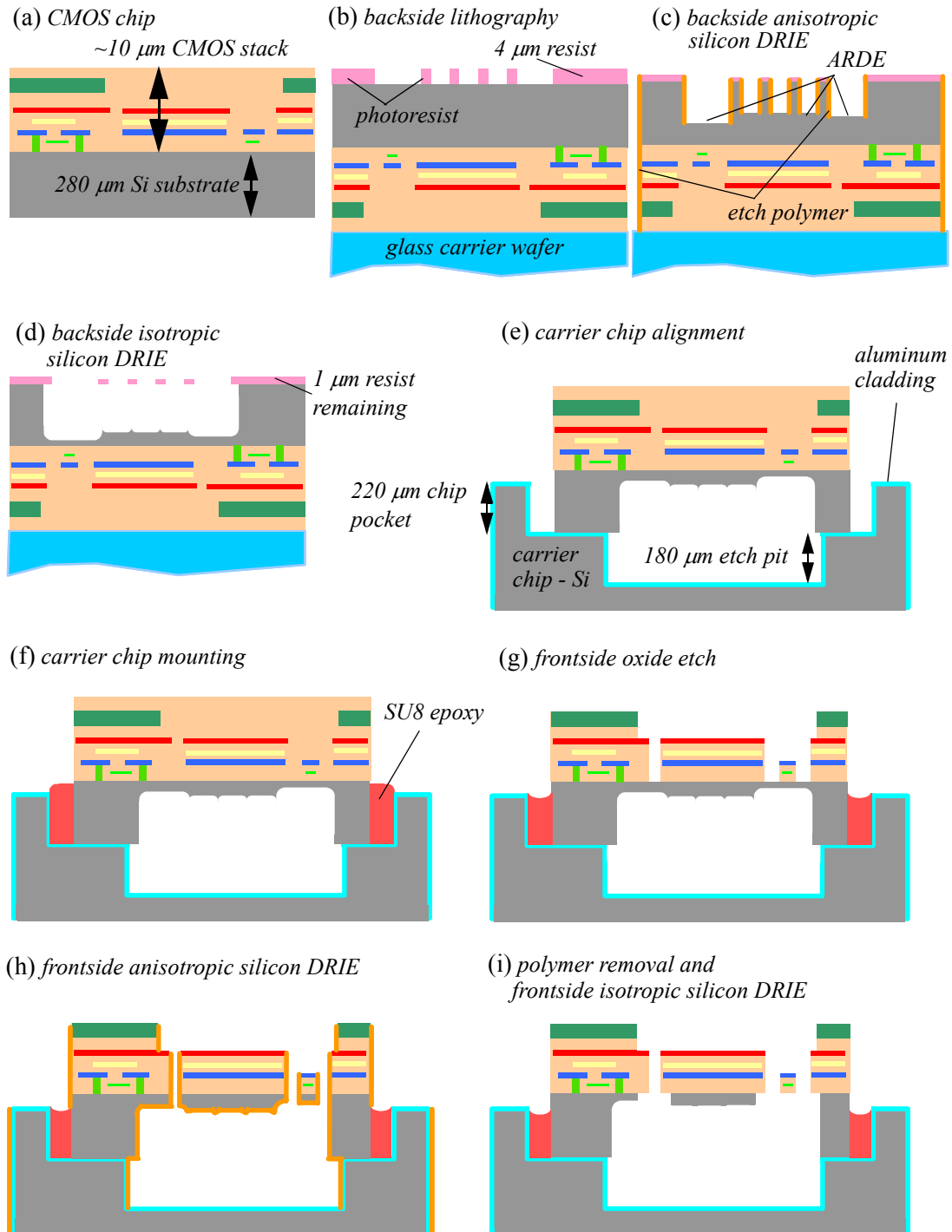
3

Device Fabrication

3.1 Post-CMOS Processing

The formation of MEMS devices from CMOS polysilicon layers and oxide layers was first proposed by Parameswaran[34], et al. in 1989. The invention of the so-called "Bosch process", a time multiplexed deep reactive ion etch of silicon (DRIE-Si), in 1996[52] introduced a new post-CMOS process that enabled independent control of vertical and horizontal etch dimensions in silicon through the use of alternating etch and passivation steps. Work by Xie[53] utilized the Bosch process to etch large amounts of silicon from the backside of a CMOS chip to tailor the silicon thickness under MEMS devices, which were later released using a front-side silicon etch. Today, the term "post-CMOS processing" is used to describe any combination of processing steps up to, and including, the structural release process.

In this chapter, post-CMOS processing of the 5 x 5 array of micromirrors will be discussed in detail. Figure 3.1 shows, in summary, the process flow comprising backside resist masked silicon etch, mounting in a process compatible carrier chip to enable the released mirror to achieve full scale deflection angles, the selective removal of the dielectric layers using the metal interconnect as an etch mask, anisotropic silicon etch and finally, isotropic silicon release etch (see Appendix A for the detailed process flow). A low cost, technology specific, etch depth process control was developed to improve etch depth control during backside silicon etch and will be presented in Section 3.2.3. Packaging and wire-bonding were performed prior to device characterization, but will not be discussed in detail here.

FIGURE 3.1 *Graphic summary of post-CMOS process flow used to fabricate the electrothermally actuated micromirrors. The images are schematic cross-sections through a chip. The images are not to scale in either the y or z directions. The CMOS color coding of Figure 2.2 has been used for consistency.*

(a) *CMOS chip*

~10 μm CMOS stack

280 μm Si substrate

(b) *backside lithography*

4 μm resist

photoresist

glass carrier wafer

(c) *backside anisotropic silicon DRIE*

ARDE

etch polymer

(d) *backside isotropic silicon DRIE*

1 μm resist remaining

(e) *carrier chip alignment*

aluminum cladding

220 μm chip pocket

carrier chip - Si

180 μm etch pit

(f) *carrier chip mounting*

SU8 epoxy

(g) *frontside oxide etch*

(h) *frontside anisotropic silicon DRIE*

(i) *polymer removal and frontside isotropic silicon DRIE*

3.2 Backside Processing

3.2.1 Backside Lithography

Backside DRIE allows the MEMS designer to take advantage of the optical flatness of the silicon wafers used for foundry CMOS. It gives the designer the ability to tune the thickness of the silicon under their devices, either for high Q springs with very low z axis compliance or to meet specific proof mass requirements. To realize the benefit of this approach, it is necessary to reproduce the desired silicon thickness reliably from device to device. Frederick[51] showed that backside etch profile control and depth uniformity could significantly be improved by spatially modulating the surface area exposed to etching over the total region to be etched. The backside pattern with open area modulation used for this device is shown in Figure 2.12.

In this application, the minimum backside etch pit proximity to the edge of the CMOS was 100 μm, which imposed a difficult resist uniformity condition. To provide a uniform resist layer to within 100 μm of the chip edge, the planar surface over which the resist front moves during spinning was extended by the use of tiles (see Figure 3.2). Tiling and other variants that move the edge discontinuity away from the device are commonly used in such situations. There was a slight height mismatch of the tiles and the CMOS, measured using a micrometer at +/- 5 μm. Edge bead was still visible with tiling due to this mismatch and from resist piling in the gaps. The edge bead was measured at ~200 μm from the chip edge using an Olympus microscope with integrated CD (critical dimension) software. The chip edge with minimum MEMS device proximity was placed at the center of the array adjacent to other CMOS chips. It can be seen in Figure 3.2 that there is no noticeable edge bead where the CMOS chips contact each other.

3.2.2 Backside DRIE

The silicon was etched on a Surface Technology Systems (STS) ASE (advanced silicon etch) multiplex inductively coupled plasma (ICP) tool using a Bosch silicon etch process[54]. The etch process

conditions are given in Appendix A. The process consisted of an endpointed anisotropic etch to reach a

target depth of approximately 220 µm, a polymer removal step to expose the silicon of the walls sepa-

rating adjacent cells, and an isotropic etch to remove the walls of the cells and smooth the bottom of

the etch pit.

FIGURE 3.2 *CMOS chips tiled to reduce edge beading. (a) Resist coated chips with a significant edge bead still visible in the corners but no edge bead over contacting CMOS edges. (b) Post etch view of tiled CMOS with endpoint coupon.*


(a) (b)
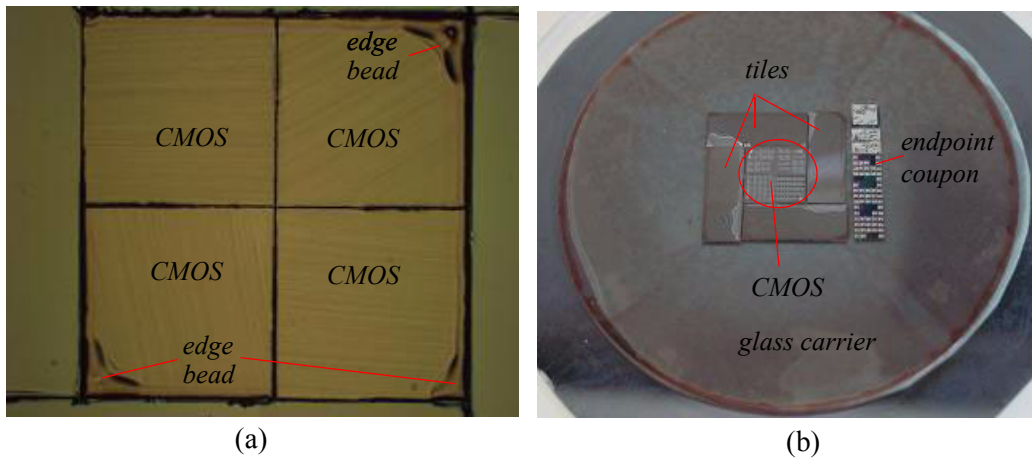
3.2.3 Plate Thickness Control

The target thickness for the silicon plate under the mirror was 50 to 70 µm requiring a

210 to 230 µm etch of silicon given a chip thickness of 278 +/- 6 µm. In industry, to achieve this level

of thickness (or depth) targeting over this etch depth, a laser interferometric system with fringe count-

ing would be employed. In the absence of such a system it is typical to etch the chip for a conservative

predefined time, measure the depth etched in this time to calculate an etch rate and then complete the

etch with a calculated fixed time. Deviations from etch depth are addressed by additional etch time

until the target is reached or if the target is exceeded the device may be scrapped, or downgraded.

To avoid such time consuming iterations, a novel etch-to-depth endpoint technique was developed

based on ARDE that enabled single step etching to within +/- 5 µm of the depth target. Xu[54] mea-

sured the variation in etch rate with trench width and found a logarithmic dependence of etch rate on

FIGURE 3.3 *The graph shows the visual endpoint time as a function of trench width for a single endpoint coupon. The time error in calling visual endpoint, i.e. the time when the aluminum on the bottom of the endpoint coupon became visible was judged to be +/- 30 s. The user should note this relationship is characteristic of the etch process at the time the experiment was run and it is likely the process performance will change over time due to equipment conditions.*

$$y = -4.6139 \ln(x) + 144.38$$

Breakthrough Time (min) vs Trench width (um)
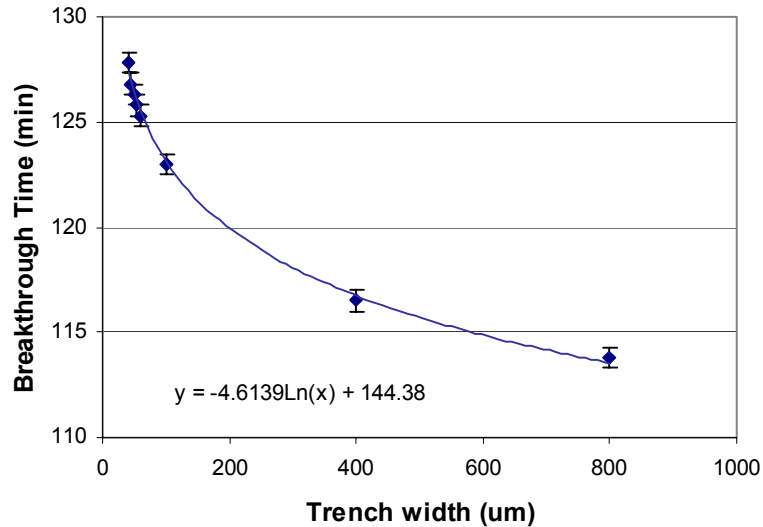
aspect ratio (up to 55 μm etch depth). Figure 3.3 shows an extension of this analysis to through wafer etching and charts the variation in time to etch a 220 μm depth as a function of trench width. The endpoint concept was to use a chip, called the endpoint coupon, of thickness equal to the desired etch depth (minus the amount of silicon removed during the isotropic etch, ~20 μm), patterned with an array of gratings of various width and metallized on the unpatterned side to increase reflectivity. The endpoint coupon was mounted on the glass carrier wafer next to the CMOS chips and etched along with them (see Figure 3.2). The trench width step size between grating array elements was chosen to provide a resolution of 5 μm in etch depth around the target depth (see Figure 3.4). ARDE led to the cells with trench widths greater than the backside CMOS pattern etching through to the reflective layer of the endpoint coupon prior to the CMOS reaching their desired depth target. By observing the staggered breakthrough of the endpoint coupon cells, the point at which the CMOS reached their depth target was identified.

The on-chip silicon depths following backside DRIE are shown in Figure 3.5. Etch depth targets were achieved to within 10 μm. The total etch depth is greater than the goal (30 μm plate thickness cf. 50 μm goal) because the wafer used to fabricate the endpoint coupon was 20 μm thicker than required, however the uniformity and range of the output using the endpoint coupon demonstrates the validity of the technique.

FIGURE 3.4 *(a) Endpoint coupon prior to backside DRIE showing cells of varying trench width. A cluster of cells were spaced at 5 μm intervals around 50 μm. (b) Series of images of endpoint coupon taken during etch showing the staggered breakthrough of silicon to the underlying aluminum layer according to trench width. (c) Image of endpoint coupon following etch.*
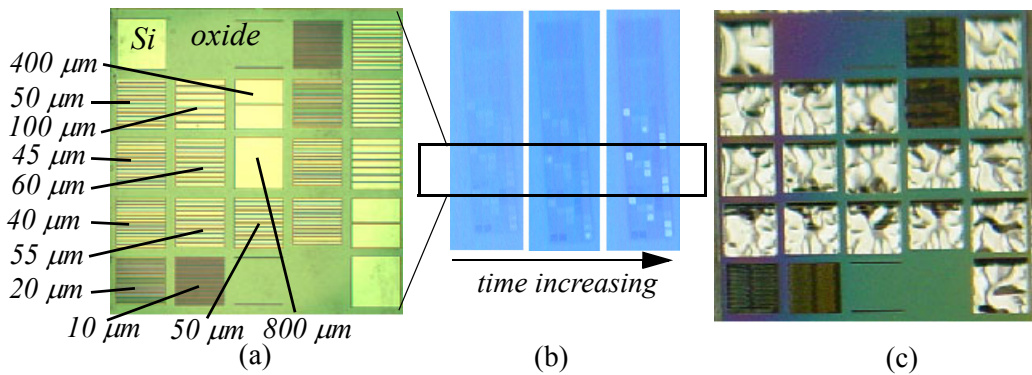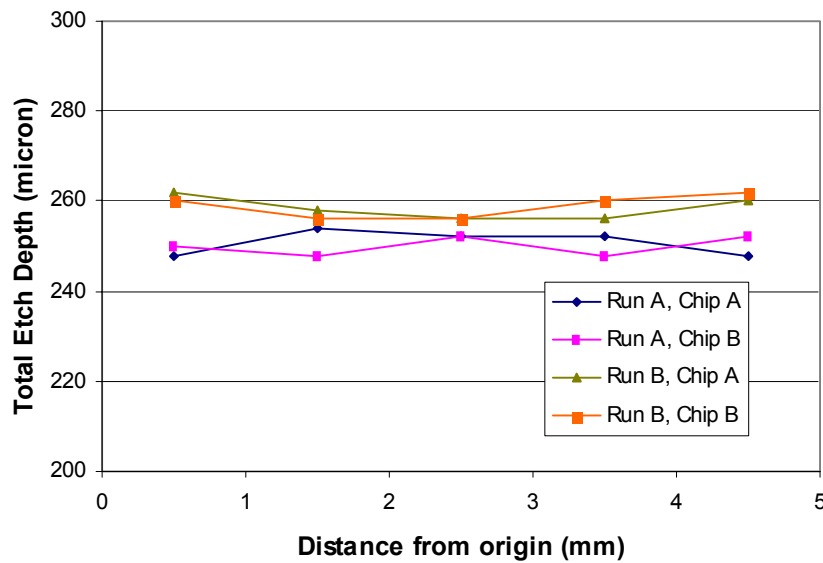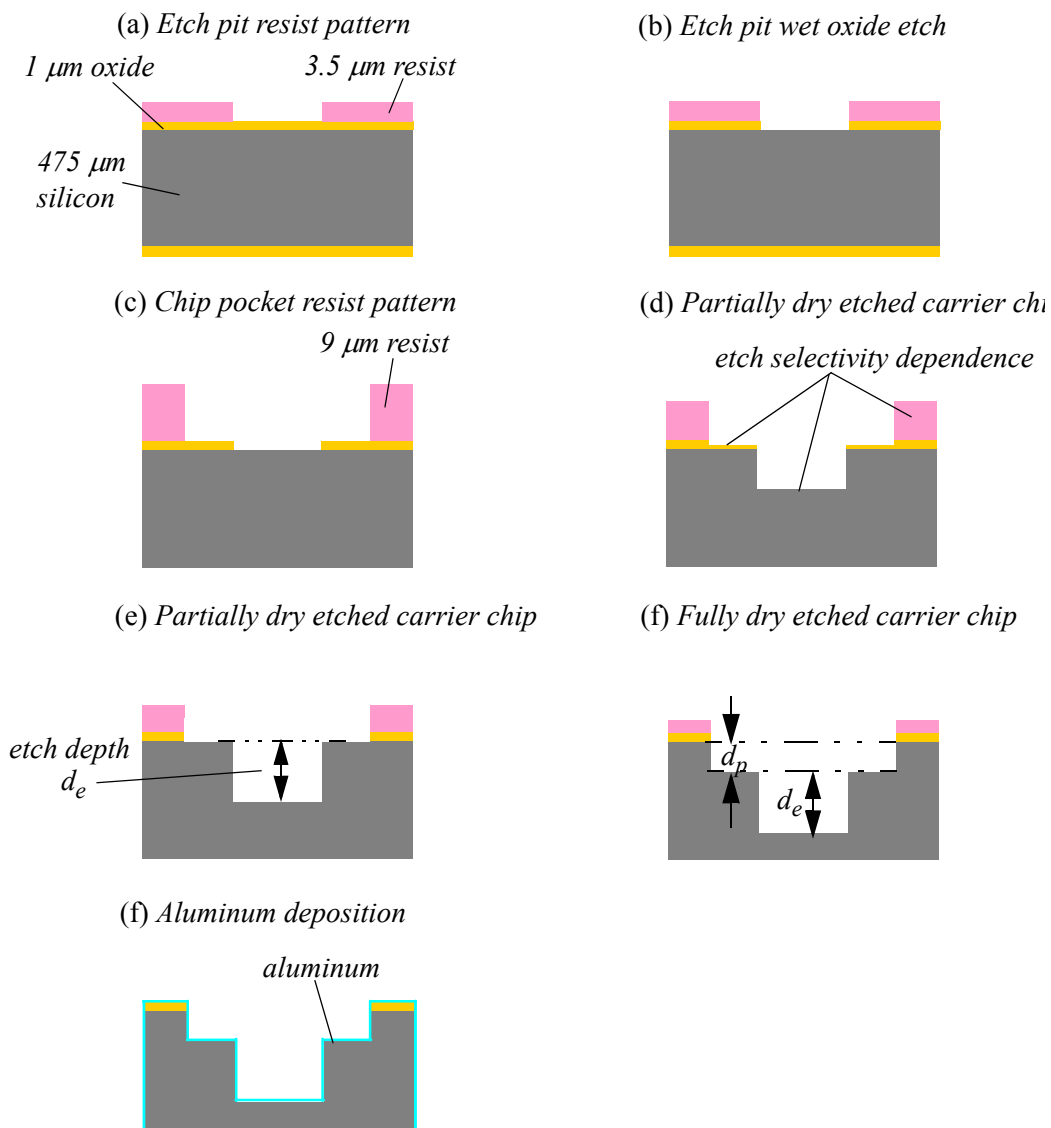

FIGURE 3.5 *Etch depth from two separate runs, two chips per run, etched with endpoint coupon.*

3.3 Carrier Chip

It was demonstrated in Section 2.5 that the CMOS chip thickness was not sufficient to allow an 800 μm x 800 μm mirror to rotate through 45°. In addition, early devices were too fragile to remove them from their carrier wafers following structural release. To address this issue, a carrier chip was fabricated using the flow shown in schematic in Figure 3.6. In order to use the carrier chip as a perma-

FIGURE 3.6 *Schematic process flow for carrier chip. Note all films etch at a finite rate. The selectivity of the etch to the various films determines the relative amount of each material etched in a given time. Resist coat and strip steps are not shown.*

(a) *Etch pit resist pattern*

1 μm oxide   *3.5 μm resist*

475 μm silicon

(b) *Etch pit wet oxide etch*

(c) *Chip pocket resist pattern*

9 μm resist

(d) *Partially dry etched carrier chip*

etch selectivity dependence

(e) *Partially dry etched carrier chip*

etch depth d_e

(f) *Fully dry etched carrier chip*

d_p

d_e

(f) *Aluminum deposition*

aluminum

nent part of the finished device, the chip and the materials used to mount the CMOS in the carrier chip had to be post-CMOS process compatible. The chip was manufactured from a 475 µm thick, oxide coated, silicon wafer. SU8 epoxy was selected as the adhesive because of its ready availability and well characterized material properties and etch behavior. The design of the carrier chip consisted of: 1) a 180 µm etch pit into which the mirror would rotate, 2) a variable width step on which the CMOS would sit and be supported during packaging and wirebonding, 3) a 220 µm pocket into which all the CMOS chips would fit with a maximum of 100 µm clearance between the edge of the chip and the inner edge of the pocket, 4) reservoirs for the application of the SU8, and 5) positioning marks at each inner corner of the pocket. The pocket dimensions were determined by a statistical analysis of CMOS chip size. The process flow for the carrier chip is given in Appendix A.

3.3.1 Damascene Etching

A variant of the dual damascene concept, in which two separate, nested etch holes are formed in a two stage masked etch was applied to form the etch pit, chip pocket and step. This concept was used because a spray on resist process was unavailable and a conformal spin-on resist coat over a 400 µm step is impossible. As shown in Figure 3.7, the pocket and reservoir pattern lay outside the etch pit, thus during the silicon etch process, the silicon in the etch pit region and the oxide in the pocket and the reservoir region were exposed to the etch plasma from the beginning of the process. The carrier chip was etched on the STS ASE etcher using the anisotropic DRIE etch conditions given in Appendix A. At some point during the etch, dependent on the selectivity of the etch process to oxide, all the oxide in the pocket and reservoir region was etched away, and at this point the silicon began to etch. The etch process was continued until the desired step height was obtained. The resist used to form the pocket and reservoir pattern was thick enough to survive the etch process without complete erosion. For a desired etch pit depth, d_e, and measured etch rates for oxide and silicon of ER_{ox} and ER_{si}, the oxide thickness required is

$$t_{ox} = \frac{ER_{ox}}{ER_{Si}} \cdot d_e.$$ (3.1)

The measured etch rates were $ER_{ox} = 12$ nm/min, $ER_{Si} = 2.18$ µm/min and $ER_{res} = 33$ nm/min. For this mirror design, (2.16) gives a minimum etch pit depth of 43 µm to allow full scale angular deflection, but this was increased to 180 µm to provide additional margin.The pocket depth was designed to be 220 µm so the center of gravity of the CMOS chip would lie below the edge of the pocket and still provide a significant area of silicon for the positioning probes to contact the chip. The oxide thickness needed for this etch pit depth was 1 µm using (3.1).

FIGURE 3.7 *The carrier chip. (a) Prior to silicon DRIE. (b) Following Al deposition. (c) Following mounting of CMOS.*


(a) (b) (c)
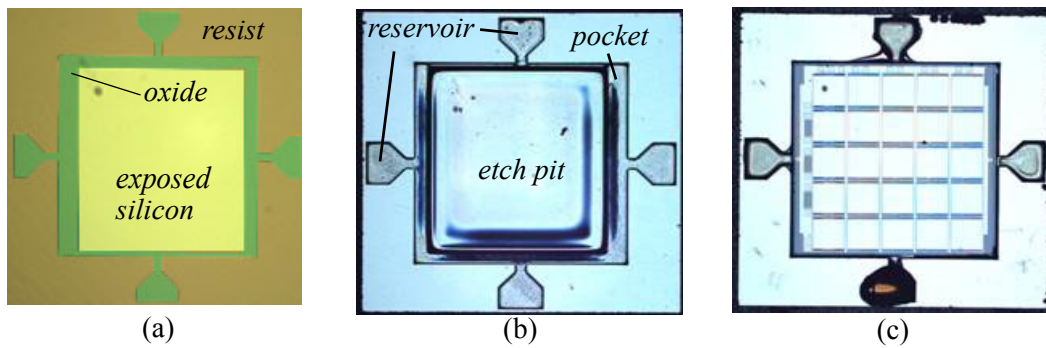
3.3.2 Mounting

Bedair, et al.[55] demonstrated the use of capillary action for loading a resonant cantilever beam chemical sensor with absorptive polymer applied to a large spatially separated reservoir. This concept was employed to form a continuous fill of SU8 in the gap between the CMOS edge and the pocket in the carrier chip. In the design of the carrier chip, a conical reservoir was placed centrally on each side of the chip to which the SU8 was applied. The neck of the reservoir was designed to be 200 µm, to ensure a positive capillary pressure would exist to draw the SU8 out of reservoir and around the CMOS. The carrier chip was coated with Al to improve SU8 wetting and enhance the capillary effect. In the best case, application of SU8 to a single reservoir was needed to completely fill the gap around

the entire chip, but generally, more than one reservoir had to be used due to chipping and etch induced

non-uniformity of the sidewall of the chip. The fill integrity of the SU8 following post-CMOS process-

ing is shown in Figure 3.8.

FIGURE 3.8 *SU8 fill of the gap between the inner edge of the carrier chip pocket and the side of the CMOS chip. The images shown were taken following completion of post-CMOS processing, leading to the recessing of the SU8 in the gap. a) Low magnification image showing the corner of a CMOS chips sitting in the pocket of the carrier chip, with SU8 filling the reservoir and the gap.*
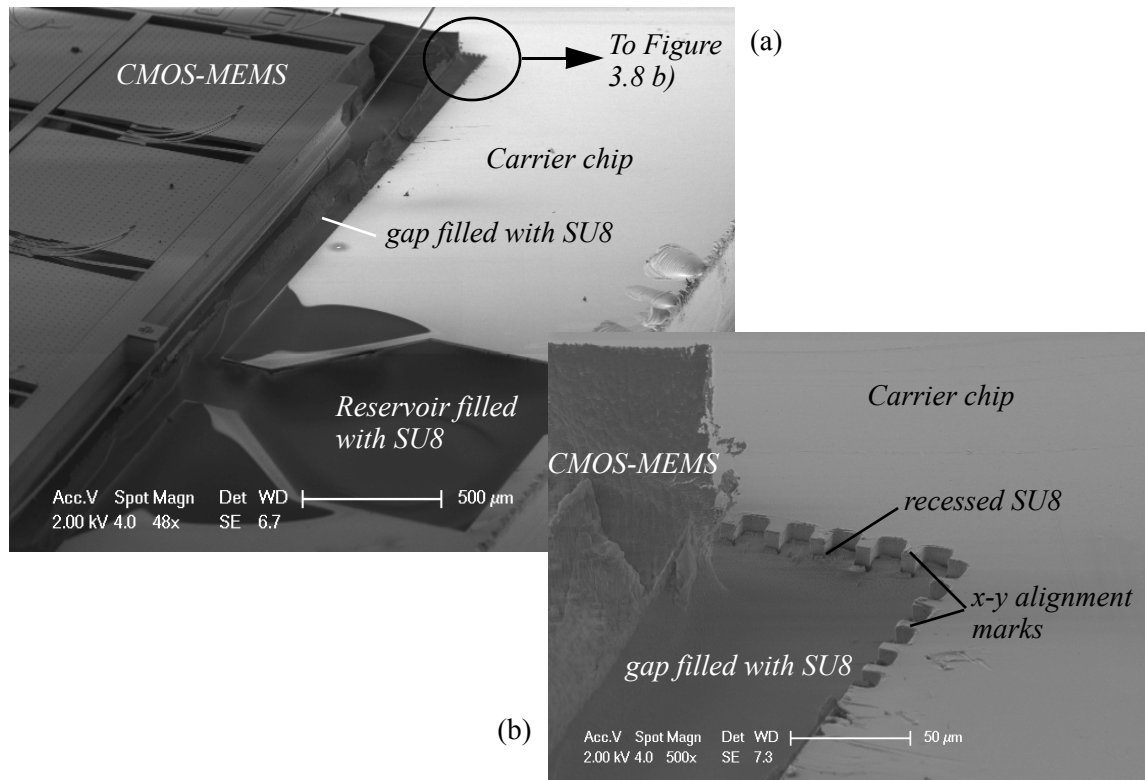
3.4 Frontside Release

3.4.1 Oxide Etch

The goal of the frontside oxide etch was to remove the passivation layers, the interlayer dielectric

and any surface oxides from the silicon to expose it for frontside DRIE and release. The process condi-

tions are given in Appendix A.

3.4.2 Silicon Etch

The frontside silicon release etch conditions are given in Appendix A. A video camera mounted to the top of the process chamber enabled real-time monitoring of the process. Due to the size of the mirrors, their release from the substrate was observable on video. The mirrors did not release en masse or even in a structured pattern, indicating either unobserved artifacts or defects from previous process steps or handling, or non-uniformity of process across the chip.

3.5 Artifacts

3.5.1 Actuation While Etching

During silicon release etch, it was observed that released mirrors actuated as the process switched between etch and passivation steps. This was repeatable for multiple transitions from etching conditions to passivation steps. The actuation of the mirrors during etch indicated the actuators' temperature was increasing significantly, on the order of 50° C to 100° C.

3.5.2 Barrier Metal Attack

As noted in Section 3.4.2, mirrors across the array released at different times, so following processing there were examples of mirrors that were overetched by several minutes, to the point that their metal layers were delaminating, mirrors that only etched for a few additional seconds following release etch and mirrors that had not yet released. Microscope inspection of each of these cases found a dramatic difference in the attack on barrier metal on released mirrors and unreleased mirrors, indicating a local shift in process regime occurred when a mirror released. In Figure 3.9, an unreleased mirror and a mirror released for 30 s before the end of the process are shown side by side. Mirror release was observed visually using a CCD camera mounted to the top of the STS ASE ICP chamber.

Figure 3.9 (a) shows a top down optical image of a structurally released mirror and SEM images of the actuators connected directly to the mirror and the anchor, respectively. Figure 3.9 (b) shows a top

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down optical image of an unreleased mirror. The SEM images of the actuators of the released mirror show the aluminum delaminating from the underlying oxide of the actuator on the mirror side, while the aluminum is still adhering to the oxide of the actuator on the anchor side. Delamination is due to etching of the titanium-based barrier metal layer under the aluminum by the fluorinated species in the isotropic step of the release etch process. Following the anisotropic step of the release etch process, the polymeric material that protected the sidewalls of the CMOS-MEMS structures and the underlying silicon is removed to enable the fluorinated species in the plasma to attack the silicon and undercut the CMOS-MEMS structures. The author speculates that the etch rate of the barrier metal is typically suppressed by ARDE due to its nanometer scale thickness. After structural release, a dramatic shift in process regime occurs that increases the lateral barrier metal etch rate to the order of 2 μm/min, based on the observed distortion of the metal 1 layer and the width of the beam.

In the optical images, the cross stress relief crosses structures in the mirror surface can be used as an indicator of barrier metal attack and delamination. In Figure 3.9 (a) there is a circular distortion around these structures to an extent greater than the dimension of the beams in the actuator but, in the SEM image of the actuator attached to the mirror in Figure 3.9 (a), the metal 1 is not fully delaminated. These observations suggest the distortion around the stress relief structure in the mirror is a sufficiently sensitive indicator of barrier metal attack, and hence risk of aluminum delamination in the actuator, to conclude there is no delamination in the actuator attached to the unreleased mirror in Figure 3.9 (b).

In order to reliably and reproducibly fabricate large released structures it is necessary to understand the origin of the localized increase in rate of barrier metal attack and how to address it. A possible cause, that will be mentioned in greater detail in Section 5.5, is increased localized heating of the mirror, leading to a large temperature gradient along the length of the actuators, which has the greatest impact where the negative actuator connects to the mirror. A temperature increase in this region could explain the large increase in the etch rate of the titanium-based barrier metal in this area.

FIGURE 3.9 *Local variation in etch attack of the barrier metal layers. (a) Optical image of a released mirror with barrier metal attack around the cross-slots in the top metal layer with a SEM blowup of the actuator connected to the mirror and the actuator. (b) Optical image of an unreleased mirror adjacent to the released mirror within 50 μm.*


(a)

(b)

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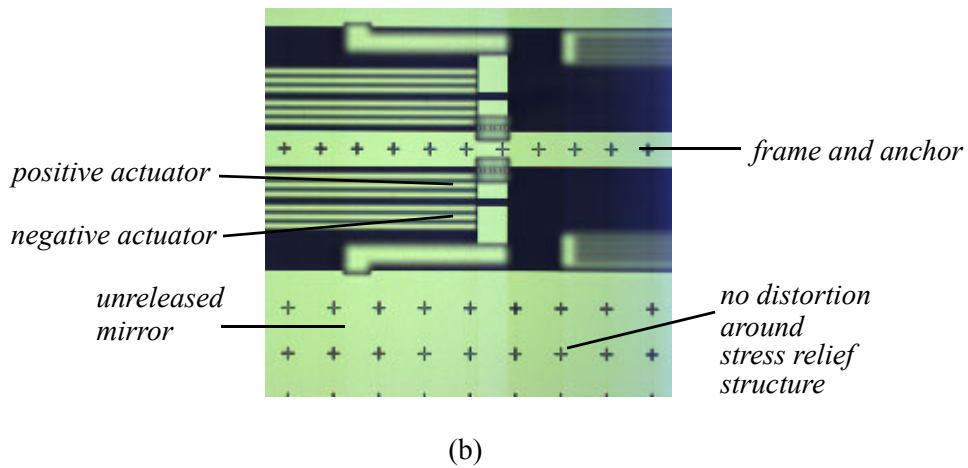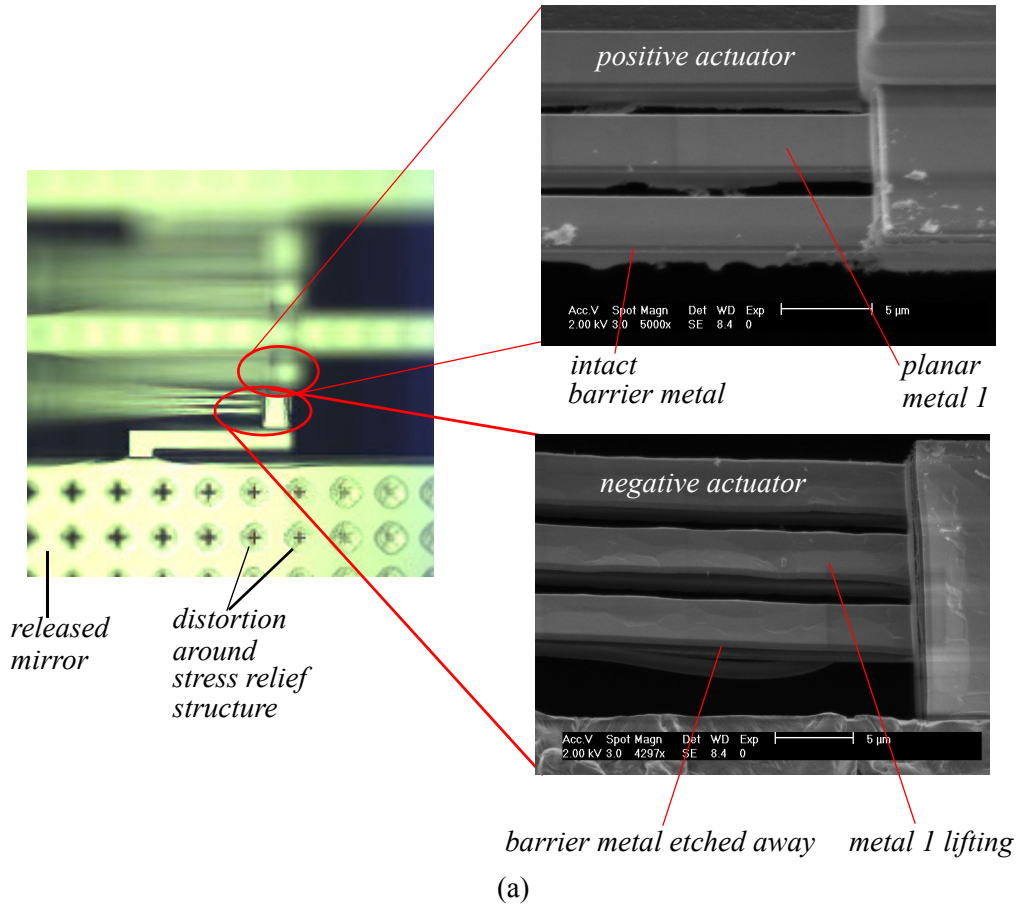
4   Device Characterization

4.1 Device Test

Process variation, barrier metal attack and lack of mechanical robustness limited the number of mirror pixels that could be tested on an individual die. The common mechanical failure mode was separation of the negative actuator beams from the strut connecting them to the mirror accompanied by delamination of the aluminum metal 1, as shown in Figure 4.1. The calculated shear force on the ends of the actuator beams for a mirror with a 60 µm silicon plate is 6.3 MPa for an arbitrary 100 G shock and 13.2 MPa if the metal 1 delaminates. Reported values for the shear strength of aluminum range from 60 - 140 MPa[56]. While not definitive, the proximity of the shear stress under shock to the shear strength of aluminum suggests a significant probability that this is the cause of the failure mode. Delamination of the metal 1 from the underlying oxide due to the barrier metal attack during the release etch process, as mentioned in Section 3.5, further reduces the shear strength of the actuator and increases the probability of failure.

For die with working pixels, the dc and frequency response of the actuators were measured. The response of the mirrors designed in this project are compared directly with electrothermally actuated mirrors designed by Xie, et al.[53], which used an embedded, low resistivity polysilicon film heater instead of discrete high resistivity polysilicon resistors.

FIGURE 4.1 *SEM showing the common mechanical failure mode of the device. The negative actuators have delaminated and sheared at their base where they connected to the strut attached to the mirror. The surface appearance of the delaminated metal 1 is identical to the actuator shown in Figure 3.9, suggesting barrier metal attack is a significant factor in this failure mode.*
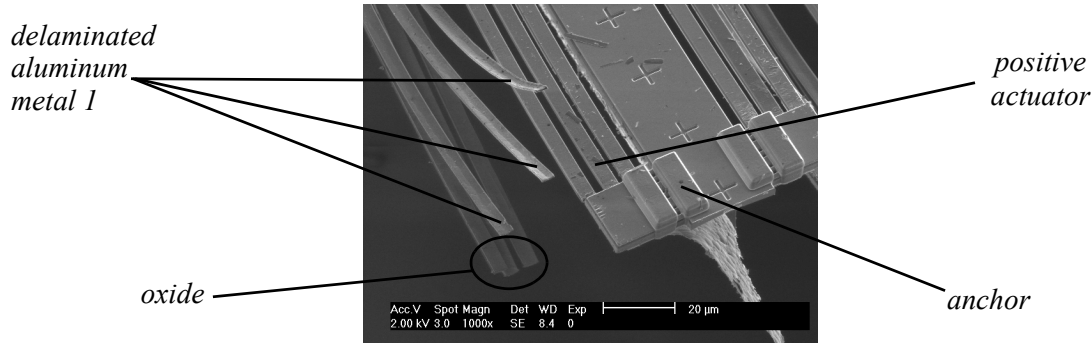
4.2 DC

DC response was tested on an optical bench using a He-Ne laser. Figure 4.2 shows static deflection angle taken by recording the position of the reflected beam on a screen of constant radius of curvature and measuring the arc length to determine the static deflection angle of the mirror. Device BET41 showed the greatest range of motion with a positive static deflection angle of 15.3° and a negative static deflection angle of 22.6°, for a total static deflection angle range of 37.9°. The largest static deflection angle of any individual mirror for a single actuation sense was 22.6° for negative actuation of BET41.

Quantum focus infrared (QIR) microscopy measurements on device BET52 at 10 V DC produced an end-beam resistor temperature and a mid-beam resistor temperature of ~54° C as shown in Figure 4.3. The beam temperature increase from the end-beam resistor to a distance of 200 μm along the beam was constant at ~31° C. With the approximation of a constant temperature change of 23° C over the remaining 230 μm of the beam, an average temperature change of the beam of 26° C was deduced. From (2.7), this temperature change corresponds to a static deflection angle of 10° which agrees within 17% of the measured deflection angle of 8.3°.

FIGURE 4.2 *Static deflection angles for a number of devices with stimulation applied to positive and negative actuators. The device identifiers contain an alphabetic label indicating they are **E**lectro**T**hermal devices and their row and column position in the array. For example, BET41 is the electrothermally actuated mirror at column 4 and row 1.*
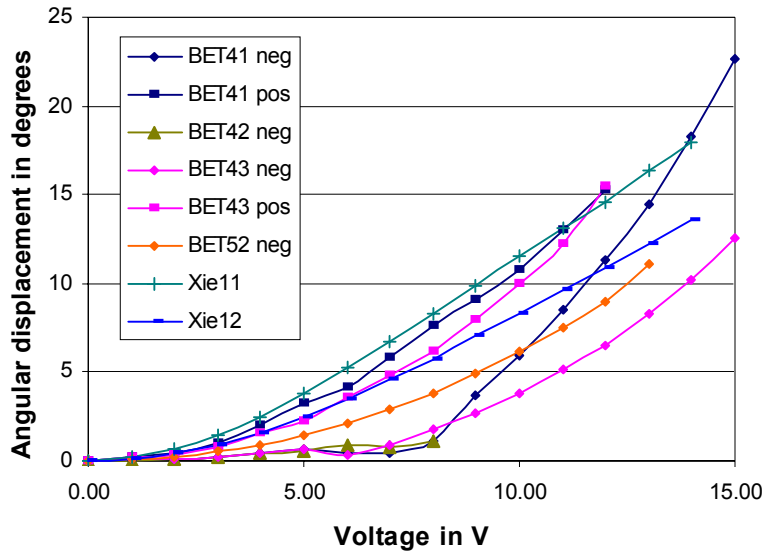
FIGURE 4.3 *(a) QIR microscopy image of BET52 during negative DC actuation at 12 V. (b) Thermal data extracted from the QIR image along a single beam in the negative actuator. The temperature of the end of the beam in contact with the end-beam resistor and the temperature of the mid-beam resistor was 54°. Note the distance scale in the graph is not given because the data was extracted from a top-down image of an upwardly curving surface, of non-uniform curvature.*

(a)   (b)
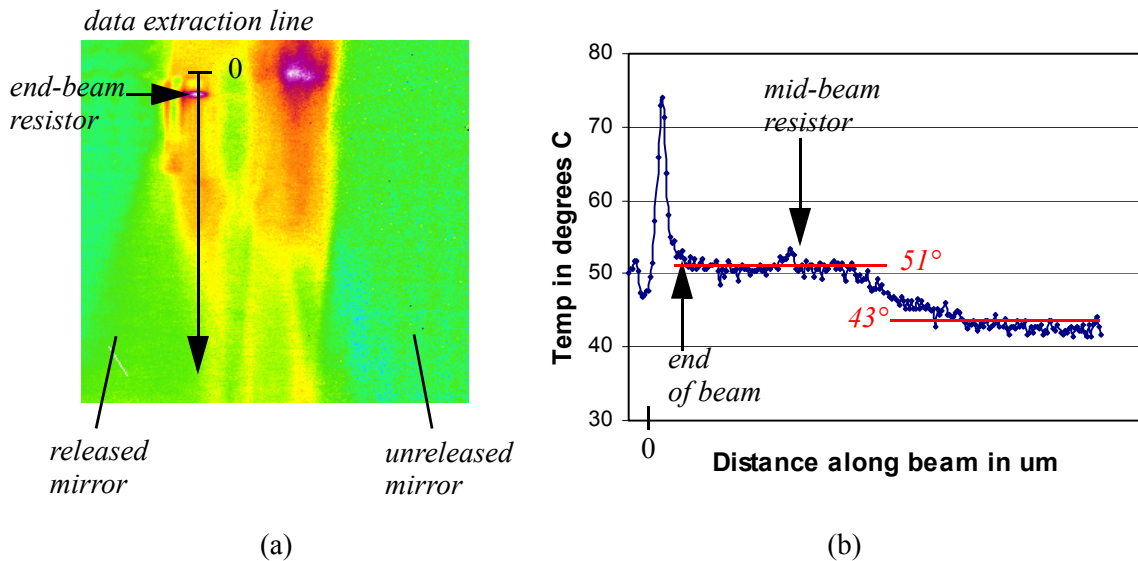
The measured temperature during actuation does not agree with the lumped parameter simulation results presented in Section 2.3.4, which predicts a higher temperature for the mid-beam resistor than the end-beam resistor. There are two possible explanations for this discrepancy: delamination of the metal in the actuator beams leading to a higher thermal resistance along the beam than used for the simulation, or greater heat loss to the surrounding air and the mirror than modeled in the simulation.

4.3 AC

AC response was measured by reflecting a He-Ne laser beam onto a Melles Griot 13 PDH silicon photodetector. A DC bias voltage of approximately 200 mV and a 100 mV peak-to-peak sinusoidal AC output voltage of a network analyzer were applied in series to a mirror actuator. The reflected laser spot was positioned on the silicon detector head using a 5-dof adjustable stage so that the photodetector response on an oscilloscope was a sinusoidally varying signal. The goal of the positioning step was to place the mean position of the center of the beam at the edge of the photodetector. Thus, the magnitude of the signal from the photodetector was proportional to the magnitude of the beam displacement. It should be noted that the absolute value of the angular displacement could not be reliably obtained from this measurement setup, but the relative magnitude of the displacements for each frequency, and hence the resonant frequencies are valid. After optimizing the sinusoidal response of the photodetector, its output was fed into a Hewlett-Packard 4395A network analyzer.

The frequency response of the device is shown in Figure 4.4. Eigenfrequencies were observed at 63 Hz, 192 Hz, and 286 Hz. The values of the eigenfrequencies obtained by simulation were 51 Hz, 192 Hz, and 263 Hz, corresponding to percentage differences between simulation and measurement of 22%, - 5% and 8.7%, respectively. The thermal cutoff was not observed due to the low values of mechanical resonance.

FIGURE 4.4 *Frequency response of a mirror pixel. Resonant peaks were observed at 63 Hz, 183 Hz and 286 Hz compared to the eigenfrequencies of 51 Hz, 192 Hz and 263 Hz obtained by simulation and reported in Section 2.4. The inset figures show the simulated mode of vibration for each of the eigenfrequecies.*
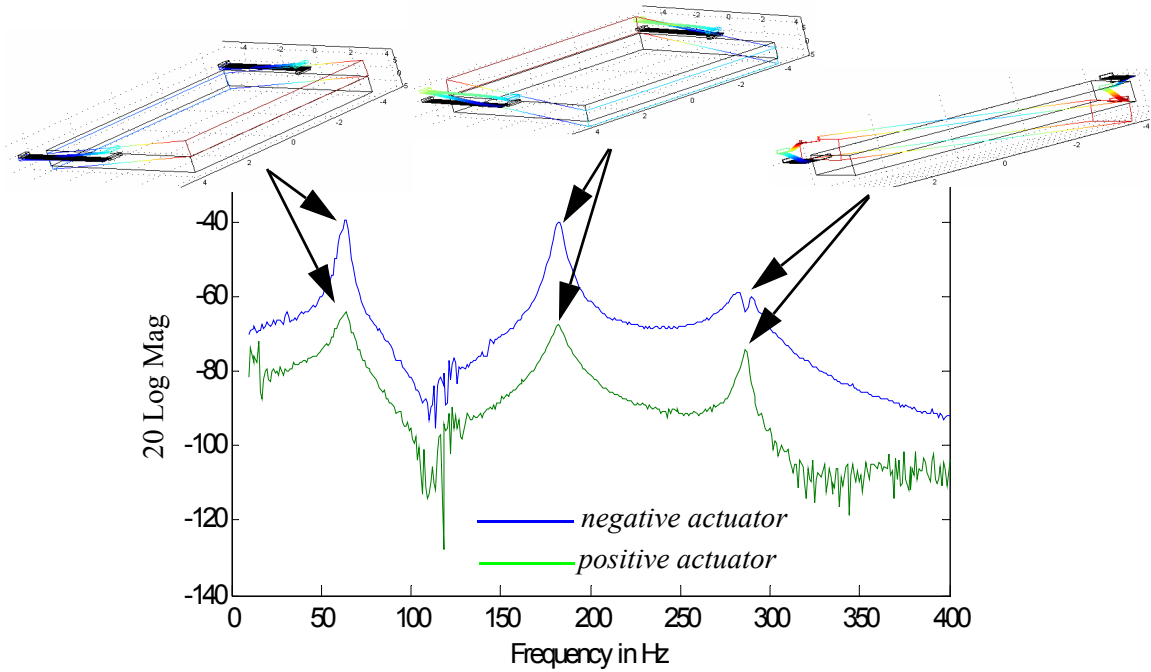
5

Conclusions and Future Work

"The apple cannot be stuck back on the Tree of Knowledge..."

Arthur Miller

5.1 Performance

Several devices of a single array were operational after post-CMOS fabrication. The devices demonstrated the potential to achieve the specified deflection angles and, with a maximum static deflection range of 38.9°, exceeded the rotations demonstrated by Xie's devices[53]. Actuation in a positive and negative sense was demonstrated on several pixels proving the validity of the concept.

5.2 Robustness

The lack of mechanical robustness of the design and process artifacts reduced the number of testable devices significantly and ultimately made the device unusable for anything other than lab-based testing. Future generations of the device will address the issue of mechanical robustness. One approach is to increase the number of actuators supporting one mirror, but this cannot be done without decoupling the actuator and mirror design to maintain a high fill factor. This direction will be pursued using flip-chip bonding of a separately designed and fabricated silicon mirror with a silicon post.

5.3 Mode Design

The position of the modes of the device were analyzed but not designed. In the future, the mode positions will be a design consideration in device topology selection. Finite element analysis proved to be an accurate predictor of mode position, with predicted eigenfrequencies varying from measured values by less than 20%. To improve the accuracy of simulation the methods of finite element analysis will be reviewed and improved. Several aspects of the design were observed to impact the modal response: actuator width, actuator length, mirror width and mirror thickness. Parametric analyses of the eigenfrequencies with respect to these parameters will be performed for subsequent designs to enable sound design decisions.

5.4 Thermal Simulation

The lumped parameter thermal simulations predicted a non-uniform thermal profile on the beam with a higher temperature at the mid-beam resistor than at the end beam. Quantum focus IR measurements showed the end-beam resistor to be at a higher temperature than the mid-beam resistor on the positive actuator, by up to 20° C.However, the analytic models of static mirror deflection, based on measured actuator temperature, showed agreement to better than 20%. This discrepancy could be due to the approximation of the temperature distribution along the beam, the simplicity of the analytic model which does not account for temperature variations in Young's modulus, incorrect approximations to the material properties of the beam members, or a combination of all of these. Mechanical frequency response limited the ability to measure the thermal cut-off frequency, which is typically in the kHz region for structures with dimensions of the actuator beams.

Future work will be done to improve the lumped parameter estimates of the thermal conductivities and capacitances of the various components of the design to better predict the thermal distributions observed on actuated devices and to improve the positioning and size of resistors. Embedded low resistivity polysilicon film will be explored to improve thermal distributions. Further NODAS model devel-

opment will continue so that coupled thermal, mechanical and electrical simulations can be performed with a view to integrating thermomechanical feedback systems. Tests will be developed to assess the thermal variation of the material parameters of the beam members.

5.5 Barrier Metal Attack

Partial and complete delamination of the aluminum in the actuator and in the mirror during release etch processing is thought to be caused by heating of the actuator during isotropic release etch. In a plasma reaction there are two sources of energy: energetic ion flux from the plasma arising from the bias across the plasma sheath and, the exothermic reaction of silicon and fluorine. It is speculated that one of these sources, or a weighted combination of both could be the root cause of the process shift that leads to metal 1 delamination. If the effect is caused by localized heating, its existence could be viewed in two ways: heating during etch shifts the process operating point and must be accounted for in the device and process design, and the change in the temperature of MEMS devices during release etch could provide a means to automatically identify the successful completion of the release etch process.

To explore the nature of the delamination phenomena, test structures will be employed that vary the surface area of a suspended plate structure and the quantity of silicon etching during the isotropic step of the release etch process. To obtain a valid result, the silicon backside of the test structures should be reduced to the same thickness for all structures and they should be suspended by a minimum dimension structure to reduce the effect of variation in release time across the structures. By optically measuring the lateral etch extent of the barrier metal attack on the plates the significance of each potential factor can be assessed.

Appendix A Post-CMOS Process Details

Step #	Operation	Process Goal	Materials and Conditions
1000	Tile CMOS chips with Si	1 - 4 CMOS chips surrounded by tiles of appropriate thickness.	Kapton tape
1020	Mount CMOS and tiles on glass	Uniform height of CMOS and silicon tile surface with minimum gap between die and tiles.	AZ4210 resist Spread - 6 s, 600 rpm Spin Time - 30 s, 2000 rpm
1050	HMDS coat		Spread - 6 s, 600 rpm Spin Time - 30 s, 3000 rpm
1070	AZ4210 Resist coat	Thickness resist 4.5 μm with uniform die surface coverage	Spread - 6 s, 600 rpm Spin Time - 30 s, 1500 rpm
1090	Expose backside pattern	Exposed resist	Heidelberg DWL Filter - 31%, Energy - 90%
1100	Develop exposed resist	No bridging of features and good edge definition	AZ Developer, room temp Time - To clear + 0.5 min.
1130	Mount glass wafer on 4" carrier wafer	Good adhesive and thermal contact between carrier wafer and glass wafer	Heat release tape 4" Si sub w/ 1.5 um oxide
1140	Backside silicon etch	Etch silicon to a depth of 220 um without eroding resist.	STS ASE DRIE Aniso, Etch only, DRIE iso
1170	Frontside oxide etch	Remove oxide from the surface of the die to expose MEMS structures and silicon surface.	Plasmatherm JAZZOXV Recipe
2000	Mount die in carrier chip	Aligned chip within pocket on the carrier chip with perimeter completely coated by SU8	Probe station 26G needle, 1mL syringe SU8 2002/2025 67%/33%
2010	Soft bake SU8	Drive out excess solvent to mechanically stabilize SU8	Hotplate, 70 ºC, 10 min.
2020	UV exposure of SU8	Create broken bonds to begin cross-linking of the epoxy.	Time - 10 min.
2030	Post-exposure bake	Complete the cross-linking of SU8 epoxy	Hotplate, 95º C, 20 min.
3020	Frontside release etch	Etch the silicon to a depth of 80 um, lateral etch for 10um to release the MEMS devices.	STS ASE DRIE Aniso, polymer removal, DRIE iso

A.1 STS DRIE Silicon Etch Conditions

Step Name	DRIE Aniso		Etch Only	Polymer Removal	DRIE Iso	
Step Type	Passivate	Etch	Etch	Etch	Etch	
Parameter	Value	Value	Value	Value	Value	Units
ASE Switching	Selected		Not Sel'd	Not Sel'd	Not Sel'd	
Cycles	285		N/A	N/A	N/A	
Process Time	~1:45:00 (by endpoint)		00:01:00	00:02:00	00:06:00	h:m:s
Cycle	1st	2nd	N/A	N/A	N/A	
Cycle Time	8	12	N/A	N/A	N/A	s
APC Mode	Manual		Manual	Auto	Auto	
APC Setting	58	58	58	N/A	N/A	%
Pressure	N/A	N/A	N/A	50	50	mTorr
C4F8	85	0	0	0	0	sccm
SF6	0	130	130		130	sccm
O2	0	13	13	80	0	sccm
RF Coil	600	600	600	600	600	W
RF Platen	0	12	12	12	12	W
Matching	Auto	Auto	Auto	Auto	Auto	

A.2 Plasmatherm Oxide Etch Conditions

Step Name	Pre-O2 Clean	Oxide Etch	Post-O2 clean	
Parameter	Value	Value	Value	Units
Pump	Turbo	Turbo	Turbo	
Terminate by	Var Time	Var Time	Var Time	
Default Time	20	300	10	min.
Pressure	50	100	200	mT
CHF3	0	22.5	0	sccm
O2	50	16	80	sccm
Power	100	100	100	W

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