

A Wide-Band Low Noise Amplifier Synthesis

Methodology

by

ABHISHEK JAJOO

A thesis submitted in partial fulfillment of the requirements

for the

degree of

Master of Science

August 2005

Department of Electrical & Computer Engineering

Carnegie Mellon University

Pittsburgh, Pennsylvania, USA

Advisor: Dr. Tamal Mukherjee

Second Reader: Professor C. Patrick Yue

Abstract

Three generations of a wide-band Low Noise Amplifier (LNA) are designed in a 0.35 μm BiCMOS technology. The topology chosen is a noise-canceling topology with shunt resistive feedback for wide-band matching to 50 Ω . The second generation design was fabricated and measured. It had a measured gain of 17 dB and a bandwidth of 2.6 GHz. Its Noise Figure is below 3 dB over the LNA bandwidth, with minimum value of 2.4 dB. It draws 13mA current from a 2.5 V supply. This LNA has an excellent figure of merit $FOM = (S_{21} \times BW)/(NF \times P_{DC})$ compared to the other wide-band LNAs.

Based on the experience gained from the first two design generations, a synthesis-based design strategy is developed. A third generation LNA is synthesized using this strategy. It optimizes between the various noise sources affecting NF with the other parameters involved in the FOM, leading to a LNA that outperforms earlier designs by about 2x.

Acknowledgement

Even though I am the author, I don't deserve the entire credit for this work. Several others have contributed towards its completion and they, at the least, deserve thanks and mention. First of all, I would like to thank my advisor Dr. Tamal Mukherjee not only for his availability for discussions but also his painstaking efforts in pointing out holes and raising questions during the course of this work, without which this work would not have been possible. He also reviewed this report and his feedback, led to significant improvements. I would also like to thank Professor C. P. Yue for taking time out of his busy schedule to read my thesis and suggest improvements.

Mary L. Moore, the executive administrator of Carnegie Mellon MEMS Laboratory, deserves special thanks for her effort in smoothing out administrative issues during the time involved in this research. She was also kind enough to take time out, at very short notice, of her busy schedule to proofread this report.

I have learnt a lot from discussions with my colleagues - Altug Oz, Umut Arslan, Chiung-Cheng Lo, Hasan Akyol, Fang Chen, Michael Vladimer, Sarah Bedair, Peter Gilgunn, Amy Wung, Michael Sperling, Ryan Magargle, Sounil Biswas - and would like to thank them. They always kept the environment very cheerful and were readily available for discussions and any kind of help.

Finally, I would like to thank my parents for instilling a sense of self, honesty and love for learning in me. I would also like to thank my brother and all my friends and relatives who showed their love, moral support and encouragement throughout the course of this work.

This work was funded in part by C2S2, the MARCO Focus Center for Circuit & System Solutions, under MARCO contract 2003-CT-888 and by the ITRI Lab at Carnegie Mellon.

Table of Contents

Abstract	i
Acknowledgement	ii
Table of Contents	iii
List of Figures	v
Chapter 1 Introduction	1
1.1 Narrow-band vs. Wide-band LNA.....	2
1.2 Wide-band Amplifier Design.....	3
1.3 Technology Choice	4
1.4 LNA Specifications.....	4
1.5 Figure of Merit.....	5
1.6 LNA Synthesis.....	6
1.7 Report Outline.....	6
Chapter 2 LNA Topology	7
2.1 Topology Choice.....	7
2.2 Noise Cancelling Principle	10
Chapter 3 Circuit Synthesis	13
3.1 Complexities in RF Design.....	13
3.2 Automated Synthesis	14
Chapter 4 Results	21
4.1 First and Second Generation LNA Designs.....	21
4.2 Measurement Results.....	24
4.2.1 S-Parameters	25

4.2.2 Noise Figure.....	26
4.2.3 1 dB Input Compression Point (ICP).....	27
4.2.4 Input-Referred Third Order Modulation Point (IIP3).....	28
4.3 Second Generation Design Result Summary.....	29
4.4 Third Generation Design	30
4.4.1 NeoCircuit Synthesis Results.....	33
4.4.2 Analysis of the 3rd Generation Synthesized LNAs	34
4.4.3 Simulation for Extracted Circuits	37
Chapter 5 Conclusion and Future Work.....	39
References	40
Appendix: Significance of 3 dB Noise Figure	42

List of Figures

Figure 1-1	Multi-band radio receiver front end with (a) narrow-band LNA and (b) wide-band LNA.	2
Figure 2-1	Shunt-feedback common emitter schematic	8
Figure 2-2	LNA with emitter follower as second stage.	9
Figure 2-3	Noise canceling principle with first amplifier stage	10
Figure 2-4	Noise canceling principle with both amplifier stages	10
Figure 2-5	Final topology	11
Figure 3-1	NeoCircuit simulation time summary for two point synthesis	15
Figure 3-2	NeoCircuit simulation time summary for entire band synthesis	15
Figure 3-3	Small signal model of HBT	16
Figure 3-4	Screenshots of NeoCircuit results showing the values of specifications for the best synthesis	20
Figure 4-1	Gain matching requirement for maximum first stage noise cancelling	21
Figure 4-2	NeoCircuit variables and goals for the first generation design	22
Figure 4-3	Measured S-Parameters	25
Figure 4-4	Noise-Figure measurement results	26
Figure 4-5	Compression point plot.	27
Figure 4-6	IIP3 Plot	28
Figure 4-7	Wide-band LNA Figure of Merit vs. Lithographic feature size	30
Figure 4-8	gm/I_c vs. I_c for HBT	32
Figure 4-9	NeoCircuit goals window with equal weights on all goals	33
Figure 4-10	NeoCircuit Synthesis results for the (a) first NeoCircuit run with equal weights (3rd	

	generation (Initial) design) and (b) second run with modified weights (3rd generation (Final) design).	34
Figure 4-11	NeoCircuit goals window with weights on some goals changed	34
Figure 4-12	Comparing minimum NF and normalized error in first stage noise cancellation across three the designs	35
Figure 4-13	Comparison of gain from transistor Q1 and Q2 across the three designs.	36
Figure 4-14	Normalized transconductance of transistors Q1 and Q2 across the three designs	36
Figure 4-15	Normalized collector current I_C and (g_m/I_C) for transistor Q1 across the three designs.	37

1 Introduction

Wireless communication systems use electromagnetic signals, with frequencies in the range of hundreds of kilohertz to several gigahertz, for the transmission and reception of information through air. Frequencies in this range are called radio frequency (RF). In any wireless system, information to be sent (e.g., voice) is first modulated, then put onto the radio frequency (RF) carrier and amplified before transmission. On the other end, received RF signals are amplified, converted to lower frequencies and then demodulated to obtain the information (voice) that had been sent. For modern wireless systems, the wireless channel interface (also known as the front end) typically has to deal with GHz frequency RF signals. Although sub-blocks for these front ends are analog in nature, their design is much more complicated than classical low-frequency analog design. Several factors, such as the ability to operate at low signal power levels, high dynamic-range, impedance matching, coupling and circuit parasitics, make the design of such front-end blocks complicated.

Traditional wireless communication systems are designed for only one communication standard. However, the demand for convergence of wireless services, in which users can access different standards from the same wireless device, is driving development of multi-standard and multi-band transceivers. Thus, future RF front-ends will need to operate over multiple frequency bands. This report focuses on the design of a sub-block called low-noise amplifier (LNA) for use in a multi-band multi-standard complimentary metal-oxide semiconductor (CMOS) integrable receiver front end for portable applications. A typical RF receiver front-end looks like *one* of the multiple parallel arms shown in Figure 1-1. In addition to the LNA, the front-end is comprised of an antenna, a band-pass filter (BPF), a voltage-controlled oscillator (VCO) and a mixer. The LNA is required to amplify the signal in the band selected by the BPF, from a wide range of frequencies. The amplified signal from the LNA can then be converted to a lower frequency by the mixer.

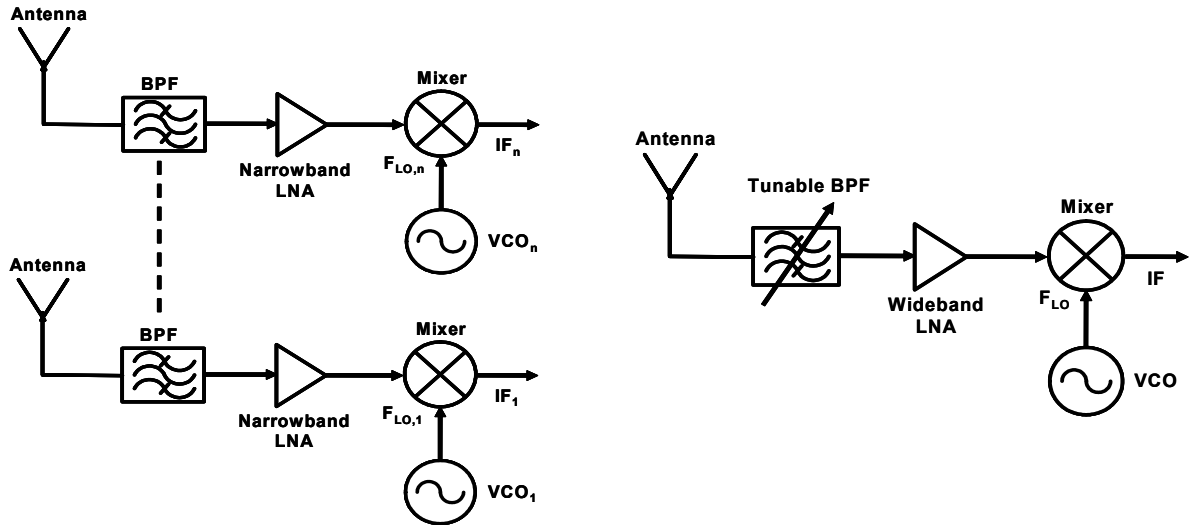


Figure 1-1 Multi-band radio receiver front end with (a) narrow-band LNA and (b) wide-band LNA.

For any RF front-end, several design decisions need to be made. The first is the overall architecture. Once the architecture is selected, the circuit topologies for various sub-blocks need to be designed, next is the choice of fabrication technology. The issues involved in these decisions are outlined in the following three sections. They are followed with a definition of the key LNA specification parameters. Target values for these specifications will also be decided. Next, these specifications will be combined to a single parameter, called the figure-of-merit (FOM).

1.1 Narrow-band vs. Wide-band LNA

The optimal LNA should add only the minimum amount of noise as it amplifies the signal, increasing the overall signal-to-noise ratio after it is done. This noise performance characteristic of an LNA is measured by its noise figure (NF). The lower the NF the better the LNA, as it means less noise is added by the LNA compared to its gain. LNA requirements for the multi-band multi-standard receiver described in the previous section could be satisfied in two ways. First, it could be accomplished by using multiple input stage for each frequency band of interest. This will require multiple classical narrow-band LNAs [1] as done in [2] and shown in Figure 1-1(a). The second option is to use a wide-band LNA in conjunction with a tunable BPF as shown in Figure 1-1(b).

The advantage of the first approach is that the performance of each front-end can be optimized for each frequency band. However, as each of the LNAs is typically LC tuned and integrated inductors are the most area consuming on-chip components, a large amount of chip area is required. This increased area implies high cost. On the other hand, the second option of using a wide-band LNA allows some hardware sharing and has the area, hence cost advantage. Wide-band LNA based RF front-end with multiple BPF have been reported in [3] and [4]. In these examples, the LNA is shared, however, the BPF filters are not. The obvious extreme end for this trend is sharing both the LNA and the filter, as shown in Figure 1-1(b). Such an architecture is now feasible with the potential for a CMOS compatible tunable BPF [5]. As a result of these advantages and trends, this report focuses on a single wide-band LNA architecture.

1.2 Wide-band Amplifier Design

A variety of wide-band amplifier designs have previously been proposed. One approach is the distributed amplifier, in which several lumped inductor and capacitor elements interconnect simple amplifier topologies as in [6]. In this approach, each stage adds to the gain. Due to the multiple stages, there is a high component count. Each of the many active and passive devices introduce noise into the system, which adds up to an overall NF that is too large for LNA applications. To reduce the noise from the active devices, the number of the active devices can be reduced. Thus, fewer amplifier stages are desirable. Although ideal (loss-less) inductors have no noise sources, practical inductor implementations have loss, and therefore, also act as a noise source. Inductor noise can be completely eliminated by using an inductor-less topology. This also substantially reduces the circuit area, as on-chip passives occupy larger chip area compared to active transistors. The resulting noise in these inductor-less topologies is solely from the transistors. To further reduce this noise, an approach that removes some of the injected transistor noise in the wideband LNAs is desired. This report uses one such inductor-less, noise cancelling topology [7].

1.3 Technology Choice

RF front-ends have been designed in a wide variety of technologies, including Gallium Arsenide (GaAs), Silicon Bipolar Junction Transistor (BJT), RF CMOS and Silicon Germanium (SiGe) BiCMOS. The desire for integration with CMOS baseband components limits our choice to RF CMOS and SiGe BiCMOS technologies. The advantage of such an integration will be reduced system size and cost (both reduced as there are fewer discrete components to assemble on a board). SiGe bipolar transistors, also called HBTs (Heterojunction Bipolar Transistors), have higher g_m/I and better noise characteristics compared to CMOS transistors [8]. This higher g_m/I implies more gain for the same amount of bias current (which is directly proportional to power consumption). The high gain can be traded off to improve the NF, by burning less current which will reduce the shot noise generated by the transistors, as shot noise is proportional to the bias current. Also, the HBT has better parametric yield as its performance depends on the vertical diffusion, a geometrical parameter that is less variable than the CMOS lateral gate length. Therefore, the LNA will be designed in a SiGe BiCMOS technology.

1.4 LNA Specifications

Performance specifications used to characterize a LNA include noise, power gain, impedance matching, power consumption and bandwidth. In this section we define the LNA specifications and specify their target values.

Noise added by any circuit or system is characterized by a term called NF. It can be shown that NF of 3 dB means that the signal-to-noise ratio (SNR) degrades by factor of two. As derived in detail in the appendix, this would mean that the noise power added by the system will be same as the noise at the input amplified by the amplifier gain. Thus, the target value for the NF is set to be below 3 dB over the entire bandwidth.

Having a high power-gain is equally important as having low noise. In RF terminology gain is reported as S_{21} . In the overall system NF expression, noise of the following stages in the cascade are divided

by the power gain of the LNA. This means that high gain LNA will reduce the ability of the following stages to degrade the system SNR. Based on [1], [6], [7], the target value of the S_{21} is set to be greater than 15 dB.

50 Ω is a standard impedance for most of the RF waveguides used to connect LNA chips with off-chip filters or mixers. For maximum power transfer, most RF circuits are designed to have input and output impedances of 50 Ω . When the interconnect is on-chip (meaning that they are much shorter than the wavelength at the desired frequency of operation) the interconnect does not behave as a waveguide and matching to 50 Ω is not required for maximum power transfer. However, as the LNA will be tested stand alone using 50 Ω RF measurement cables and test equipment, the input and output impedance are designed to match to 50 Ω . S_{11} and S_{22} are measures of the input and the output match. A value of -10 dB means matching to within 20 %. Therefore the target value for S_{11} and S_{22} is set to be below -10 dB over the entire usable bandwidth.

The bandwidth (BW) of the amplifier was set by the range of frequencies that the multi-band receiver front-end has to support. The target value for the bandwidth is set to be 2.5 GHz so that LNA covers AMPS, PCS and ISM bands. Another goal was to minimize the power consumed to enable long operational life in a limited battery power portable application.

1.5 Figure of Merit

One LNA circuit may have a larger BW, while another may have a larger gain, making comparison between different LNAs difficult. To enable such a comparison, designers typically map the multitude of circuit specifications into a single scalar figure of merit. For the case of the wide-band LNA the FOM is defined as:

$$FOM = \frac{S_{21} \times BW}{NF \times P_{DC}} \quad (1.1)$$

It takes into account the power gain (S_{21}), bandwidth (BW), noise figure (NF) and power consumed (P_{DC}). It is inspired by expression for FOM for narrow-band LNAs in [9] but includes the BW term as this report focuses on wide-band LNAs. Clearly the best circuit will have the highest FOM.

1.6 LNA Synthesis

The need to simultaneously meet multiple specifications makes RF circuit design complicated. To manage the design complexity, we use an automated circuit synthesis approach similar to [6]. Individual design constraints for each specification is combined with FOM maximization to obtain the best possible design.

1.7 Report Outline

Chapter 2 discusses the LNA topology choice and principle of operation. Chapter 3 describes the design methodology using automated design tool NeoCircuit[®]. Chapter 4 presents the results (synthesis, simulation and measurement) and their comparison to the literature. Chapter 5 concludes the thesis and outlines future plans.

2 LNA Topology

The architecture and technology decisions in the previous chapter constrain us to a wideband LNA implemented in SiGe BiCMOS technology. We now need to select the circuit topology before we can size and bias the transistor schematic. This chapter will start by describing the design issues affecting the LNA topology, and lead to the choice of the noise-cancelling topology for the LNA designed in this report.

2.1 Topology Choice

Many common LNA topologies are ruled out either because of their inability to provide impedance match over the wide range of frequencies or their inability to provide wide bandwidth with low NF [7]. Therefore, we start with a basic single-stage amplifier topology and expand on it to arrive at the final topology by considering requirements for the LNA one at a time. Each time we fail to meet the desired requirement, a topology change will be instituted to help extend the LNA's performance.

Power gain is a primary performance specification for the LNA. Our starting point is one of the three simple single-stage amplifier topologies, namely common-emitter (CE), common-collector (CC) and common-base (CB). Of these, the common-emitter (CE) is the only topology with both voltage and current gain. This means that it is capable of giving power gain, in presence of either current or voltage as input. Unfortunately, the CE topology has an input impedance that is too large for RF applications. A resistive shunt feedback as shown in Figure 2-1 can reduce the input impedance to achieve $50\ \Omega$ over a wide range of frequencies.

Assuming that

- (a) the extrinsic base resistance $r_b \ll r_\pi$

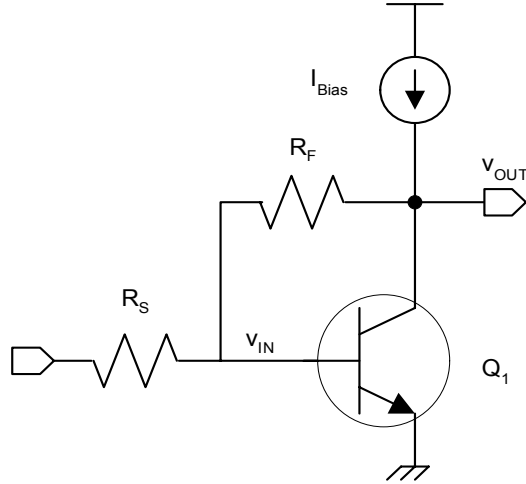


Figure 2-1 Shunt-feedback common emitter schematic

(b) the feedback resistance $R_F \ll r_o$ (the transistor output resistance)

(c) current gain β is large

then the small signal gain, input and output impedance of the circuit in Figure 2-1 are given by [10]:

$$A_V = -(g_{m1}R_F - 1) \quad (2.1)$$

$$R_{in} = 1/g_{m1} \quad (2.2)$$

$$R_{out} = (R_S + R_F)/2 \quad (2.3)$$

Setting $R_{in} = R_S = 50\Omega = R_{out}$ in equation (2.2) & (2.3) leads to $R_F = 50\Omega$ and $g_{m1} = 1/(50\Omega)$. Plugging g_{m1} and R_F into equation (2.1) unfortunately implies zero gain, because impedance matching (input and output) conditions are both coupled to the gain. In the above equations there are three constraints (gain, input and output impedance) and two variables or degrees of freedom (g_{m1} and R_F). Therefore the three constraints cannot be met independently. Decoupling these three constraints requires adding one more variable. We can obtain that by adding a second stage, as shown in Figure 2-2.

For implementing the current source, I_{Bias} , in Figure 2-1 a p-type metal oxide semiconductor field effect transistor (MOSFET or MOS) is preferred over BJT. This is because MOS current sources require less voltage headroom compared to BJT current sources. In a PNP type BJT the emitter-base (EB) junction has to be forward biased and the base-collector (BC) junction has to be reverse biased. The voltage head-

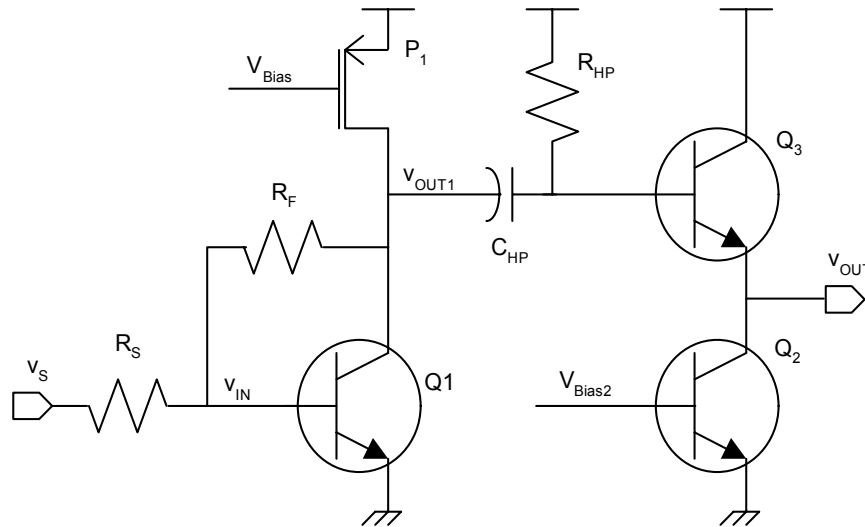


Figure 2-2 LNA with emitter follower as second stage.

room needed by such a PNP source, is set by the emitter-collector (EC) voltage. This EC voltage has to be more than the EB voltage. In a PMOS current source, the voltage between source and drain, which is the voltage headroom, has to be greater than gate-source voltage, minus the threshold voltage. This means the source-drain voltage can be less than gate-source voltage and the device will still work as a current source. Furthermore, the HBT turn-on emitter-base voltage is higher than the CMOS gate-source threshold voltage. Thus, MOS current sources require less voltage headroom compared to HBT current sources. Moreover, the PNP type HBT is typically not available in SiGe BiCMOS processes.

The high-pass filter constituted by R_{HP} and C_{HP} is used to independently bias the two stages. This new second stage decouples the gain and the output impedance match requirements, as output impedance is now determined by the output impedance of the emitter follower (second stage). However, this is at the expense of the added noise from the additional devices in the second stage. Note that this second stage does not provide any additional gain, but does add to the noise. Some noise reduction is possible by modifying this circuit to cancel some of the generated noise. This approach is described in the next section.

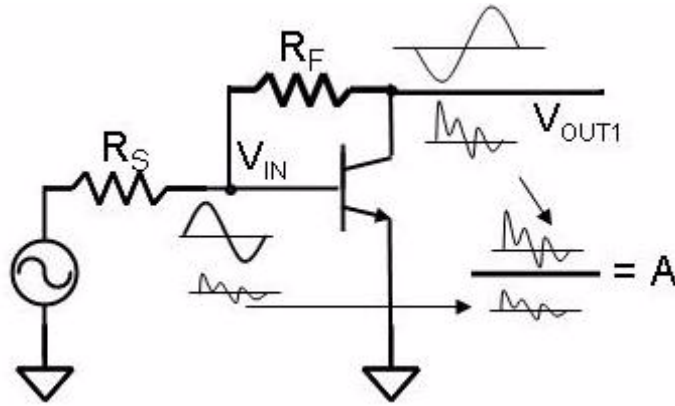


Figure 2-3 Noise canceling principle with first amplifier stage

2.2 Noise Cancelling Principle

The noise cancelling principle [7] is explained using Figure 2-3 and Figure 2-4. It takes advantage of the resistive feedback through R_F , to cancel the noise from the transistors Q_1 and P_1 . The noise originating in these transistors appears at the output of the first stage (V_{OUT1}). The resistor R_F causes this noise to appear at the input (V_{IN}) with some attenuation. The exact value of this attenuation can be calculated by using the small signal model of the first stage. A detailed derivation of the expression of the attenuation factor A can be found in [10]:

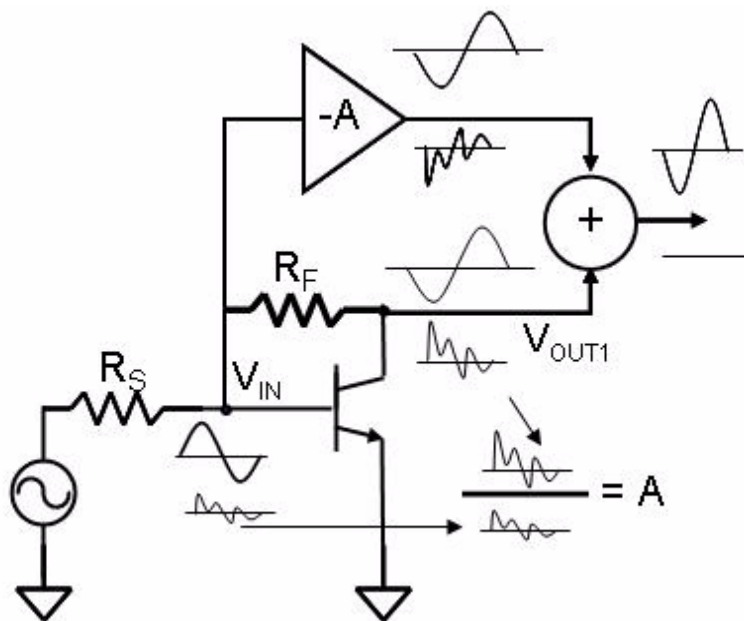


Figure 2-4 Noise canceling principle with both amplifier stages

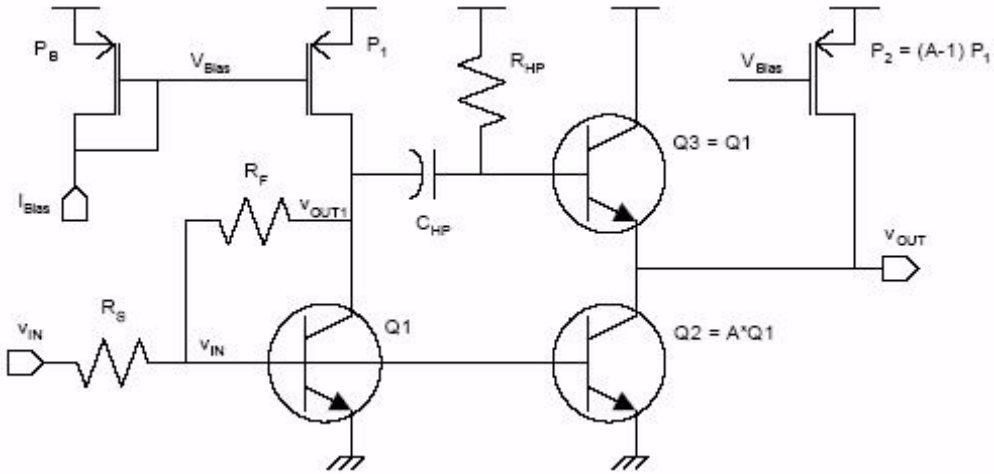


Figure 2-5 Final topology

$$A = \frac{R_F}{R_S} + 1 \quad (2.4)$$

The input signal at V_{IN} is amplified to the first stage output according to equation (2.1). Since the value of the gain is negative, the amplified signal at V_{OUT1} will be out of the phase with the input signal. As the value of the attenuation factor is positive, the attenuated noise at the input will be in phase with the noise at V_{OUT1} , as shown in Figure 2-3. This property of the circuit can be exploited to cancel some of the noise originating in transistors Q_1 and P_1 .

Noise cancelling can be achieved by connecting an inverting amplifier of gain $-A$, which is negative of the attenuation factor seen by the noise at V_{OUT1} as it is fed back to V_{IN} , and summing its output with V_{OUT1} , as shown in Figure 2-4. In this amplifier, both the desired signal and the attenuated noise at the input are amplified and undergo phase inversion. It can be easily seen (and is shown in Figure 2-4) that when inverting amplifier output is summed with the signals at V_{OUT1} , the noise gets cancelled and desired signals add up.

A transistor implementation of the concept demonstrated in Figure 2-4 is shown in Figure 2-5. The reasoning for the sizing relationships between the devices has been arrived at previously [10]. The summing circuit is implemented using transistor Q_3 . Inverting amplifier is implemented using transistor Q_2 . In order

to set its gain to be $-A$ the ratio g_{mQ2}/g_{mQ3} has to be set to be equal to $-A$. The current source is implemented by transistor P_2 in Figure 2-5. It robs current from Q_3 and helps set this ratio. This device (P_2) adds some noise of its own. However, as it appears after the first gain stage, its noise contribution is not as critical as the components of the first stage. It is shown [10] that the NF of topology in Figure 2-5 is better than that in Figure 2-2.

The next chapter describes the complexities of designing a wideband LNA. The formulation of a wideband LNA synthesis problem is then described, followed by the use of an automated synthesis tool for synthesizing the amplifier.

3 Circuit Synthesis

With the fabrication technology, architecture and transistor schematic topology selected, the next task is to determine the device sizes and circuit bias point needed to achieve the desired performance. In case of RF circuit design this could be an extremely challenging task. This chapter begins with a description of the challenges in RF circuit design, leading to the argument for the use of the automated synthesis tools for sizing and biasing. Following this is a description of the synthesis tool used as well as the formulation of the wide-band LNA design problem for efficient circuit synthesis.

3.1 Complexities in RF Design

There are many competing specifications like power, noise, gain, linearity and impedance matching for RF sub-blocks. At high frequencies device and interconnect parasitic have to be considered, as they adversely affect circuit performance. Even though RF circuits have fewer devices compared to the conventional analog circuits, these factors make RF design extremely complex. In such a situation manual optimization of circuit becomes intractable.

Fierce market competition and rapidly evolving standards are resulting in shorter design cycles. However, the time required for designing a typical RF circuit, even for an experienced designer, remains constant, on the order of a few weeks.

Automated synthesis tools are now available with the promise of being able to search the design space faster and more exhaustively than an experienced designer. The designs in this report exploit one such commercially available synthesis tool: NeoCircuit.

3.2 Automated Synthesis

Synthesis tools suggest a design candidate, evaluate the circuit performance, and then perturb the design candidate iteratively to improve the design. NeoCircuit employs simulation for performance evaluation and uses an optimization-based synthesis engine to search the design space. NeoCircuit users enter the circuit topology and setup the circuit testbenches and the simulation needs for evaluating the candidate circuit's performance. Also, the list of circuit design variables and the list of performance specifications must be entered into the software.

NeoCircuit is the circuit optimization engine for the custom IC design suite in Cadence. It interfaces to Cadence Virtuoso Schematic Editor (where the circuit topology is entered by the user) and employs Cadence SpectreRF to evaluate the performance of candidate circuits that it considers as it traverses the design space while sizing and biasing the schematic. The NeoCircuit User Interface uses a single window that is partitioned into a page for each type of object that the user specifies. The variables page is used to set the device relationships and independent variables. At the simulation page, one specifies simulation information and extracts simulation output. Computations on the simulation output are entered in the goals page and used to define the design goals. The results of the synthesis run can be viewed at the results page.

The time required to synthesize a design is governed primarily by the amount of the time required to simulate each candidate design. Therefore, one needs to set up the simulation environment carefully. Circuit evaluation of the wide-band LNA is ideally performed over the entire desired bandwidth. Frequency analysis in a circuit simulation requires time-consuming matrix inversions for each frequency point in the analysis. So, evaluation over the entire bandwidth becomes computationally expensive. As the Bode plot of the frequency response of the noise cancelling LNA topology is flat between the high pass filter cutoff frequency and the amplifier -3 dB frequency, the linear S-parameter analysis for the input and output match, gain and noise specification is performed only at two frequency points in the desired bandwidth. To verify this short-cut simulation approach, several synthesis runs were done with simulation performed over the entire desired LNA bandwidth and only at two frequency points. These experiments confirmed that simu-

Diagnosics

Summary

Points	8545	Points/Hour	3731.05
Mean Time/Point	0:00:07	Total Errors	44
Total Nodes	14	Elapsed Time	2:17:24

Simulations

Name	Avg (s)	Curr #	# Errs
DC	7.43	0	2
SP	6.46	0	0
neocalc	74.58m	0	0

Machines

Name	Jobs
garcia.ece.cmu.edu	2
holly.ece.cmu.edu	2
joplin.ece.cmu.edu	2
jennings.ece.cmu.edu	2
entwhistle.ece.cmu.edu	2
elvis.ece.cmu.edu	2
cobain.ece.cmu.edu	2

Figure 3-1 NeoCircuit simulation time summary for two point synthesis

lating at only two frequency points leads to less overall synthesis time compared to when the simulation is done over the entire LNA bandwidth. Figure 3-1 and Figure 3-2. show NeoCircuit screenshots for the two-frequency and multi-frequency synthesis runs. To ensure that the flat-gain assumption in the two-frequency case remains correct during the synthesis, the cutoff frequency of the high-pass filter is constrained to be smaller than the lower of the two frequency points. The higher of these two points is the maximum input signal frequency that needs to be amplified by the specified gain.

Diagnosics

Summary

Points	8545	Points/Hour	3235.8
Mean Time/Point	0:00:08	Total Errors	49
Total Nodes	14	Elapsed Time	2:38:26

Simulations

Name	Avg (s)	Curr #	# Errs
DC	6.08	0	0
SP	6.85	0	0
neocalc	86.18m	0	0

Machines

Name	Jobs
garcia.ece.cmu.edu	2
holly.ece.cmu.edu	2
joplin.ece.cmu.edu	2
jennings.ece.cmu.edu	2
entwhistle.ece.cmu.edu	2
elvis.ece.cmu.edu	2
cobain.ece.cmu.edu	2

Figure 3-2 NeoCircuit simulation time summary for entire band synthesis

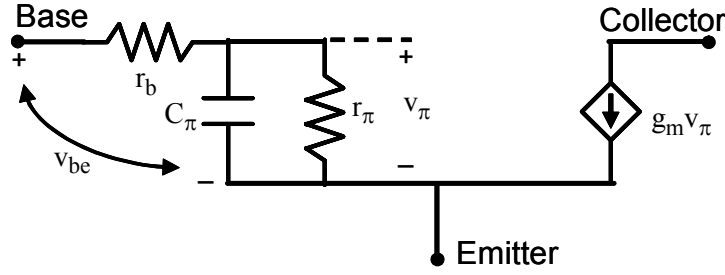


Figure 3-3 Small signal model of HBT

Non-linear analysis takes much more time per candidate evaluation than linear analysis, and hence is only performed at one of the two frequencies. The frequency dependence of IIP3 can be understood from the ratio of the Taylor's series coefficients of the collector current of a HBT. Gain is proportional to $g_m R_{out}$, where R_{out} is the output resistance of the PMOS load transistor. As the MOS transistor is more linear than the HBT, the non-linearity will be dominated by HBT's non-linearity. HBTs are more linear at higher frequency, as shown by analyzing the small signal model of an HBT (as shown in Figure 3-3.). We need to obtain the relation between the input voltage (v_{be}) and output current (I_c), and then use this relation to find the frequency dependence of IIP3.

The output current I_c depends on the effective base-emitter voltage v_π as given by equation (3.1). In turn, the v_π dependence on the externally applied voltage v_{be} can be obtained by a voltage divider as shown in equation (3.2).

$$I_c = I_{c, sat} \cdot e^{\frac{v_\pi}{V_T}} \quad (3.1)$$

$$v_\pi = \frac{v_{be} \cdot \frac{r_\pi}{1 + sr_\pi C_\pi}}{r_b + \frac{r_\pi}{1 + sr_\pi C_\pi}} \quad (3.2)$$

$$= \frac{r_\pi v_{be}}{r_\pi + r_b + sr_\pi r_b C_\pi} = H(s)v_{be}$$

The Taylor series expansion of I_c in equation (3.1) is shown in equation (3.3) and also expressed in terms of v_{be} ,

$$\begin{aligned} I_c &= I_{c,sat} \cdot \left[1 + \frac{v_\pi}{V_T} + \frac{1}{2!} \left(\frac{v_\pi}{V_T} \right)^2 + \frac{1}{3!} \left(\frac{v_\pi}{V_T} \right)^3 + \dots \right] \\ &= I_{c,sat} \cdot \left[1 + \frac{H(s)}{V_T} v_{be} + \frac{1}{2!} \left(\frac{H(s)}{V_T} \right)^2 v_{be}^2 + \frac{1}{3!} \left(\frac{H(s)}{V_T} \right)^3 v_{be}^3 + \dots \right] \end{aligned} \quad (3.3)$$

For time-variant, memory-less systems with input (x), and output (y) we can assume that [11],

$$y = a_0 + a_1 \cdot x + a_2 \cdot x^2 + a_3 \cdot x^3 + \dots \quad (3.4)$$

and for this system input IIP3 is defined as [11],

$$IIP3 = \sqrt{\frac{4}{3} \cdot \frac{|a_1|}{|a_3|}} \quad (3.5)$$

On similar lines IIP3 for HBT, using expression of I_c from equation (3.3), after some simplification becomes,

$$IIP3 = \frac{2\sqrt{2}V_T}{H(s)} \quad (3.6)$$

Plugging the expression for $H(s)$, it can be seen that IIP3 improves with frequency. Thus, IIP3 needs to be evaluated only at the lower frequency point for the candidate designs during synthesis. If the IIP3 specification is met at the lower frequency point, it would be met over the entire band.

It should be noted though, that the above analysis considers only the low frequency non-linearity behaviour. The exact frequency dependence of the IIP3 must be considered using Volterra Series with frequency dependent coefficients [12]. Nevertheless for the objective of setting the optimization condition the aforementioned analysis is sufficient as the desired frequency range is small to have any significant IIP3 variation.

NeoCircuit creates candidate designs by iteratively changing the value of the device parameters that had been declared as design variables during the setup process. For the LNA in this report, the variables used during the synthesis include device geometries (lengths and widths of the MOS gates, polysilicon resistors and MIM capacitors), device multiplicity as well as the bias current. The technology used is Jazz's 0.35 μm BiCMOS process with 60 GHz f_T SiGe devices. A few select HBT emitter lengths and widths are available in this technology. NeoCircuit can handle both continuous or discrete parameter sets for design variables. However, in the Jazz design kit, changes to the HBT's emitter length, width and number of emitter require changes to the model names in the final circuit netlist. As NeoCircuit cannot change device model names during synthesis, these parameters can't be set as design variables. Therefore, we manually identified an emitter geometry such that the HBT's f_T is about 10x the maximum intended frequency of operation while burning minimum current. Thus, the sole design variable related to the HBTs in the LNA is the device multiplicity.

The LNA performance targets also has to be specified during NeoCircuit setup. Goals can be specified as constraints or design optimization objectives. Constraints can be single-sided, specified as an inequality (either less than or greater than a certain value) or double-sided (requiring the parameter to lie in a range). Optimization objectives can be either maximized or minimized. NeoCircuit allows users to prioritize between the goals by setting weights. In the presence of trade-offs among various specifications, optimizing synthesis by focusing on individual specification can be an impossible task. Therefore, the LNA FOM is used as a design optimization objective (to be maximized as described in Section 1.5). Once NeoCircuit meets the individual performance specification goals, it will work at improving the critical goals that are aggregated in the FOM expression, thereby improving FOM. The overall synthesis effort can also be set to be low, medium or high. Weight and synthesis effort settings affect the way the design space is searched and determines the outcome of the synthesis. Therefore, it is important to know how to use these features to get good synthesis results. The designs in this report used the following strategy.

- Set up the goals to have a weight of one. Synthesize for maximum FOM with medium effort. The synthesis results help determine if targeted goals are achievable.
- If all goals are met during the first synthesis run then a second synthesis run with higher specifications for the critical goal can be attempted.
- If all goals are not met during the first run, increase the weight on the goals that did not meet the specified target values. This will force NeoCircuit® to work harder at meeting those goals at the cost of the other goals. If among these 'other' goals there are certain critical goals which one would like to be compromised least, then one should increase their weights too. For example, if NeoCircuit® is failing to meet S_{11} during the first run, then its weight should be increased during the second run. But if the designer would like to prevent NeoCircuit from trading off the tougher S_{11} specification with S_{21} , NF and FOM, so weights on these critical goals should also be increased. This time, synthesize with high effort.
- If goals are still not met then re-synthesize with either of following, until the goals are met:
 - Revise target values. They are infeasible for the circuit topology and the fabrication process.
 - Increase the weights further

To establish the validity of the idea that setting FOM as a goal to be maximized will improve the synthesis results, two synthesis runs were done: one with FOM as a design optimization objective and another without it. For these runs, the NeoCircuit synthesis FOM was defined as $\frac{S_{21}}{NF \times I_{DC}}$ (as a BW upto 3 GHz was desired and V_{DC} is a constant, these terms were excluded from the definition in equation (1.1)). Screenshots of NeoCircuit results for these are shown in Figure 3-4(a) and Figure 3-4(b) respectively. The FOM for circuit with results in Figure 3-4(b) is 637m compared to 937m for that in Figure 3-4(a). This validates the claim that setting FOM as a design optimization objective improves the synthesis results.

Results

Goals

Name	Dir	Target	Default	Current
current	<	18m		6.5678m
S11low	<	-11		-14.5041
S11high	<	-11		-17.3648
S12high	<	-25		-26.9436
S12low	<	-25		-36.7286
S22high	<	-11		-16.1778
S22low	<	-11		-18.9647
S21low	>	17		17.0033
BW	<	3		2.5153
NFlow	<	2.8		2.4526
NFhigh	<	2.8		2.7643
FOM	max	700m		936.5386m

(a)

Results

Goals

Name	Dir	Target	Default	Current
current	<	18m		10.5349m
S11low	<	-11		-11.3301
S11high	<	-11		-12.6371
S12high	<	-25		-25.7658
S12low	<	-25		-34.6377
S22high	<	-11		-16.8049
S22low	<	-11		-19.8377
S21low	>	17		18.1165
BW	<	3		2.9882
NFlow	<	2.8		2.3389
NFhigh	<	2.8		2.703

(b)

Figure 3-4 Screenshots of NeoCircuit results showing the values of specifications for the best synthesis

4 Results

Three generations of the noise cancelling LNA have been designed for the 0.35 μm Jazz BiCMOS process. The LNA was sized, either using NeoCircuit or manually. The layout of the sized circuit was then manually drawn. The first and second generation designs were the initial forays into using NeoCircuit for wide-band LNA design and are discussed together below. They have been fabricated and their measured results are presented. The third generation design used the synthesis strategy described in the previous chapter. It has not yet been fabricated, so only simulation results (after layout extraction) are presented.

4.1 First and Second Generation LNA Designs

Design details for the first generation design are reported in [10]. Although it used NeoCircuit for synthesis, only a few device parameters were considered design variables due to the combination of a lack of designer experience with NeoCircuit, and a limited amount of design time till the tapeout deadline. Also, only S-parameters and NF were defined as goals. The device sizes for this design were related as shown in Figure 4-1 and described in [10] in order to get complete first stage noise cancellation. As the synthesis strat-

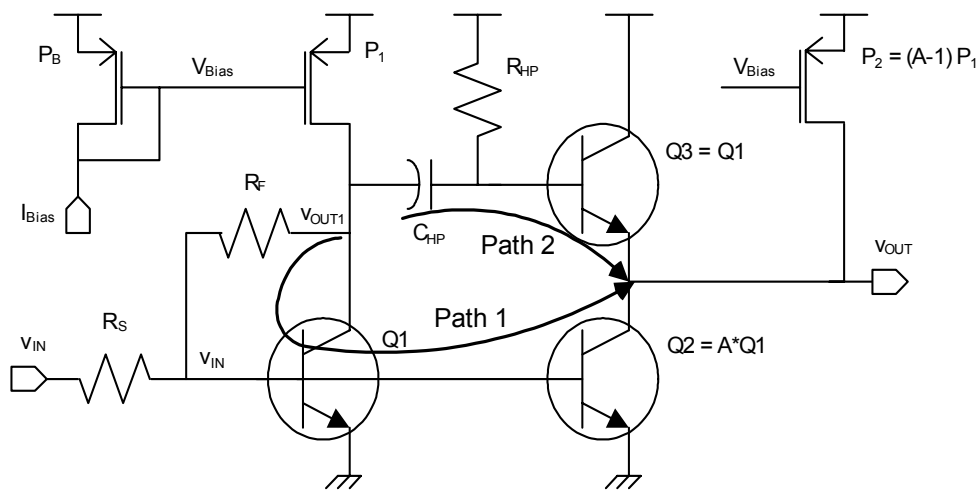


Figure 4-1 Gain matching requirement for maximum first stage noise cancelling

Variables Both Device Vars

Device				Design		
Dev	Prop	Expression	S	B	Variable	Value
CHighPass	c	CHP	<input type="checkbox"/>	<input type="checkbox"/>	Ibias1	[500u;25u;800u]
IStage1	idc	Ibias1	<input type="checkbox"/>	<input type="checkbox"/>	Ibias2	[3.2m;0.1m;5.0m]
IStage2	idc	Ibias2	<input type="checkbox"/>	<input type="checkbox"/>	QL1	[2u;1u;10u]
Qamp1	enl	QL1	<input type="checkbox"/>	<input type="checkbox"/>	QL2	[2u;1u;10u]
	mult	Qamp1Mult	<input type="checkbox"/>	<input type="checkbox"/>	pA	[5;2;9]
Qamp2	enl	DV(Qamp1,enl)	<input type="checkbox"/>	<input type="checkbox"/>	CHP	2p
	mult	pA	<input type="checkbox"/>	<input type="checkbox"/>	RHP	2K
Qsum	enl	QL2	<input type="checkbox"/>	<input type="checkbox"/>	pResF	(pA+1)*50
	mult	QsumMult	<input type="checkbox"/>	<input type="checkbox"/>	QsumMult	1
RHighPass	r	RHP	<input type="checkbox"/>	<input type="checkbox"/>	Qamp1Mult	1
Rf	r	pResF	<input type="checkbox"/>	<input type="checkbox"/>		

Match Schematic Propagate Delete

(a)

Goals

Name: NF_12G

Expression: noiseFigSparamRf(1200000000,EO(LNA_SP,NOISE,SP_NF))

Add Goal Type: lessthan Target Value: 2.4 Clear

RF sParamRf(sFreq,wsParam)

sParam	noiseFig	kFactor	gain	Parameter	Value
oscFreq	oscMag	lip3PAC	lip3Dist	sFreq	
pNoise	pscPNoise	convGain	harmVolt	wsParam	

Parameter Add Function

Name	Expression	Type	TargetValue
S11_12G	sParamRf(1200000000,EO(LNA_SP,SP_S11))	lessthan	-12
S11_21G	sParamRf(2100000000,EO(LNA_SP,SP_S11))	lessthan	-10
S22_12G	sParamRf(1200000000,EO(LNA_SP,SP_S22))	lessthan	-12 -10
S22_21G	sParamRf(2100000000,EO(LNA_SP,SP_S22))	lessthan	-10
S21_12G	sParamRf(1200000000,EO(LNA_SP,SP_S21))	greaterthan	15
S21_21G	sParamRf(2100000000,EO(LNA_SP,SP_S21))	greaterthan	14.5
NF_12G	noiseFigSparamRf(1200000000,EO(LNA_SP,NOISE,SP_NF))	lessthan	2.4
NF_21G	noiseFigSparamRf(2100000000,EO(LNA_SP,NOISE,SP_NF))	lessthan	2.6

octave Apply Delete

(b)

Figure 4-2 NeoCircuit variables and goals for the first generation design

egy described in the previous chapter had not yet been formulated, FOM was neither evaluated nor optimized during synthesis. These characteristics can be seen in the screen shots of the NeoCircuit variables and goals windows shown in Figure 4-2 (a) & (b). In this synthesis, the value of the feedback resistance, R_F , is set by an analytic constraint, $pResF = (pA + 1) * 50$. R_F is tied to the multiplicity of transistor Q_2 (Qamp2) through variable pA . This way, the multiplicity of Q_2 is changed with the value of R_F , so that the product of gain through R_F and Q_2 is one, which is assumed to be the gain through emitter-follower (EF). Thus this assumption related to complete first stage noise cancellation constrains the device sizes. When the fabricated circuit was tested, its measured NF rose above 3 dB within 3 dB gain bandwidth. Thus, the overall usable bandwidth of this LNA is limited by the NF and not by the gain bandwidth.

The goal of the second generation design was to solve this problem. Simulations of the first generation design showed that, for the circuit synthesized by the NeoCircuit, gains of the two paths, from the output of the first stage, V_{OUT1} , to the overall circuit output, V_{OUT} (labelled as “Path 1” and “Path 2” in Figure 4-1), were not equal. The attenuation factor analysis assumed an ideal emitter follower gain of 1. Thus, using this analysis in the NeoCircuit constraints led to a larger gain in “Path 2” compared to “Path 1”.

Complete noise cancellation of the first stage noise takes place when gains of these two paths are identical. To keep the NF below 3 dB over the entire 3 dB gain bandwidth, the second stage design focus was to match the gains in these two paths. Reduction in the difference between the gains can be achieved by reducing g_{m3} , the transconductance of transistor Q_3 . This, in turn can be achieved by increasing the current through P_2 , thereby robbing Q_3 of some current reducing its transconductance. It will not affect the biasing of the transistor Q_2 , as its biasing point is set by the DC voltage at node V_{IN} . Which means the current through second stage will not change. To understand how this changes the gain difference we will do a first order approximations of the gains through transistors Q_2 and Q_3 to understand their dependence on g_{m3} .

Gain of path “Path 1” is gain through R_F multiplied by the gain of the CE stage formed by transistor Q_2 with $1/g_{m3}$ in parallel with output 50Ω as load (output impedance of P_2 is assumed to be very large and therefore ignored). The gain of this CE stage will be:

$$\frac{-g_{m2} \cdot 50}{1 + 50 \cdot g_{m3}} \quad (4.1)$$

It can be easily seen that this will increase with a decrease in g_{m3} . As attenuation through R_F depends only on its value [10] it will remain constant. Thus the gain of “Path 1” will also increase with a decrease in g_{m3} . For “Path 2” the transistor Q_3 forms an emitter-follower whose gain is given as [13]:

$$\frac{1}{1 + \frac{r_{\pi} + R_s}{(\beta_o + 1) \cdot R_L}} \quad (4.2)$$

Here R_s which is source resistance will be zero, $\frac{r_{\pi}}{(\beta_o + 1)} \cong \frac{r_{\pi}}{\beta_o} = \frac{1}{g_{m3}}$ and $R_L \cong 50 \Omega$ since output impedance of Q_2 will be very large compared to 50Ω . Plugging these values in equation (4.2) simplifies the EF gain expression to:

$$\frac{1}{1 + \frac{1}{50 \cdot g_{m3}}} \quad (4.3)$$

Table 4.1: Measured LNA response

Specification	Value
S_{21} [dB]	17
S_{11} [dB]	< -8.9
S_{12} [dB]	< -25.3
S_{22} [dB]	< -6
BW [GHz]	2.6
NF [dB]	3
ICP [dBm]	-16.5
IIP3 [dBm]	-1.1
Power [mW]	32.5
Area [μm^2]	90x70
Technology	0.35 μm SiGe
FOM	0.46

This will decrease with g_{m3} . Thus, as g_{m3} is decreased, the gain of “Path 2” will decrease and the gain of “Path 1” increases, decreasing the difference between the gains. As output match depends on g_{m3} [10], only a small decrease in g_{m3} should be attempted.

Based on this analysis, size of P_2 was changed in order to increase its current. Manual tweaking of the circuit topology was done to arrive at a design free from the problem observed in the first generation. There was no other change made in the first generation topology to create the second generation. It was fabricated and following fabrication, it has been characterized. Its measured response, reported in the next section shows that NF is below 3 dB over the entire 3 dB gain bandwidth.

4.2 Measurement Results

Measurements were made using high-frequency rated coaxial cables paired with shielded Ground-Signal-Ground (GSG) probes on a Cascade Microtech Probe station. Results from the testing of the second-generation circuit are listed in Table 4.1. The numbers represent the worst case value of each specification

within the pass band of the amplifier, except for the S_{21} , IIP3 and ICP. S_{21} is the maximum value in the passband, which is itself set by the frequency where the gain equals $S_{21} - 3$ dB. ICP is measured at 1.5 GHz and IIP3 with tones at 1.5 GHz and 1.51 GHz. All measurements were taken with circuit biased at 13 mA from 2.5 V supply. Details concerning measurement setup and calibration can be found in [10].

4.2.1 S-Parameters

S-Parameters were measured using an Agilent E8364A Network Analyzer, following calibration of the high-frequency cables and probes. Measured S-Parameters plots are shown in Figure 4-3. S_{11} is shown

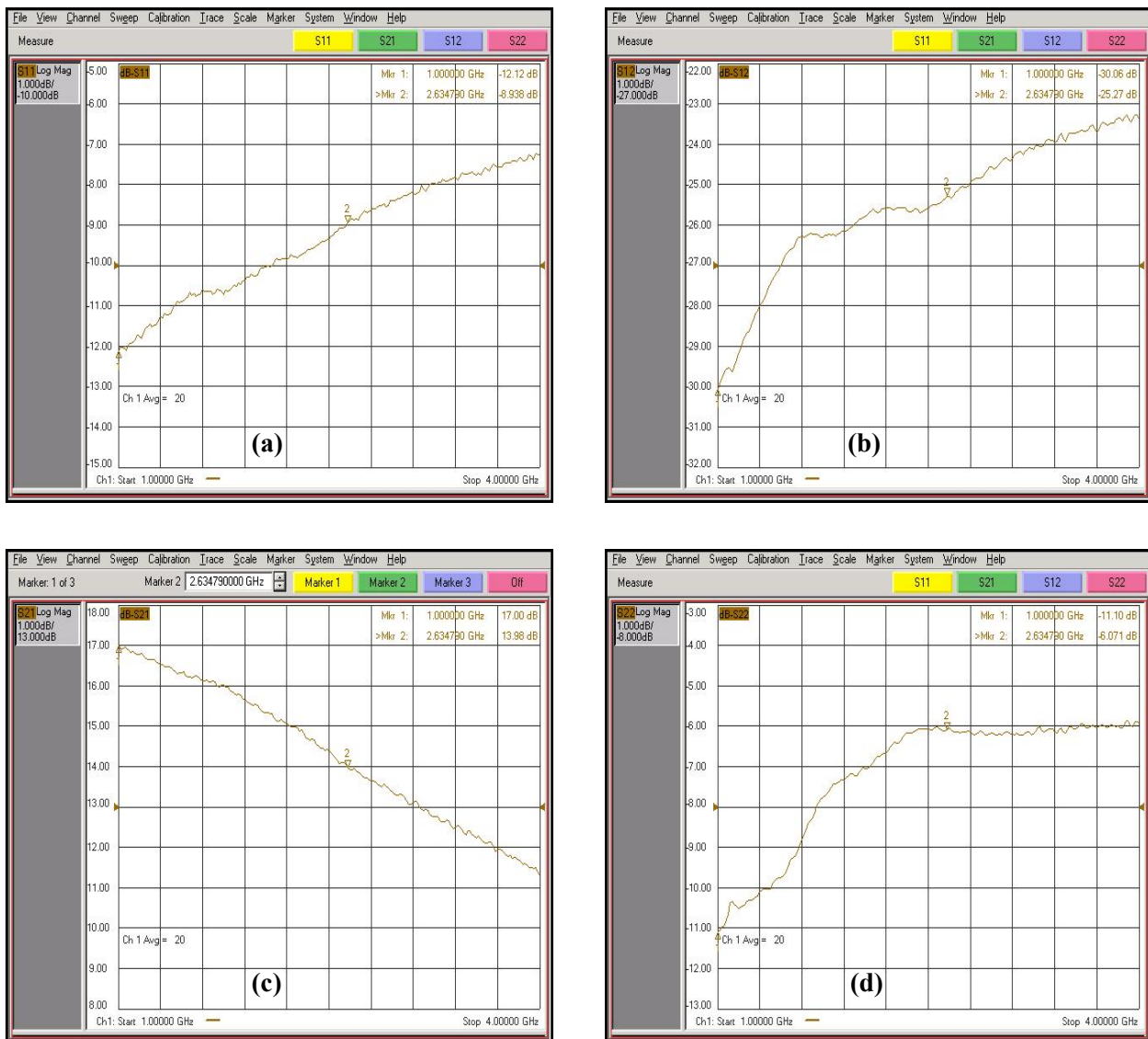


Figure 4-3 Measured S-Parameters

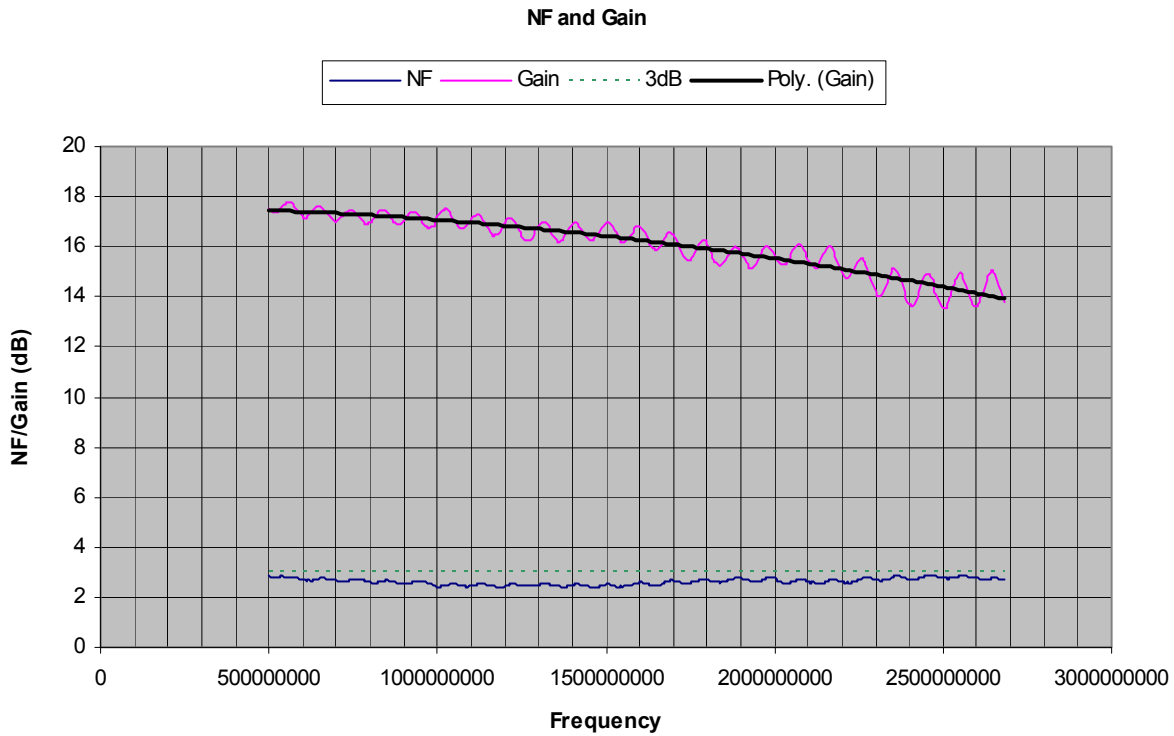


Figure 4-4 Noise-Figure measurement results

in Figure 4-3(a) S_{12} in Figure 4-3(b), S_{21} in Figure 4-3(c) and S_{22} in Figure 4-3(d). From markers in S_{21} plot, it can be seen that 3 dB gain bandwidth is 2.64GHz.

4.2.2 Noise Figure

The NF was measured using an Agilent E4440A Performance Spectrum Analyzer (PSA) and an external Agilent 346B noise source. The PSA has a built-in Noise-Figure personality which displays both gain and NF. As with the S-parameter measurement, the test fixture cables and probes were calibrated first. However, since the PSA is a scalar measurement device, only the loss amplitude can be removed during calibration. This is compared to vector calibration (available only in the NA) which takes both gain and phase into account. This results in the ripples seen in the measured gain as shown in Figure 4-4. The polynomial approximation of the measured gain has a maximum close to 17 dB, which is in agreement with S_{21} results obtained from the NA. In the figure the bottom-most solid plot is of NF which has been recorded

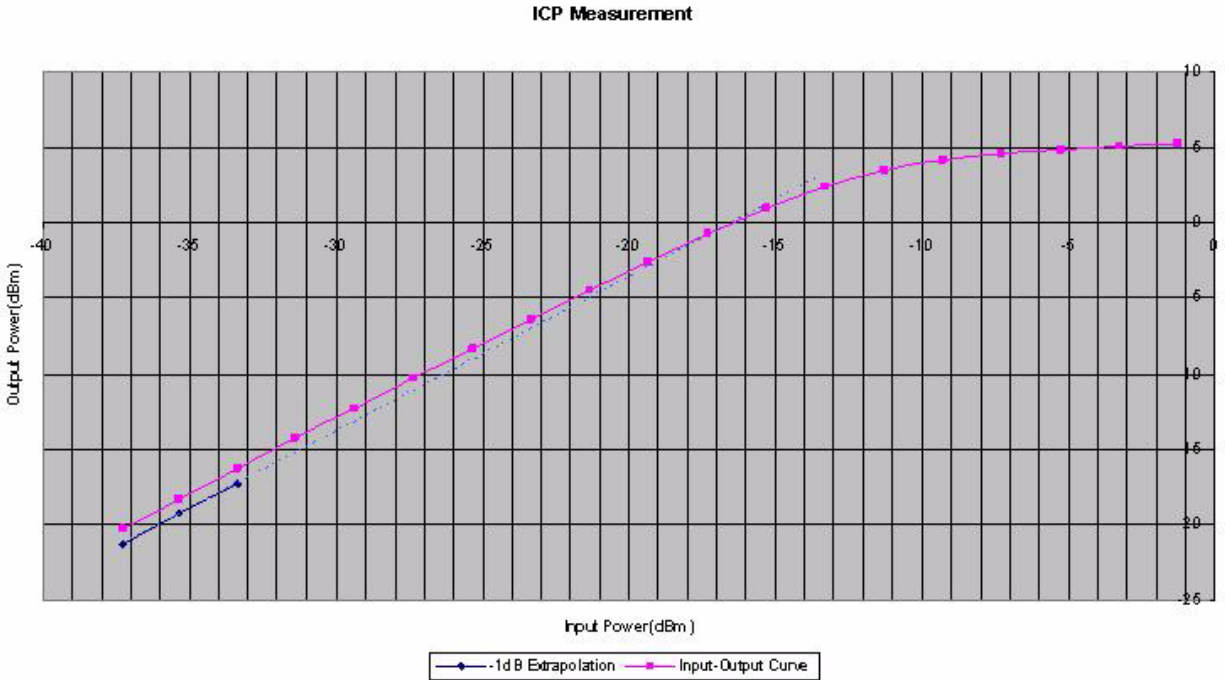


Figure 4-5 Compression point plot.

upto 2.7 GHz (beyond the -3 dB BW), and is shown against the -3 dB NF dotted line to indicate that the measured LNA NF is below 3 dB over the entire operating BW.

4.2.3 1 dB Input Compression Point (ICP)

ICP is a measure of linearity of the device and is defined as the input power that causes a 1 dB drop in the linear gain due to device saturation. The ICP was measured using the PSA with a 1.5 GHz test signal from an Agilent E8251 performance signal generator (PSG).

The input compression point plot is shown in Figure 4-5. The curve in the solid line is the measured gain compression characteristic of the amplifier. The dotted line, which is parallel to the characteristic at low input power, is 1 dB below it at low input power levels. The crossover point, defined as the 1 dB input compression point, is -16.5 dBm.

This plot also shows that when the input power is -37 dBm, the output power is -20 dBm, implying a gain of 17 dB. This input power is low enough to assume small signal nature of the circuit. Therefore, ICP

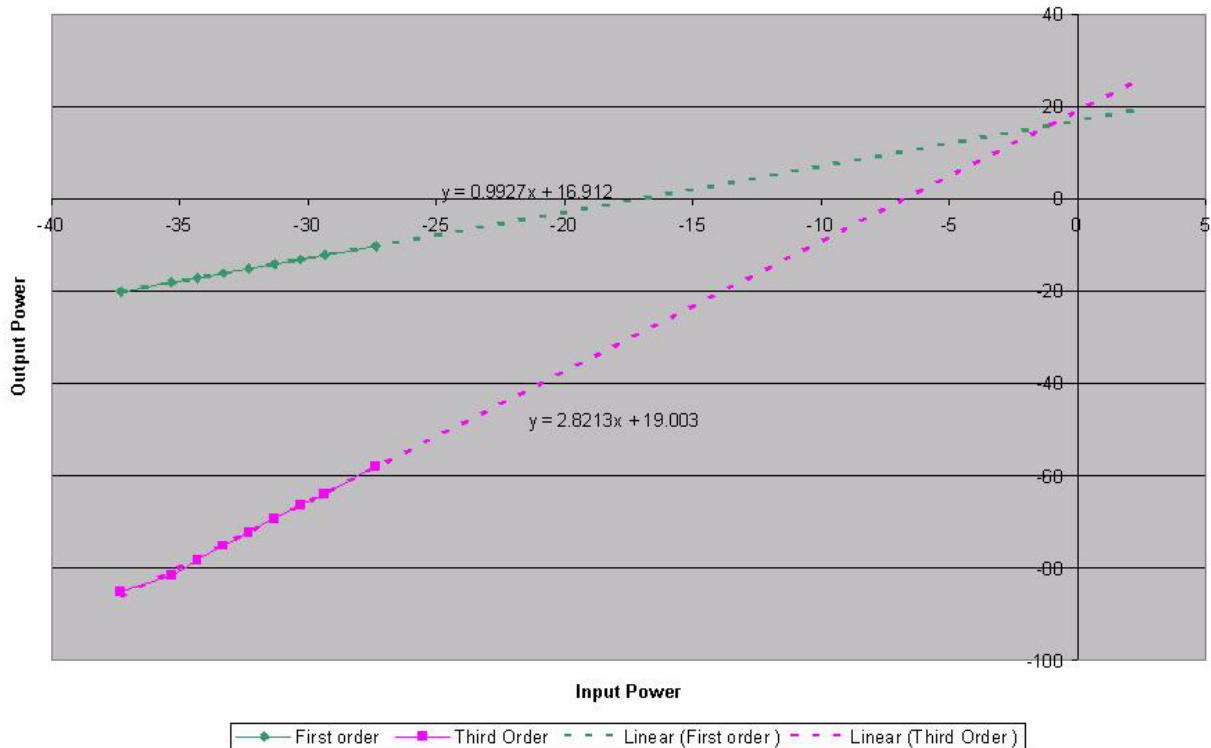


Figure 4-6 IIP3 Plot

measurement gives a small signal gain as 17 dB, which is in agreement with the S-Parameter and NF measurements.

4.2.4 Input-Referred Third Order Modulation Point (IIP3)

When a RF circuit is driven with a high-power RF signal, non-linearity causes inter-modulation of signals at different frequencies generating undesirable spurious signals. IIP3 is a very useful parameter to predict low-level intermodulation effects. It is measured by applying two input tones and is defined as the point at which the power in the third-order product and the fundamental tone intersect, when the amplifier is assumed to be linear.

The IIP3 on the LNA was measured using the PSA. Agilent E8251 and E8241 PSGs were used to generate the two input tones at 1.5 GHz and 1.51 GHz. The IIP3 plot is shown in Figure 4-6. The solid section of the plots connects measured points and the dotted section is the linear extrapolation. The top line plot is of the output power at the fundamental frequency and bottom line plot is of the output power in the third-

order intermodulation product vs. power at input frequency. The equation of the first order extrapolated line is $y = 0.9927x + 16.912$ and of the third order extrapolated line is $y = 2.8213x + 19.003$. Solving for the crossover point between these lines leads to the IIP3, which occurred at an input power of -1.14 dBm. Ideally slope of the first order line should be 1, because output power in the fundamental tone should increase by the same amount as at the input. The measured slope is 0.9927. Gain is given by y-intercept of the line, which is 16.91 dB and is in agreement with all previous measurements. Since power in the third-order modulation product increases by three times the amount of increase in the input power, ideally the slope of the extrapolated line for the third-order intermodulation should have slope of 3. The measured slope of 2.83, is very close.

4.3 Second Generation Design Result Summary

The simulation performance of the extracted layout and the measured LNA are summarized in Table 4.2. It can be seen that the measurement results match the extracted simulation results

Table 4.2: Comparison of Extraction and Measurement Results of Second Generation LNA

Specifications	Extraction	Measurement
S ₂₁ [dB]	18	17
S ₁₁ [dB]	-8	< -8.9
S ₁₂ [dB]	-23.5	< -25.3
S ₂₂ [dB]	-6.7	< -6
BW [GHz]	2.75	2.6
NF [dB]	2.7	3
ICP [dBm]	-14.63	-16.5
IIP3 [dBm]	-3.2	-1.1
Power [mW]	29	32.5
FOM	0.63	0.46

Figure 4-7 compares the measured FOM for the second generation LNA with that of other wide-band LNA papers in the literature. The FOM data is plotted against the feature size of the process in which

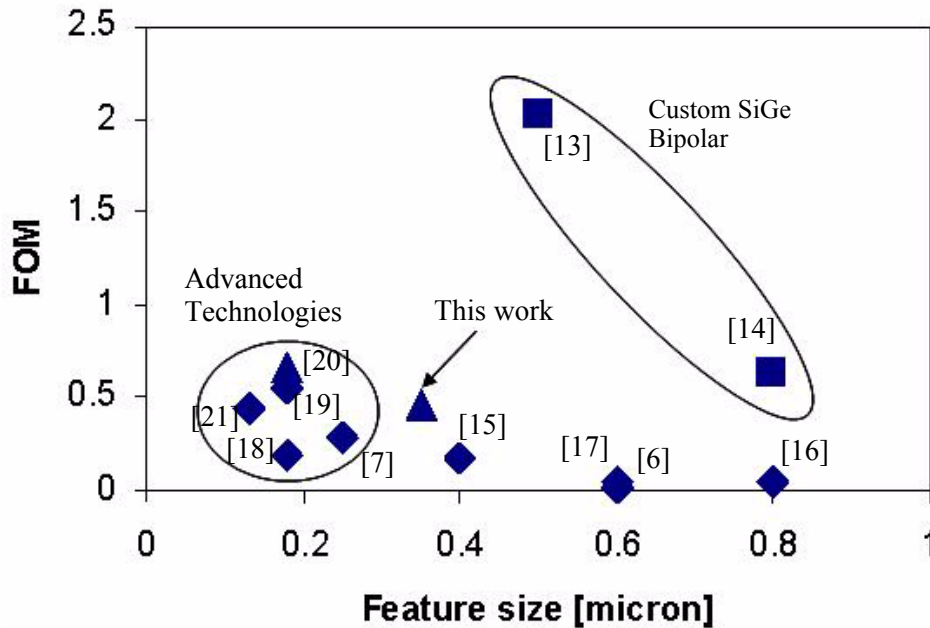


Figure 4-7 Wide-band LNA Figure of Merit vs. Lithographic feature size they are fabricated (due to lack of f_T data). The higher the figure of merit, the better the design. The marker shape indicates the type of process (square for custom SiGe bipolar technologies without CMOS integration, triangle for foundry SiGe BiCMOS technologies and diamond for foundry CMOS technologies). Our fabricated LNA has a higher FOM than all the designs other than those from more advanced foundry technologies or from the custom bipolar processes. Moreover, this 0.35 μm BiCMOS LNA is at least equal in performance to all the 0.13 and 0.18 μm CMOS LNAs. This shows the benefit of combining a scalable noise cancelling topology with SiGe BiCMOS technologies.

4.4 Third Generation Design

Even though the first generation synthesis made use of the NeoCircuit, it did so in a very restricted way. Since it used an analysis equation that related the device sizes in the schematic for first stage noise cancellation, NeoCircuit couldn't bias and size the schematic freely. Moreover, there was no constraint on the power. So, while the manually modified second generation circuit met the gain, BW and NF requirements, and showed the potential for the noise-cancellation topology, it is not an appropriate design for multi-band radios described in Chapter 1. For example, like the first generation design, it has no power constraint.

Therefore, the noise cancellation in the second generation design was accomplished primarily by burning power. One approach to preventing free use of power would have been to add a constraint on the power, or a minimization objective to the power specification. However, this had not been done in the first generation design.

In the third generation design, circuit power consumption is captured in the FOM expression, which is optimized. By using an aggregate of several circuit specifications for the optimization objective, the synthesis can trade off between the objectives, ensuring that the constraints are met, and power is minimized.

To understand the difference between the second and third generation designs, we need to consider the relationship between circuit power and noise cancellation. The impedance looking into the emitter of the transistor Q_3 determines the output impedance, as output impedances of Q_2 and P_2 are very large and thus, can be ignored. This impedance (at the emitter of Q_3) depends on its transconductance g_{m3} . Therefore, g_{m3} is set by the output match condition. This sets the gain of the EF amplifier (“Path 2” in Figure 1-1) (equation (4.3)). The gain of “Path 1” is the gain through Q_2 divided by the attenuation through R_F (which is $(1 + R_F/R_S)$). To increase this gain to that of the “Path 2”, either gain through Q_2 should be increased or attenuation through R_F should be decreased. To reduce the attenuation, R_F will have to be reduced, thereby reducing the gain of the first stage (equation (2.1)). Since the overall LNA gain comes primarily from the first stage, this cannot be done. The other alternative, increasing gain through Q_2 (given by equation (4.1)), requires a lot of current. This increase in current increases the noise generated by the CE stage, which eventually becomes more important than the reduction in the noise due to noise cancellation [7]. Therefore, complete first stage noise cancellation condition requires a lot of power and doesn’t necessarily lead to the best overall NF. This condition was removed for the third generation design.

The overall required gain is shared by the first CE stage (with resistive feedback) and the second CE stage (Q_2). The gain of the first CE stage is $\sim -g_{m1} \cdot R_F$ (from equation (2.1)) and that of through Q_2 is given by equation (4.1). Since $R_F \gg 50\Omega$, investing current into Q_1 rather than Q_2 in order to improve g_{m1} instead of g_{m2} will lead to the most power efficient way to achieve gain. On the other hand, the gain

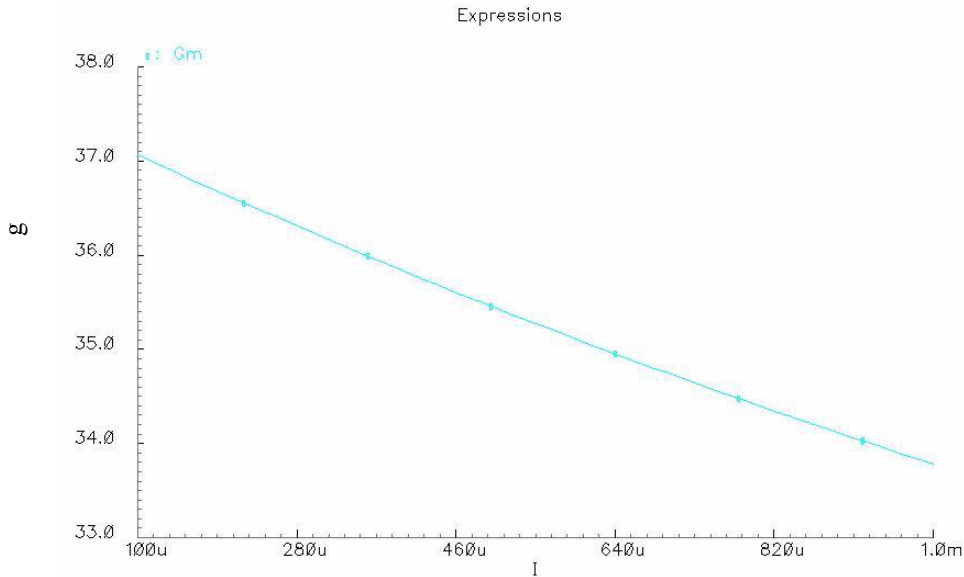


Figure 4-8 g_m/I_c vs. I_c for HBT

through Q_2 needs to be close enough to the gain through the emitter follower to achieve some amount of noise cancellation.

Figure 4-8 shows the simulation plot of the transconductance of a HBT per unit biasing current vs. different values of the biasing currents. Ideally it should be a constant as $g_m = I_C/V_T$. But, due to second order effects we get more g_m per unit biasing current when HBT is biased at lower current. Thus, one would like to bias transistors at lower current and use more transistors in parallel to achieve the same net transconductance. However, this increases device parasitics at the input which will affect the input matching and thus, S_{21} , as less of the input signal will get transmitted into the circuit to be amplified.

For optimum power efficiency to get the desired gain and NF, the circuit has to be designed in accordance with the trade-offs discussed in the previous three paragraphs. NeoCircuit was used to locate this optimum. Unlike the first generation design, more device parameters were made variables to give NeoCircuit more freedom while sizing and biasing the circuit. In the next section NeoCircuit synthesis results are presented for the third generation LNA. In the section following the next we will analyze the synthesis results to validate our trade-off hypothesis presented.

Name	Expression	Type	Value	Weight
current	magnitude(EO(DC,DCOPDC_LNA_CORE_V_P))	lessthan	18m	1
S11low	sParamRf(1e9,EO(SP,SP_S11))	lessthan	-11	1
S11high	sParamRf(3e9,EO(SP,SP_S11))	lessthan	-11	1
S12high	sParamRf(3e9,EO(SP,SP_S12))	lessthan	-25	1
S12low	sParamRf(1e9,EO(SP,SP_S12))	lessthan	-25	1
S22high	sParamRf(3e9,EO(SP,SP_S22))	lessthan	-11	1
S22low	sParamRf(1e9,EO(SP,SP_S22))	lessthan	-11	1
S21low	sParamRf(1e9,EO(SP,SP_S21))	greaterth	17	1
BW	sParamRf(1e9,EO(SP,SP_S21))-sParamRf(3e9,EO(SP,SP_S21))	lessthan	3	1
NFlow	noiseFigSparamRf(1e9,EO(SP,SPNOISE_SP_NF))	lessthan	2.8	1
NFhigh	noiseFigSparamRf(3e9,EO(SP,SPNOISE_SP_NF))	lessthan	2.8	1
FOM	sParamRf(1e9,EO(SP,SP_S21))/(noiseFigSparamRf(3e9,EO(SP,SPNOISE_SP_NF))*magnitu	maximize	0.4	1

Figure 4-9 NeoCircuit goals window with equal weights on all goals

4.4.1 NeoCircuit Synthesis Results

The synthesis strategy presented in Chapter 3 was used for the third generation design. A target gain BW of 3 GHz was used during synthesis. This allows for enough over design to compensate for BW reduction due to interconnect parasitics which are not considered during the circuit simulation used for synthesis. Following synthesis an extraction-based simulation will be used to ensure that the BW is greater than 2.5 GHz. The supply voltage used was 2.5 volts. The variables and simulation environment were initialized as outlined in Chapter 3. The goals, shown in Figure 4-9, were set with target values in accordance with the LNA specifications (Section 1.4). The FOM (Section 1.5) was marked as a parameter to be maximized with the target value being the second generation measured LNA FOM.

As described in the synthesis strategy (Chapter 3), the first NeoCircuit run used a weight of 1 on all the goals as shown in Figure 4-9. We will refer to this as the third generation (Initial). The synthesis results are shown in Figure 4-10 (a). The column labelled “Current” shows the values for the corresponding goals achieved. Comparing the values in this column with those in the “Target” column, indicates that the targets are reasonable for this topology and process. “NFhigh” (which is NF value at higher frequency) is narrowly missed, and the remaining goals are all met.

So, in the second run the weights on some of the goals are altered, as shown in Figure 4-11. A higher weight is used for “NFhigh”. Since BW, “NFlow” and FOM are critical goals, their weights are also

Results

Goals

Name	Dir	Target	Default	Current
current	<	18m	18m	7.6312m
S11low	<	-11	-11	-13.2318
S11high	<	-11	-11	-16.8518
S12high	<	-25	-25	-26.6826
S12low	<	-25	-25	-36.194
S22high	<	-11	-11	-17.0616
S22low	<	-11	-11	-20.3599
S21low	>	17	17	17.5145
BW	<	3	3	2.7649
NFlow	<	2.8	2.8	2.4862
NFhigh	<	2.8	2.8	2.8405
FOM	max	400m	400m	807.9843m

(a)

Results

Goals

Name	Dir	Target	Default	Current
current	<	18m	18m	6.5678m
S11low	<	-11	-11	-14.5041
S11high	<	-11	-11	-17.3648
S12high	<	-25	-25	-26.9436
S12low	<	-25	-25	-36.7286
S22high	<	-11	-11	-16.1778
S22low	<	-11	-11	-18.9647
S21low	>	17	17	17.0033
BW	<	3	3	2.5153
NFlow	<	2.8	2.8	2.4526
NFhigh	<	2.8	2.8	2.7643
FOM	max	700m	700m	936.5386m

(b)

Figure 4-10 NeoCircuit Synthesis results for the (a) first NeoCircuit run with equal weights (3rd generation (Initial) design) and (b) second run with modified weights (3rd generation (Final) design).

increased. Also, the target value of altered FOM was also changed to the FOM achieved in the first NeoCircuit synthesis run. The second synthesis run results are shown in Figure 4-10(b). We will refer to this design as the third generation (Final). This time all the goals were met and the FOM achieved is about is $\sim 2.5x$ better than the second generation design.

4.4.2 Analysis of the 3rd Generation Synthesized LNAs

If incomplete cancellation of the noise from the first stage improves the overall circuit NF, as claimed above, then there should be two differences in the third generation circuits compared to the second generation one. First, there should be a difference in the gains between the two noise cancellation paths, sec-

Name	Expression	Type	Value	Weight
current	magnitude(EO(DC,DCOPDC_LNA_CORE_V_P))	lessthan	18m	1
S11low	sParamRf(1e9,EO(SP,SP_S11))	lessthan	-11	1
S11high	sParamRf(3e9,EO(SP,SP_S11))	lessthan	-11	1
S12high	sParamRf(3e9,EO(SP,SP_S12))	lessthan	-25	1
S12low	sParamRf(1e9,EO(SP,SP_S12))	lessthan	-25	1
S22high	sParamRf(3e9,EO(SP,SP_S22))	lessthan	-11	1
S22low	sParamRf(1e9,EO(SP,SP_S22))	lessthan	-11	1
S21low	sParamRf(1e9,EO(SP,SP_S21))	greaterth	17	1
BW	sParamRf(1e9,EO(SP,SP_S21))-sParamRf(3e9,EO(SP,SP_S21))	lessthan	3	2
NFlow	noiseFigSparamRf(1e9,EO(SP,SPNOISE_SP_NF))	lessthan	2.8	3
NFhigh	noiseFigSparamRf(3e9,EO(SP,SPNOISE_SP_NF))	lessthan	2.8	3
FOM	sParamRf(1e9,EO(SP,SP_S21))/(noiseFigSparamRf(3e9,EO(SP,SPNOISE_SP_NF))*magnitu	maximize	0.7	3

Figure 4-11 NeoCircuit goals window with weights on some goals changed

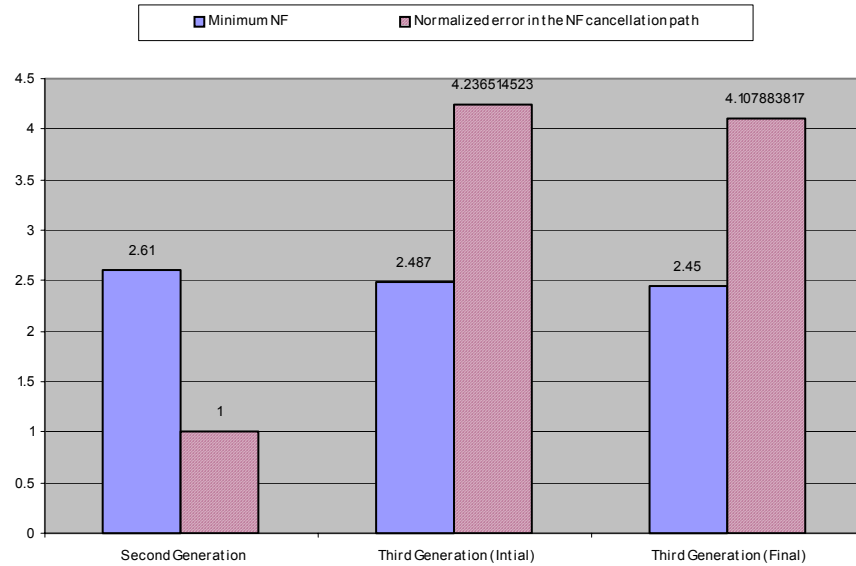


Figure 4-12 Comparing minimum NF and normalized error in first stage noise cancellation across three the designs

ond, the third generation designs should have should have better NF. Figure 4-12 compares magnitude of the difference in the gain between “Path 1” and “Path 2” (normalized to that for the second generation design) and the minimum NF across the three designs. It can be seen that the minimum NF has improved, even though the error in the noise cancellation path has increased for the third generation designs. The error in the noise cancellation paths increased between the third generation (Initial) and the second generation designs while the NF decreased. Also, going from the third generation (Initial) to the third generation (Final) designs, both the error in gain matching between the noise cancellation paths and the NF decreased. This means that there is an optimal error in the noise cancellation for best minimum overall NF.

Gains provided by the first CE stage (with resistive feedback) and the second CE stage (Q_2) for the three designs are normalized to the value for the second generation and compared in Figure 4-13. NeoCircuit synthesized circuits, compared to hand-designed second generation have more gain for the first CE stage and less gain through Q_2 . Gains for the third generation (Final) are slightly less than the gains for the third generation (Initial), as the overall gain was reduced by the NeoCircuit to just meet the target value.

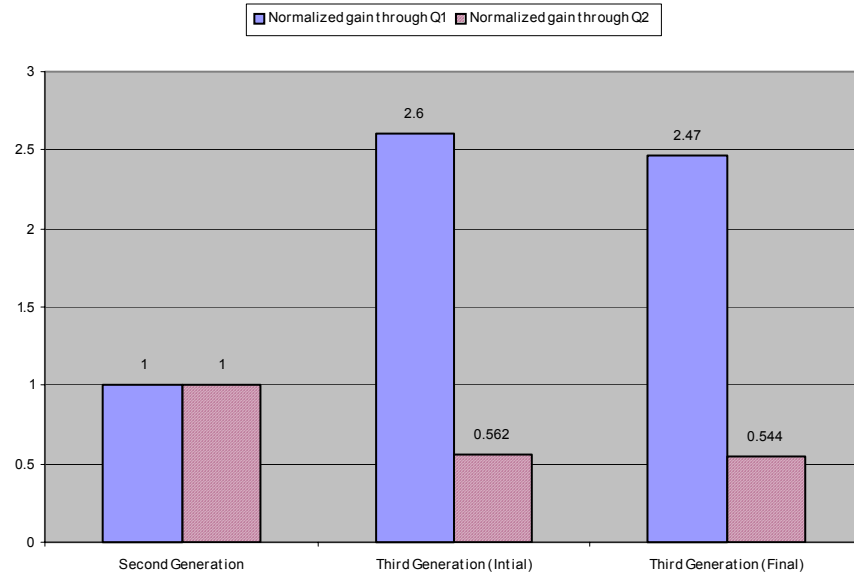


Figure 4-13 Comparison of gain from transistor Q_1 and Q_2 across the three designs.

Also, the normalized total g_m of transistors Q_1 and Q_2 are compared in Figure 4-14. Since gain is directly proportional to g_m , this plot confirms the gain distribution hypothesis.

NeoCircuit biased the HBTs for the third generation designs at lower currents as compared to the second generation hand design thus improving the g_m/I_C . This is shown in Figure 4-15 which plots the normalized collector current I_C and g_m/I_C for the transistor Q_1 across the three designs.

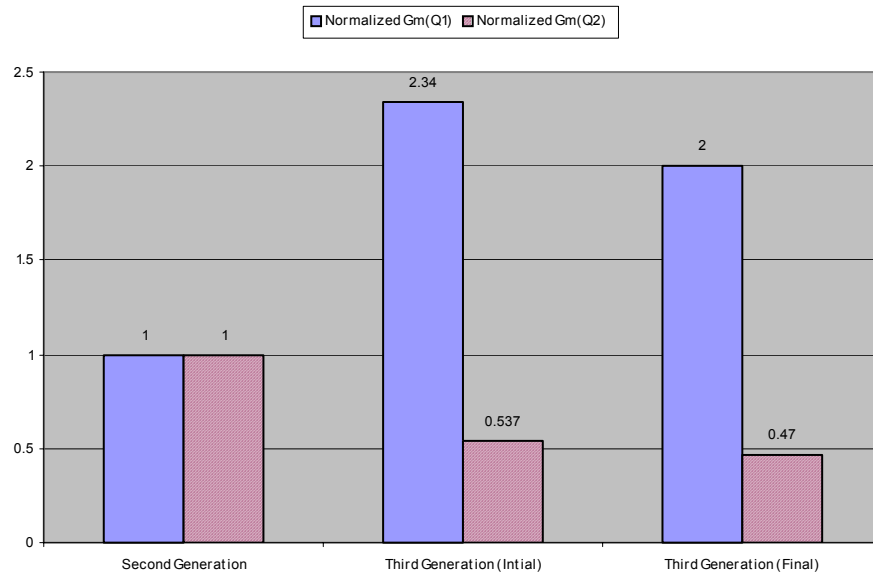


Figure 4-14 Normalized transconductance of transistors Q_1 and Q_2 across the three designs

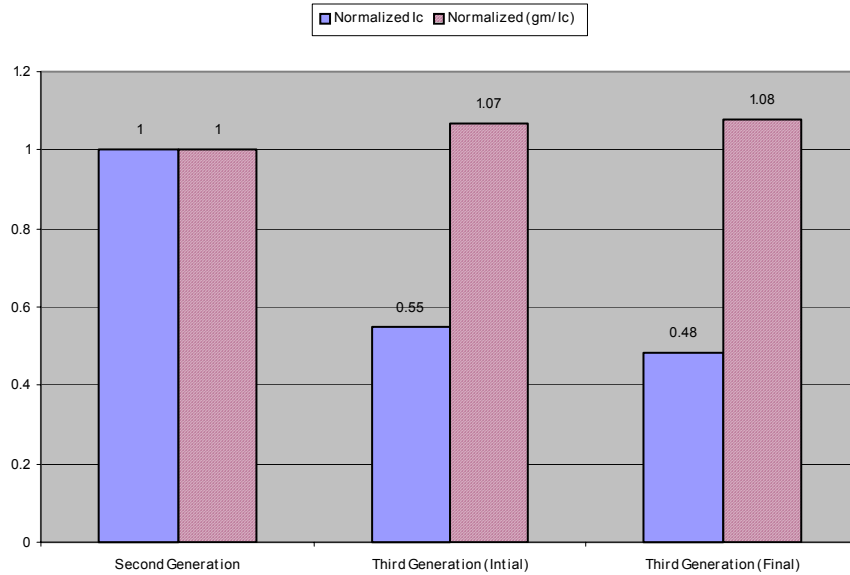


Figure 4-15 Normalized collector current I_C and (g_m/I_C) for transistor Q_1 across the three designs.

Thus, analysis of the synthesized results shows that NeoCircuit synthesizes improved the LNA design by optimizing in the directions suggested at the beginning of this section.

4.4.3 Simulation for Extracted Circuits

As the third generation design has not yet been fabricated, the extraction simulation results are shown in Table 4.3 to allow comparison with the second generation extracted and measured datasheet

Table 4.3: Extraction Results

Specifications	Third Generation
S_{21} [dB]	17.21
S_{11} [dB]	-11.2
S_{12} [dB]	-27.21
S_{22} [dB]	-14
BW [GHz]	2.88
NF [dB]	2.85
ICP [dBm]	-18.4
IIP3 [dBm]	-7.4
Power [mW]	16.55
Area [μm^2]	118x78
FOM	1.05

shown in Table 4.2. The extracted circuit includes interconnect parasitics. This together with the quality of the device models available in the Jazz design kit lends credibility to the potential for achieving these targets when the design is fabricated. If we derate the FOM obtained from extracted circuit simulation by the ratio of the measured to extracted FOM in Table 4.2, the resulting FOM will still be higher than all the advanced CMOS LNAs shown in Figure 4-7.

5 Conclusion and Future Work

An LNA design for application in multi-band wireless transceivers has been presented. The desire for monolithic integration of the RF front end with CMOS baseband processing led to the choice of the wide-band LNA (compared to multiple parallel narrow-band LNAs), and SiGe BiCMOS technology (over CMOS). Selected specifications and RF issues, such as impedance matching and low NF over wide band of frequency, drove to the choice of wide-band noise cancellation topology [7].

Three generations of the selected topology have been designed in the Jazz 0.35 μm BiCMOS process. The first two generations of these have been fabricated and characterized. A third generation design was automatically synthesized, and its physical design completed.

The best fabricated LNA has measured gain of 17 dB and a bandwidth of 2.6 GHz. The NF is less than 3 dB over the LNA bandwidth, with minimum value of 2.4 dB. It draws 13mA current from a 2.5 V supply. Simulation, following layout extraction, of the third generation LNA suggests that a gain of 17.21 dB and bandwidth as 2.9 GHz is achievable. The worst NF over this band is 2.85 dB. These were obtained by burning 6.62 mA current from a 2.5 V supply. This design shows a FOM improvement of $\sim 2x$ compared to the extracted simulation results of the second generation design, showing the effectiveness of NeoCircuit. Furthermore, if we derate the extracted simulation results of this design by what was see for the second generation, we anticipate being able to measure a circuit which outperforms all the CMOS wide-band LNAs in the literature.

Future work includes fabrication and testing of this LNA and comparing it with previous generations. Additionally, narrow-band LNA topologies that have tunable matching networks will be explored for use in multi-band radio front ends.

References

- [1]D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE JSSC*, SC-32(5), May 1997, p. 745.
- [2]R. Magoon *et. al.*, "A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCOs and fractional-n synthesizer," *IEEE JSSC*, SC(37)12, Dec. 2002, pp. 1710 - 1720.
- [3]Adiseno, M. Ismail and Hakan Olsson, "A Wide-Band RF Front-End for Multiband Multistandard High-Linearity Low-IF Wireless Receivers," *IEEE JSSC*, SC(37)9, Sept. 2002, pp. 1162-1168.
- [4]C.-S. Wang, W.-C. Li and C.-K. Wang, "A Multi-band Multi-standard RF Front-end for IEEE 802.16a and IEEE 802.11a/b/g application," *ISCAS 2005*.
- [5]D. Ramachandran, A. Oz, V. K. Saraf, G. K. Fedder and T. Mukherjee, "MEMS-Enabled Reconfigurable VCO and RF Filter," *Proc. IEEE RFIC Symp.*, June 6-8, 2004, p. 251.
- [6]B. M. Ballweber, R. Gupta, and D. J. Allstot, "A Fully Integrated 0.5–5.5-GHz CMOS Distributed Amplifier," *IEEE JSSC*, SC-35(2), February 2000, pp. 231-239.
- [7]F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE JSSC*, SC-39(2), Feb. 2004, pp. 275-282.
- [8]D. L. Hamee, *et. al.* "Current status and future trends of SiGe BiCMOS technology," *IEEE Transactions on Electron Devices*, vol. 48, no. 11, Nov. 2001, pp. 2575-2594.
- [9]K. W. Kobayashi, A. K. Oki, L.T. Tran, and D. C. Streit, "Ultra-low dc power GaAs HBT S- and C-band low noise amplifiers for portable wireless applications," *IEEE MTT*, vol. 43, no. 12, Dec. 1995, pp. 3055-3061.
- [10]M. Sperling, "SiGe BiCMOS RF Circuit Design: A Wideband LNA Example," Masters Thesis, Carnegie Mellon University, August 2003.
- [11]B. Razavi, *RF Microelectronics*, Prentice Hall, pp 20.
- [12]S. Narayanan, H. Poon, "An analysis of distortion in bipolar transistors using integral charge control model and Volterra series," *IEEE Transactions on Circuits and Systems*, vol. 20, no. 4, Jul. 1973, pp. 341-351.
- [13]P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, third edition, pp.211.
- [14]H. Knapp, *et. al.*, "15 GHz Wideband Amplifier with 2.8 dB Noise Figure in SiGe Bipolar Technology," *RFIC 2001*, pp. 287-290.

- [15]H. Schumacher, *et. al.*, "A 3 V supply voltage, DC-18 GHz SiGe HBT wideband amplifier," *BCTM*, 1995, pp. 190-193
- [16]J. Janssens, M. Steyaert and H. Miyakawa, "A 2.7 Volts CMOS Broadband Low Noise Amplifier," *1997 Symposium on VLSI Circuits*, pp. 87-88.
- [17] P. I. Sullivan, B. A. Xavier and W. H. Ku, "An integrated CMOS distributed amplifier using packaging inductance," *MTT*, vol. 45, no. 10, Oct. 1997, pp. 1969-1975.
- [18]H. Ahn. and D. J. Allstot, "A 0.5-8.5-GHz fully differential CMOS distributed amplifier," *IEEE JSSC*, SC(37)8, Aug. 2002, pp. 985-993.
- [19]S. Andersson, C. Svensson, and O. Drugget, "Wideband LNA for a Multistandard Wireless Receiver in 0.18um CMOS," *ESSCIRC*, 2003, pp. 655-658.
- [20]R.-C. Liu, K.-L. Deng and H. Wang, "A 0.6-22-GHz Broadband CMOS Distributed Amplifier," *RFIC 2003*, pp. 103-106.
- [21]Q. He and M. Feng, "Low-power, high-gain, and high-linearity SiGe BiCMOS wide-band low-noise amplifier," *IEEE JSSC*, SC(39)6, June 2000, pp. 956-959.
- [22]R. Gharpurey, "A Broadband Low-Noise Front-End Amplifier for Ultra Wideband in 0.13um CMOS," *CICC 2004*, pp. 605-608.

Appendix: Significance of 3 dB Noise Figure

Input and output SNR is denoted by:

$$SNR_{in} = \frac{S_{in}}{N_{in}} \quad SNR_{out} = \frac{S_{out}}{N_{out}} \quad (\text{A.1})$$

where S denotes signal power and N denotes noise power. If gain of amplifier is denoted by G and noise added by it as N_{added} then:

$$S_{out} = G \cdot S_{in} \quad (\text{A.2})$$

$$N_{out} = G \cdot N_{in} + N_{added} \quad (\text{A.3})$$

$$SNR_{out} = \frac{G \cdot S_{in}}{G \cdot N_{in} + N_{added}} \quad (\text{A.4})$$

NF is defined as:

$$NF = 10 \cdot \log_{10} \left(\frac{SNR_{in}}{SNR_{out}} \right) \quad (\text{A.5})$$

For given expressions of SNR_{in} and SNR_{out} it becomes:

$$\begin{aligned} NF &= 10 \cdot \log_{10} \left(\frac{S_{in}/N_{in}}{(G \cdot S_{in})/(G \cdot N_{in} + N_{added})} \right) \\ &= 10 \cdot \log_{10} \left(\frac{G \cdot N_{in} + N_{added}}{G \cdot N_{in}} \right) \end{aligned} \quad (\text{A.6})$$

For NF of 3 dB:

$$3 = 10 \cdot \log_{10} \left(\frac{G \cdot N_{in} + N_{added}}{G \cdot N_{in}} \right) \quad (\text{A.7})$$

which, on simplification gives:

$$N_{added} = G \cdot N_{in} \quad (\text{A.8})$$

Thus, for NF of 3 dB, the noise power added by the system is same as the noise at the input amplified by the amplifier gain.