Design of a Chopper Stabilized Variable Capacitive Sense Amplifier for a MEMS Probe-Based Data Storage System

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Table of Contents

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Abstract

Applications of MEMS variable capacitive sensors are introduced. The design trade-offs of variable capacitive sense amplifiers are discussed and a chopper stabilized variable capacitive sense amplifier topology is introduced. The chopper stabilized topology has the advantage of not being sensitive to 1/f noise, charge injection noise, kT/C noise, and dc offsets. This circuit was designed to meet the requirements of a MEMS probe-based data storage system. These requirements include a signal-to-noise ratio of greater than 30dB and an incremental power dissipation of under 200μW per sense amplifier. The circuit was designed in HP .5 μm CMOS and laid out using NeoCell, an automated analog layout tool. The layout was extracted and the system was simulated to demonstrate linear operation and a signal-to-noise ratio exceeding 30dB.

Chapter 1: Introduction

1.1 MEMS Variable Capacitor Sensor Applications

Micro-electro-mechanical variable capacitive sensors are finding increasing application to micro-electro-mechanical systems (MEMS). These sensors are employed in accelerometers, inertial navigation systems, control systems for MEMS actuators, pressure sensors, acoustic sensors, and data storage systems, along with a host of other applications. Variable capacitive (ΔC) sensors are an important field of research due to their generality of application to a large variety of MEMS systems. ΔC sensors have a number of advantages over other MEMS sensors. These include scalability, small size, the potential for high levels of integration with microelectronics, symmetry of the sense - actuation system and many others [1][2].

CMOS MEMS fabrication processing allows variable capacitors, sensing circuitry, actuators and processing circuitry to be fabricated in close proximity. This property yields systems with a very high level of integration, which allows these systems to be space efficient and cost effective. The high level of integration allows the sensor system to take advantage of process scaling.

Variable capacitive sensors consist of a variable capacitor and variable capacitive sense amplifier. The variable capacitor often consists of a released MEMS conducting structure with a controllable displacement with reference to a fixed conductive structure. In some cases the fixed structure is not truly static and can move at low frequencies. The performance of the variable capacitive sense amplifier is critical to the performance of the overall sensor. This report deals with the design of a variable capacitive sense amplifier for application to a MEMS variable capacitive sensor. The amplifier discussed in this paper is for application to a continuous-time system.

Continuous-time baseband capacitive sensing circuits are not ideal because they have major limitations due to dc offsets and 1/f noise in the amplifier stages. Many ΔC sensors make use of switched capacitor circuits. The noises produced by switched capacitor circuits often becomes the dominant limitation of such systems [2]. Switched capacitor circuits exhibit noises such as kT/C noise and charge injection noise. Autozeroing systems which make use of correlated double sampling turn out to be a better solution for discrete time systems. However, they are not as well suited for continuous time systems due to their aliasing of noise when sampling [3].

The approach taken in this report is to design a modulated ΔC sensor system using the principle of chopper stabilization. This system has the advantage of not being sensitive to 1/f noise, charge injection noise, kT/C noise, and dc offsets, while not aliasing noise by sampling. For a continuous time application, chopper stabilization offers better noise performance than continuous-time baseband, switched capacitor, and autozeroing systems.

1.2 Probe-Based Data Storage Project

The specific application that the discussed Δ Capacitive sensor circuit was designed for is a probe-based magnetic data storage system. This system is discussed in detail in "Single Chip Computers with MEMS-Based Magnetic Memory" [4]. In this system, an array of probe tips along with their circuitry sit on a die that is bonded over another die containing a sheet of magnetic media. A diagram of the mechanical system is shown in figure1.1 [4].
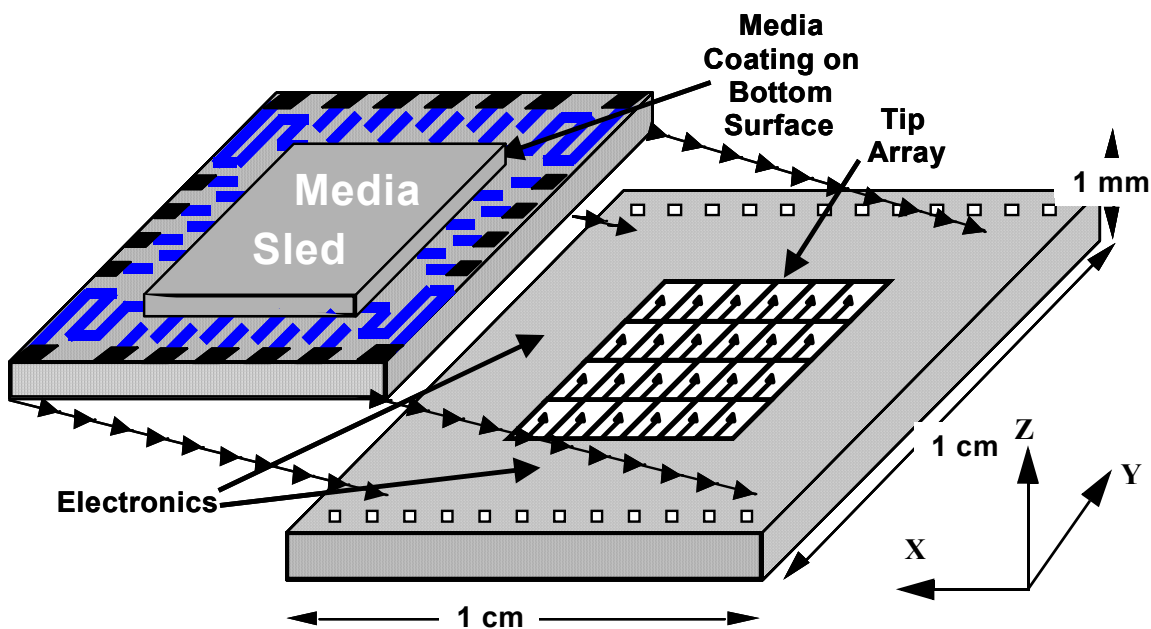
Figure 1.1 Conceptual Diagram: MEMS-Actuated Data Storage System [4]

The members of the tip array are referred to as "probes". Each probe has magnetic material deposited on it's tip which allows it to read and write magnetic bits onto the media. The magnetic media is attached to a series of MEMS actuators which allow it to move in the X and Y dimensions with respect to the probe tip array. Each probe can be actuated in the X and Z dimensions. A ΔC sensor is needed to measure the dis-

tance between the probe tip and the media in the Z dimension. This is used to servo the gap between the probe tip and the media and also to detect deflections of the probe caused by magnetic fields. This paper discusses the design of a ΔC sense amplifier for application to this probe-based data storage system.

Chapter 2: Background

2.1 Capacitive Sense Amplifiers

Most of the previous work to design integrated capacitive sense amplifiers has been focused on switched capacitor techniques. In a switched capacitor ΔC sensing system, the principle of charge distribution between the sense capacitance and the circuit is used to obtain a voltage at the output that is proportional to the value of the sense capacitance. A simple switched capacitor circuit is shown in figure 2.1 [5].
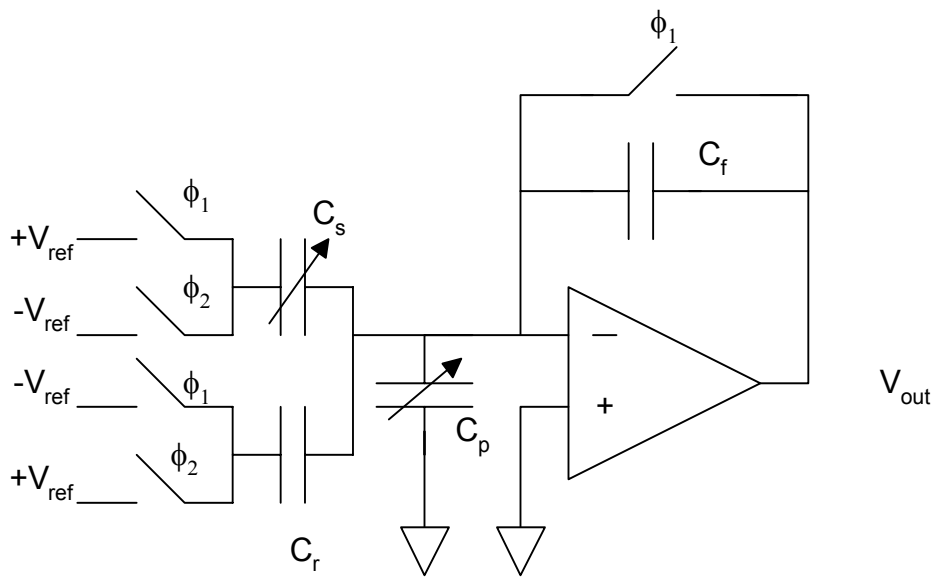

Figure 2.1 Simple Switched Capacitor ΔC Sensing Circuit

This circuit is a basic switched capacitor circuit which is shown to illustrate the principles of operation with a switched capacitor technique. C_s is the sensed capacitance, C_f is the feedback capacitor, C_r is a reference capacitor, and C_p is the parasitic capacitance on the inverting input node of the opamp. V_{ref} is a reference voltage. ϕ_1 and ϕ_2 are a pair of non-overlapping clocks. The dc biasing of this circuit is implemented by the reset system. When ϕ_1 is high, the opamp is in unity gain feedback and the output will change to set the node voltage at the inverting input to ground.

The output of this circuit is shown in equation 2.1.

$$V_{out} = V_{ref} \cdot \frac{C_s - C_r}{C_f} \quad (2.1)$$

The output of the amplifier is proportional to the difference between the sense capacitor and the reference capacitor. This circuit uses feedback to make the system insensitive to parasitics and opamp gain variation. Since both plates of C_p are held at a common potential, no current flows through the parasitic capacitor. Use of a matched reference capacitor helps the system become insensitive to many first order inaccuracies caused by fabrication and operating condition variation. More advanced switch capacitor circuits can be designed that are insensitive to amplifier offsets, 1/f noise, and charge injection noise. Also, switched capacitor circuits can be designed to have a digital output [6].

The fundamental limitation of switched capacitor circuits is the broadband noise that is generated by the switch transitions and the thermal noise of the amplifier. Because switched capacitor circuits are sampled-data systems, they undersample their own broadband noise, which gets aliased down into the signal band. The minimum detectable input to the system is ultimately limited by the undersampled broadband noise. Equation 2.2 shows the minimum detectable signal spectral density of the input to a switched capacitor system [2].

$$ MDS \approx \sqrt{\frac{8kT \cdot C_s}{f_{clk} \cdot V_{ref}^2}} \cdot sinc\left(\frac{f}{f_{clk}}\right) \quad (2.2) $$

Where k is Boltzmann's constant, T is the absolute temperature, V_{ref} is the a reference voltage, f is signal frequency, and f_{clk} is the frequency of the non-overlapping clocks, ϕ_1 and ϕ_2.

2.2 Chopper Stabilization

Chopper stabilization is a continuous time modulation technique that overcomes basic amplifier limitations such as offsets and 1/f noise. Chopper stabilization and autozeroing are similar in operation and so they are often confused. However, there is a clear distinction between these two circuit techniques. While autozeroing is a sampling technique, chopper stabilization is a continuous time modulation technique. This leads to different effects on the amplifier's broadband noise. A disadvantage of autozeroing is that the circuit will undersample the broadband, non-deterministic amplifier noise. This lead to aliasing of the broadband noise into the signal band. Chopper stabilization does not suffer from this effect and is therefore a more noise optimal solution for continuous-time systems [3].

The operation of a chopper stabilized system is actually rather simple. The signal is first modulated by a carrier to a higher frequency. Next, the modulated signal is amplified. After amplification, the signal is demodulated back down to it's original frequency. The advantage of such a system is that since the signal is modulated before passing through the amplifier, the frequencies at which the signal is present are far higher than the frequencies at which the amplifier exhibits low frequency noise. For example, a typical CMOS opamp has some offset voltage and a great deal of 1/f noise. The noise corner frequency where the 1/f noise is diminished to below the thermal noise floor of the opamp typical occurs in the 100's of kilo-Hertz. When the signal is demodulated, the offset and 1/f noise show up at high frequencies. For example, if the carrier signal is a square wave at 1 Mhz, the 1/f noise and offset will appear as a zero mean signal around 1 Mhz and it's odd harmonics. This low frequency noise now appears at much higher frequencies than the signal bandwidth and can easily be filtered. This is demonstrated graphically in figure 2.2 (This figure is not to scale.).
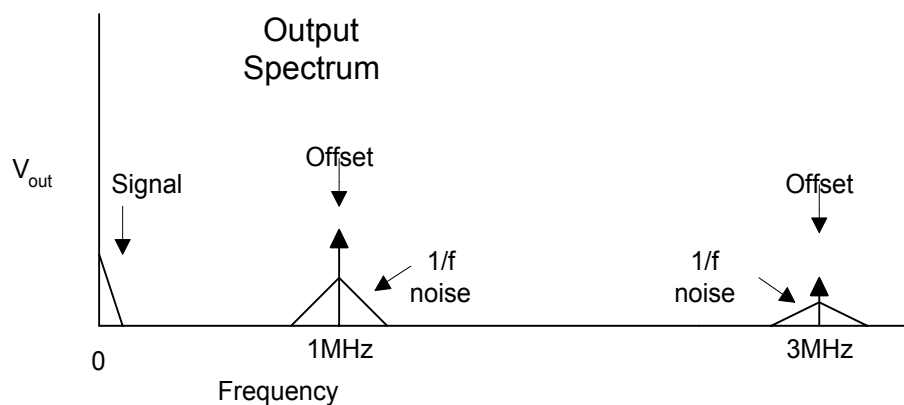
Figure 2.2 Example Output Spectrum for a Chopper Stabilized System

The major limitation of chopper stabilization is increased circuit bandwidth requirements. The circuit must now have a flat amplitude response at and beyond the carrier frequency, which can be many times the original signal bandwidth. This bandwidth requirement implies increased power dissipation. Nevertheless, when 1/f noise is the dominant source of noise and when bandwidth requirements are modest, chopper stabilization can be the most noise efficient technique. The system described in this report is a chopper stabilized system.

Chapter 3: System Design

3.1 System Topology

The system referred to in this chapter includes a capacitive sense amplifier, a variable capacitor, and a set of clocks including a modulation clock applied to the media side of the variable capacitor. The purpose of this system is to measure the capacitance between the probe and the media in order to determine the distance between the probe tip and the media. This information is used to servo the probe to keep it an optimal distance from the media. It can also be used to read data stored on the media. Data is stored as a pattern of magnetic fields on the media. If a magnetic material is deposited onto the tip of the probe, these magnetic fields will cause a small deflection in the probe and therefore change the capacitance between the probe and the media. The output of this system is a differential voltage that is proportional to the measured capacitance. The major constraints on the system are threefold; noise, power, and die area. A signal to noise ratio of at least 30 dB is required to reliably detect bits. The incremental power consumption (not including shared bias networks) and the die area per amplifier were to be minimized while achieving this noise performance.

A simplified block diagram of a capacitive sense amplifier is shown in figure 3.1
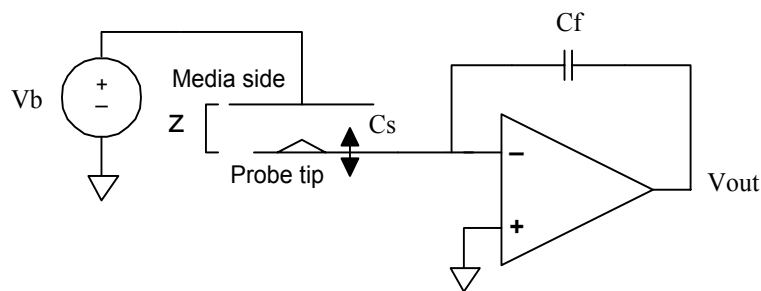
Figure 3.1 Simplified ΔCapacitance Sensor Circuit

Cs is the capacitor formed between the media and the probe tip. The distance between the probe tip and the media is labeled *z*. *Cs* is a time varying quantity as the probe-media distance varies as a function of time. This circuit operates on the principle of charge conservation and redistribution. *Cs* changes as the distance, *z*, changes, thus the charge is redistributed between *Cf* and *Cs* which causes a change in the output voltage.

The signal output voltage, *Vout*, is a function of *Cf*, *Cs*, and *Vb*. This relationship is shown in equation 3.1.

$$Vout = \frac{-(Vb \cdot Cs)}{Cf} \qquad (3.1)$$

Since *Cs* is the variable capacitor that this circuit measures, it should be represented as a function of the media - probe gap (*z*). This is shown in equation 3.2.

$$Vout = \frac{-Vb\left(\frac{\varepsilon_o A}{z}\right)}{Cf} \qquad (3.2)$$

We are also interested in the change of *Vout* with respect to a small change in the gap distance. Taking the first derivative of *Vout* with respect to *z* yields equation 3.3, where z_o is the initial gap.

$$\left.\frac{\Delta Vout}{\Delta z}\right|_{z_o} = \frac{V_b \varepsilon_o A}{Cf(z_o^2)} \qquad (3.3)$$

This equation shows the sensitivity of the circuit to small changes in capacitance.

The topology shown in figure 3.1 illustrates the basic functionality of the capacitive sense amplifier; however, it will not operate properly as shown. The circuit as shown, has no dc feedback path and therefore has no means of setting the voltage at the input to the opamp or of insuring that the inverting input voltage falls within the input voltage range of the opamp. Clearly this is not acceptable and a dc bias network must be included. In addition, the system as shown would be susceptible to 1/f noise and offsets. 1/f noise and offsets are low frequency and dc noises which fall into the same range of frequencies that we are interested in measuring. This motivates the use of a chopper stabilized modulated system.

Figure 3.2 illustrates an improved system based on chopper stabilization, which shows more detail of the circuit operation.
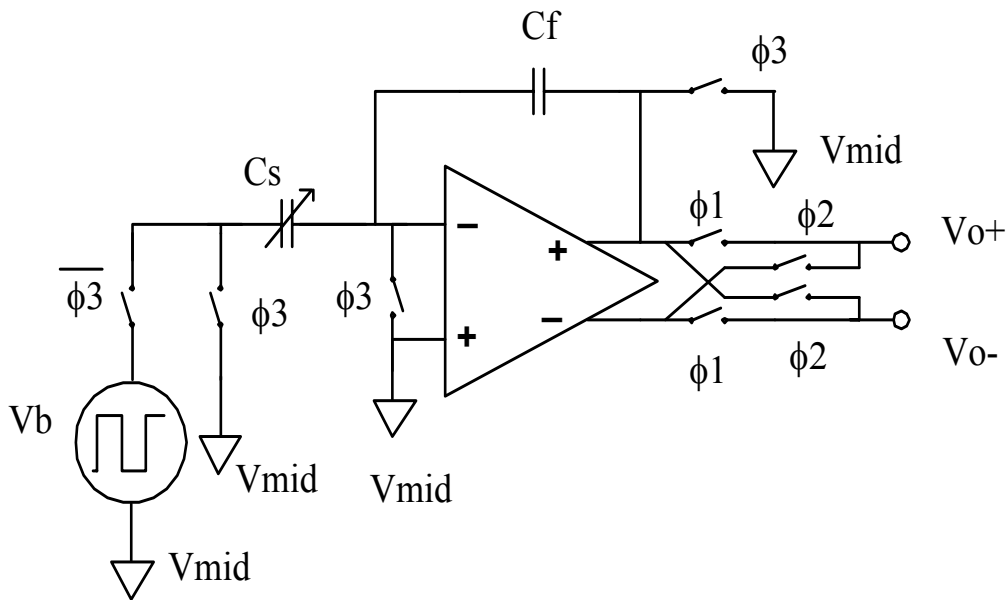
Figure 3.2 Chopper Stabilized Δ-Capacitive Sense Amplifier System

In this circuit *Vb* is now a square wave rather than a dc voltage source. The frequency of *Vb* can range from 500 kHz to several MegaHertz. The frequency of *Vb* must be higher than the 1/f noise corner frequency; however, if it is chosen too high, it places greater bandwidth demands on the opamp. This circuit was simulated with the frequency of *Vb* equal to 500 kHz and 1 MHz. *Vb* must drive a very large capacitance and even larger parasitics, so it is important to drive *Vb* with a large buffer. Since the media plate is common for the whole array of probe tips, only one such buffer is required. *Vb* becomes the carrier for a dual sideband amplitude modulated signal, which acts as the first half of the chopper stabilization scheme. *Cs* changes at relatively low frequency since the mechanical resonance of the probe is at a few KiloHertz. These low frequency changes in *Cs* are modulated by the carrier *Vb* and show up at the opamp input as sidebands to the high frequency carrier and it's odd harmonics (from the Fourier decomposition of a square wave).

The opamp in this system is fully differential. This is important for two reasons. The fully differential opamp provides both inverting and non-inverting symmetrical outputs, which are used by the chopper to demodulate the signal. Also, fully differential circuits have better power supply and substrate noise rejection than single ended circuits.

All switches were implemented with minimum size transmission gates. The four criss-crossed transistors at the output form a balanced modulator. A pair of non-overlapping clocks, ϕ_1 and ϕ_2, at the same frequency and phase as Vb control the switches of the modulator. This serves to demodulate the signal back down to the baseband.

The third clock phase, ϕ_3, is the reset phase. DC biasing occurs during the reset phase as both opamp inputs are set to $Vmid$. The reset phase occurs during the non-overlapping period while the clocks are transitioning from ϕ_1 to ϕ_2. All three clocks are non-overlapping. The switches controlled by ϕ_3, provide dc feedback by setting the voltage at both opamp inputs to midway between the supply rails. The feedback capacitor, Cf, is also reset by having both plates set to a common potential. Both plates of the sense capacitor, Cs, are also set to a common potential. Figure 3.3 shows the relative clock timing scheme. The time scale is exaggerated in order to show the detail of the non-overlapping and reset periods. In reality the reset and non-overlapping periods are much shorter than the time that ϕ_1 or ϕ_2 are high. It should be noted that the reset happens during every other transition. This is done in order to improve noise performance.
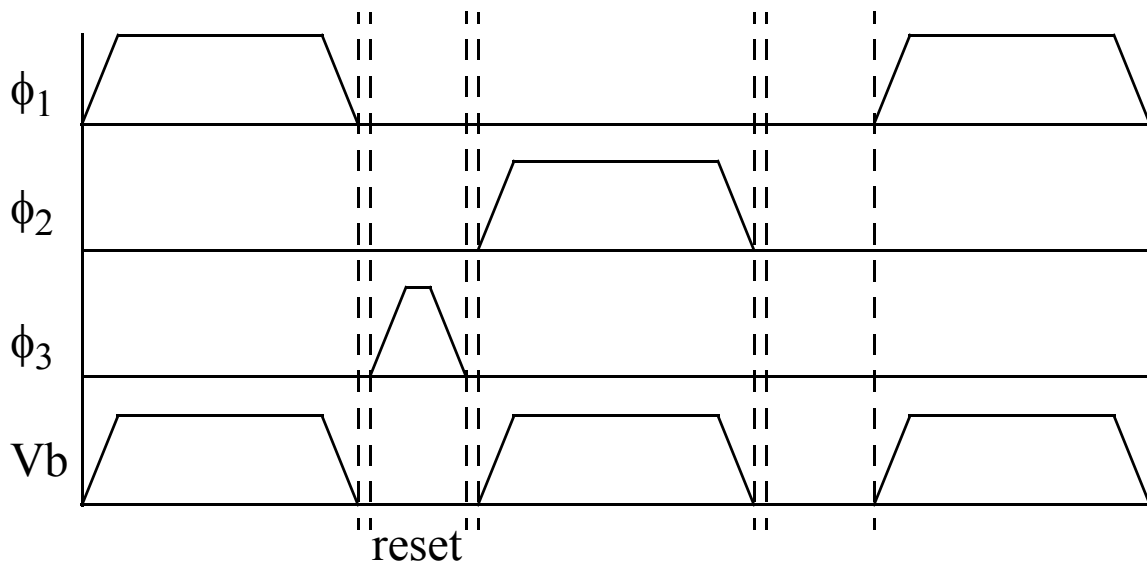
Figure 3.3 Clocking Diagram

3.2 Advantages of Chopper Stabilization and Reset Scheme

The chopper stabilization scheme used in this topology has several important advantages. One important advantage is the circuit's insensitivity to 1/f noise and offsets. Both offsets and 1/f noise occur at frequencies much lower than the modulating clock. Once the signal is demodulated by the balanced modulator at

the output, these noises are modulated up to the carrier frequency. This keeps the noise out of the signal bandwidth and allows it to easily be filtered.

There are two other important noise sources that are addressed by this system topology. Charge injection noise occurs when the reset switches are opened. Part of the charge that was stored in the channel of the switch MOSFET is injected onto the plate of capacitor Cf which creates a noise voltage at the sensitive input node of the operation amplifier. Another noise source that must be considered is the kT/C noise due to the resetting of the feedback capacitor. As the reset switch is opened the thermal noise in the channel of the switch MOSFET is sampled onto the feedback capacitor Cf. Unlike the charge injection noise, this kT/C noise in not deterministic.

The reset scheme that was implemented is insensitive to both kT/C noise and charge injection noise. Since the reset signal occurs after every other chopper transition, the same noise values are stored for both a ϕ_1 phase and a ϕ_2 phase. During the first phase the signal plus the stored noise is present at the output. During the second phase the signal and the inverse of the noise is present at the output. This causes the charge injection and kT/C noise to show up as a zero mean signal at the chopping frequency. As mentioned earlier, the chopping frequency is much higher than the signal bandwidth. Since the noise is high frequency and zero mean it can easily be filtered by a first order integrator.

Chapter 4: Noise Analysis of Δ Capacitance Sensor

4.1 Differential Amplifier Noise Analysis

The following is a detailed analysis of the electrical noise contributed by the amplifier in a capacitive sensing system. The purpose of this analysis is to motivate the choice of probe quantity and bandwidth. For a given probe structure the mechanical signal-to-noise ratio is presented for a fixed power budget and data rate. The resonant frequency of the probe is fixed at 10 kHz. The power budget in this example is 1 Watt for the entire array of sense amplifiers and the system data rate is specified to be 100 Mega-bits per second. This analysis is focused on the differential amplifier pair at the input to the amplifier since in general its noise contribution is dominant. Figure 4.1 shows a typical differential amplifier.
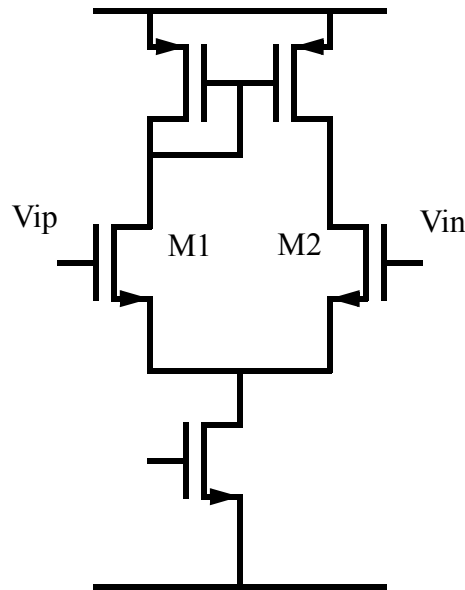

Figure 4.1 Typical Differential Amplifier

The noise of this amplifier can be referred to a voltage noise source at the input node *Vip*. The first step to obtaining the signal-to-noise ratio of the capacitive sense amplifier is to find the value of this input referred noise. At high frequencies the dominant source of noise for this amplifier is the drain current noise of M1 and M2. For simplicity half circuit analysis is employed and the noise of only M1 is considered. The drain current noise of M1 is given by equation 4.1.

$$i_d^2 = 4kT\frac{2}{3}g_{m1} \qquad (4.1)$$

where k is Boltzmann's constant, T is the temperature in Kelvin and g_{m1} is the transconductance of M1.

The noise power can be referred to a voltage at the input node *Vip* as shown in equation 4.2.

$$v_n^2 = \frac{i_d^2}{g_{m1}^2} \qquad (4.2)$$

The input referred noise can also be represented as a current as shown in equation 4.3.

$$i_n^2 = (j\omega Cgs)^2 \, v_n^2 \qquad (4.3)$$

For a given transconductance and input capacitor size, the v_n and i_n contributions to the overall system noise can be found. In order to find the signal-to-noise ratio we have to examine the signal gain of the system in question. This is covered in the following discussion.

4.2 Sensitivity of Capacitive Sense Circuit

Figure 4.2 shows the small signal representation of a Δ capacitive sense circuit without dc biasing, reset or chopping networks shown.
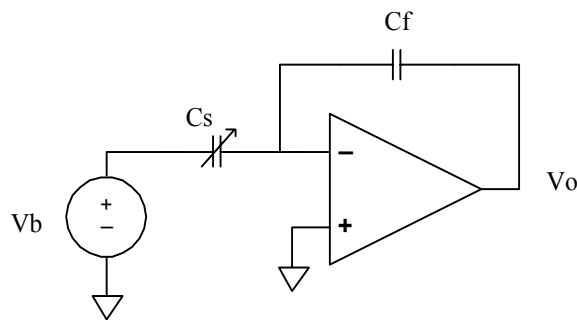
Figure 4.2 Basic Δ-Capacitance Amplifier

The signal output voltage *Vo* is shown in equation 4.4.

$$Vo = \frac{-Vb\left(\frac{\varepsilon_o A}{z}\right)}{Cf} \quad (4.4)$$

A = plate area

z = gap

Vo is the signal voltage at the output for a fixed Vb and gap. Taking the first derivative of Vo with respect to z yields equation 4.5.

$$\left.\frac{\Delta Vo}{\Delta z}\right|_{z_o} = \frac{V_b \varepsilon_o A}{Cf(z_o^2)} \quad (4.5)$$

z_o = initial gap

This equation shows the sensitivity of the circuit to small changes in capacitance. In order to determine the input referred noise, superposition was used to separately determine the noise due to v_n and i_n.

4.3 Noise Due to v_n

Figure 4.3 shows the basic capacitive sense circuit with the amplifier's input referred voltage noise added as a voltage source in series with the input.
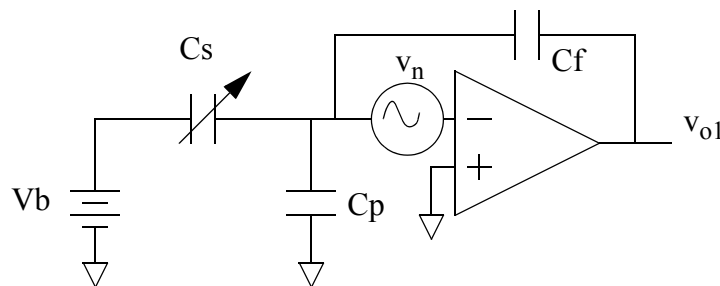
Figure 4.3 Δ-Capacitance Amplifier with Voltage Noise

Since no dc current can flow from the input node of the opamp, the dc charge stored on this node is constant. Therefore, the small signal charge on this node is zero and the charge stored on the plates of the three capacitors connected to this node must sum to zero. This is expressed in equation 4.6.

$$qs + qp + qf = 0 \qquad (4.6)$$

From the definition of charge stored in a capacitor we can get equation 4.7 and equation 4.8.

$$v_n - v_{o1} = \frac{qf}{Cf} \qquad (4.7)$$

Where v_{o1} is the output voltage due to the voltage noise v_n.

$$qf = -(Cs + Cp)v_n \qquad (4.8)$$

Combining (4.7) and (4.8) yields:

$$v_n - v_{o1} = \frac{(-(Cs + Cp))v_n}{Cf} \qquad (4.9)$$

solving (4.9) for v_{o1} gives:

$$v_{o1} = v_n\left(\frac{Cs + Cp + Cf}{Cf}\right) \qquad (4.10)$$

This is the noise component at the output which is due to v_n.

4.4 Noise Due to i_n

Figure 4.4 shows the basic capacitive sense circuit with the amplifier's input referred noise represented as a current source in parallel with the input. The noise in the output voltage (v_{o2}) due to i_n is analyzed and it's noise power is added to the noise power due to v_n.
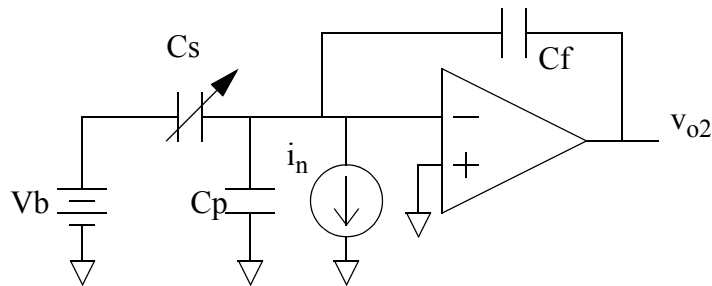
Figure 4.4 Δ-Capacitance Amplifier with Current Noise

Since *Cp* and *Cs,* to a first order, have no small signal potential difference across them and no current can flow into an ideal opamp, i_n must flow through *Cf*. This creates a potential difference across *Cf* which causes a current noise induced voltage, $v_{o2,}$ which is shown in equation 4.11.

$$v_{o2} = \frac{i_n}{sCf} \quad (4.11)$$

By using (4.3) i_n can be expressed as a function of v_n as shown in equation 4.12.

$$v_{o2} = \frac{s \cdot Cgs \cdot v_n}{s \cdot Cf} = \frac{Cgs \cdot v_n}{Cf} \quad (4.12)$$

4.5 Total Input Referred Noise

Since v_{o1} and v_{o2} are correlated, we can add expressions (4.10) and (4.12) to arrive at the total noise-induced output voltage. The total noise voltage squared at the output of the preamp is given by equation 4.13.

$$V_{total noise}^2 = v_n^2 \left(\frac{Cs + Cp + Cf + Cgs}{Cf} \right)^2 \quad (4.13)$$

The input referred noise can be expressed as an rms displacement by dividing by the *Vout/Δz* gain. Equation 4.14 shows the circuit noise expressed as an rms error in the measured displacement. Equation 4.14 can be multiplied by the square root of the system bandwidth in order to estimate the best displacement resolution theoretically achievable.

$$|z_n| = \frac{v_n \left(\dfrac{Cs + Cp + Cf + Cgs}{Cf} \right)}{\dfrac{V_b \varepsilon_o A}{Cf \cdot z_o^2}} \quad (4.14)$$

The displacement noise, z_n is proportional to the sum of *Cs, Cp, Cf*, and *Cgs*. Therefore it is important to minimize *Cp* and to choose a small but practical value for *Cf*. If *Cf* is large, poor noise performance will result. However, too small a value of *Cf* will result in a high voltage gain and will necessitate the choice of a small *Vb* if the voltage supply is limited.

4.6 Noise Examples for Different Quantities of Probes

It is of interest to compare the signal-to-noise ratios of systems that use a different number of probes to achieve the same overall data rate. One could use many probes operating in parallel at relatively low frequencies. Alternatively, a system could be designed to achieve the same data rate with a smaller number of probes that operate at higher frequencies. The purpose of this example is to illustrate how the choice of probe quantity impacts upon the signal-to-noise ratio of the system. Also, it is important to determine if there is a noise optimal operating bandwidth for a given probe structure.

For this example, a comparison is made with systems using a probe designed by Dave Guillou [2] which was also implemented on the test chip. This probe has a resonant frequency of approximately 10 kHz and a static signal displacement of 33 pico-meters. The response of the probe as a function of frequency is shown in figure 4.5.
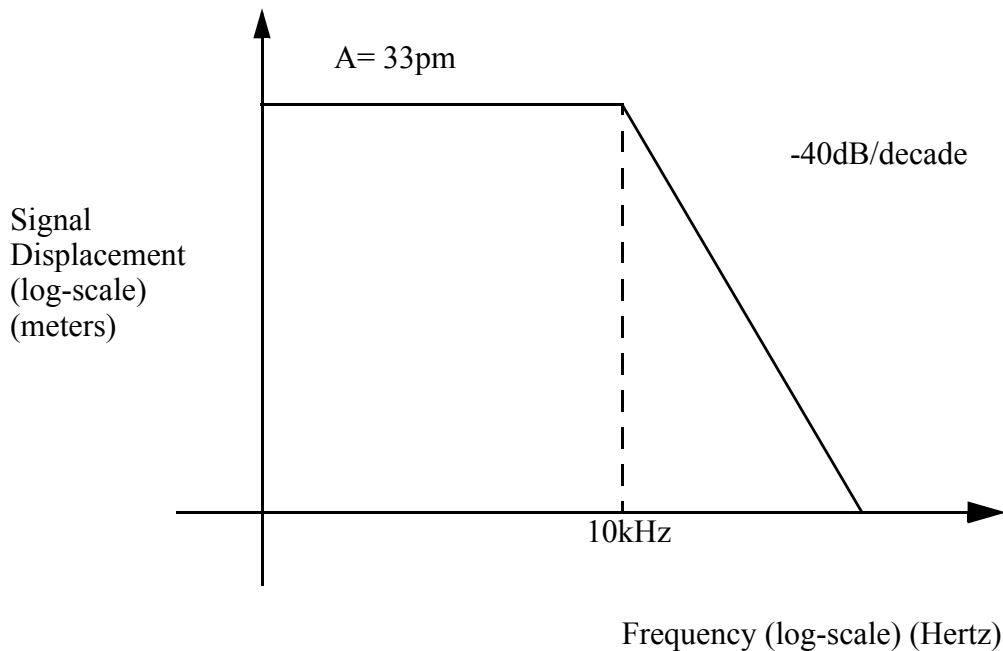
Figure 4.5 Probe Frequency Response

For this example, it was assumed that one half of the 1 Watt power budget would be dissipated in the first stage of the amplifier. It was also assumed that the first stage would consist of a differential pair which implies that one quarter of the total power would be dissipated in each branch of the differential pair. I_d is the current through each branch of the differential pair.

Table 1: Drain Currents

Number of Probes	System Bandwidth	Power per probe	I_d
10,000	10kHz	100 uW/probe	8.3 uA
1,000	100kHz	1 mW/probe	83 uA
100	1 MHz	10 mW/probe	830 uA

For all three example systems the ΔVgs is set to .25 Volts in order to maximize the transconductance. Therefore, the transconductances of the first stages are set at 6.64mA/V, 664uA/V, and 66.4uA/V for the 100 probe, 1,000 probe, and 10,000 probe systems respectively. Plugging g_m into equations (4.1), (4.2), and (4.3) yields v_n and i_n which are needed to find the voltage noise of the amplifier. For this particular probe the following parameters apply:

$z_o =$ 215 nm

$Cs = 25.7$ fF

$Cp = 10$ fF

$Cf = 10$ fF

$Cgs = 7.3$ fF

$Vb = 1$V

$A = 625$ um^2

These parameters along with v_n and i_n of the three systems can be plugged into equation 4.14 to yield the amplifier thermal noise represented as an rms displacement. Table 2 shows v_n^2 and the magnitude of the rms displacement ($|z_n|$) of each system.

Table 2: Noise per Root Hertz

Number of Probes	$v_n{}^2$	$|z_n|$
100	1.666×10^{-18} V/Hz	.57 fm /Hz$^{1/2}$
1,000	16.66×10^{-18} V/Hz	1.8 fm /Hz$^{1/2}$
10,000	166.6×10^{18} V/Hz	5.7 fm /Hz$^{1/2}$

Table 2 gives the amplifier noise referred to a displacement error as a function of system bandwidth. To maintain a constant data rate the bandwidth of each system must be inversely proportional to the number of probes. Table 3 shows the displacement noise per root Hertz, bandwidth, and total rms displacement error due to amplifier noise.

Table 3: RMS Displacement Noise

Number of Probes	$|z_n|$	Bandwidth	Rms Displacement noise
100	.57 fm /Hz$^{1/2}$	1MHz	570 fm rms
1,000	1.8 fm /Hz$^{1/2}$	100kHz	570 fm rms
10,000	5.7 fm /Hz$^{1/2}$	10kHz	570 fm rms

Table 3 shows that the amplifier thermal noise of all three systems causes exactly the same noise when referred to a displacement of the sensing capacitor. However, the signal amplitude has a second order rolloff following the device resonance at 10 kHz as shown in figure 4.3. To achieve maximum bit-rate the signal should be present at the frequency corresponding to the system bandwidth. By dividing the signal magnitude by the rms noise we can obtain a one standard deviation signal-to-noise ratio. Table 4 lists the signal frequency, the signal amplitude, the rms displacement noise, and the signal-to-noise ratio for each system.

Table 4: Signal-To-Noise Ratio

Number of Probes	Signal Frequency	Signal Amplitude	Rms Displacement noise	SNR
100	1Mhz	3.3 fm	570 fm rms	-44.75 dB
1,000	100Khz	330 fm	570 fm rms	-4.75 dB
10,000	10Khz	33 pm	570 fm rms	35.25 dB

The signal-to-noise ratios shown in table 4 make a strong case for using a system composed of many probes operating at lower signal frequencies. It is not power efficient to run higher currents though the amplifier in order to improve the signal-to-noise ratio when the probes are operating above their resonant frequency. This analysis assumed that all systems are using identical probes. This would not be the case in a real system, because the storage requirements would mandate that if fewer probes were to be used, they would each have to cover a larger area. This implies larger probes which would have more mass and greater compliance. Both of these factors would lower the probe resonant frequency and make the noise disadvantages of systems with a low number of probes even more pronounced. In brief, it does not make much sense to fight against the mechanically limited bandwidth when the option of further parallelism is available. A noise and power optimal system would use the largest number of small probes that could be reliably manufactured.

Chapter 5: Amplifier Topology and Design

5.1 Folded Cascode Design

In this section, the choice of topology and the design procedure for the operation amplifier used in the capacitive sensing system is discussed. This opamp was designed in the HP .5 micron CMOS process. The most important requirements for this opamp and were low noise and very low power. Also a fully differential design was necessary in order to have both positive and negative outputs to deliver to the balanced modulator. The load of the opamp was the gate of a MOSFET so there was no need to design an opamp that could drive a resistive load. A fully differential folded cascode amplifier is a logical choice as it has only one high impedance node and can have a larger bandwidth for a given power dissipation.

A simplified folded cascode opamp is shown in figure 5.1. The purpose of this diagram is to introduce some of the design variables of a folded cascode amplifier before going into a detailed analysis. The bias network and common-mode feedback (CMFB) circuit are not shown.
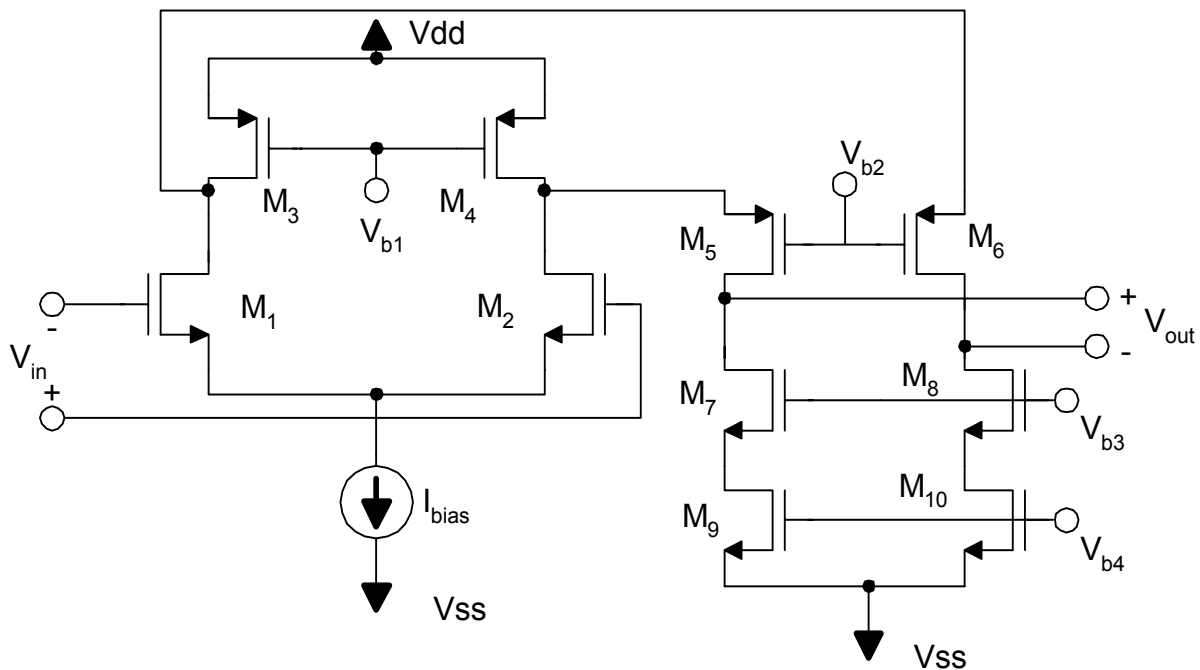

Figure 5.1 Simplified Folded Cascode

M_1 and M_2 form a differential pair with I_{bias} setting the tail current. M_3 and M_4 are current sources which supply current both to the differential pair and the common gate amplifiers to the right. M_5 and M_6 are a pair of common gate amplifiers that form the cascode circuit. M_7, M_8, M_9, and M_{10} form a pair of cascode

loads for the folded cascode amplifier. The bias circuits for these cascode loads provides the correct voltages V_{b3} and V_{b4} to ensure that the cascode loads are biased to provide a wide swing cascode load. A common mode feedback circuit is needed to set the output common mode voltage to a value midway between the supply rails.

Each of the outputs of the folded cascode amplifier are hooked up to the gate of a MOSFET of the circuit that follows the capacitive sense amplifier. In the case of the test circuit, these MOSFETS are the input differential pair of a buffer amplifier. The opamp is compensated by the gate capacitance provided by the following stage.

The drain current through each transistor of the input pair is equal to half the value of I_{bias}. The current through the common gate amplifiers is set by the difference between the drain current of M_3 or M_4 and $I_{bias}/2$.

Figure 5.2 shows the complete folded cascode circuit that was implemented in the capacitive sense system. The circuit is shown in two parts; figure 5.2a shows the amplifier and figure 5.2b shows the bias network. One bias network can be shared by many amplifiers and this should be taken into account when considering the die area of this circuit.

Figure 5.2a Fully Differential Folded Cascode

M_{12} is a diode connected transistor that sinks the current provided by I_{bias1}. This transistor is one of two master current mirrors for the circuit. M_{11} forms a current mirror with M_{12} to provide the current source for the differential pair. M_{13} is a diode connected P-type transistor that sources the current pulled by I_{bias2}. This transistor is the second master current mirror for this circuit. The ΔVgs of M_{13} sets the bias voltage for the gates of transistors M_3 and M_4. M_{25} and M_{26} are included to improve performance while the amplifier is slewing. They increase the slew rate and also help the amplifier recover quickly from slewing conditions.

Compensation for this circuit is provided by the capacitive load attached to the output nodes. In the case of the test circuit, this capacitance is the gate capacitance of the buffer that follows the opamp.

5.2 Common mode Feedback Circuit Operation

M_{20} and M_{21} comprise the common mode feedback circuit. These transistors operate in the linear region. In the linear region these transistors act a variable resistors. The gate voltage of a linear region transistor controls the channel resistance seen between the source and the drain. Since M_{20} and M_{21} are P-type transistors, a decrease in the gate voltage corresponds to an decrease in the resistance between the source and the drain. An increase in the gate voltage causes the resistance between the source and the drain to increase

The drains of M_{20} and M_{21} are tied together to form a node that acts as a pseudo power supply rail for the gain stages of the opamp. If a differential signal is present at the output of the opamp, one of the CMFB transistors will increase in resistance while the other decreases, so the net resistance and Ohmic drop between Vdd and the pseudo rail will remain unchanged. However if a common mode signal is present at the outputs, the net resistance of the CMFB transistors and the Ohmic drop at the pseudo rail will change to cancel the common mode output.

 For example, if there is a positive common mode signal present at the outputs, the gate voltages of both M_{20} and M_{21} will be increased. This increase in gate voltage turns the transistors more off and increases the resistance between the source and drain of both resistors. This in turn causes a larger Ohmic drop between *Vdd* and the pseudo rail at the drains of the CMFB transistors since the sum of the currents flowing through them is constant. The drop in the rail voltage seen by the opamp will cause the output nodes to experience a common mode voltage drop until the circuit reaches an equilibrium. The sizes of the CMFB transistors are chosen such that the equilibrium occurs midway between the power supply rails.
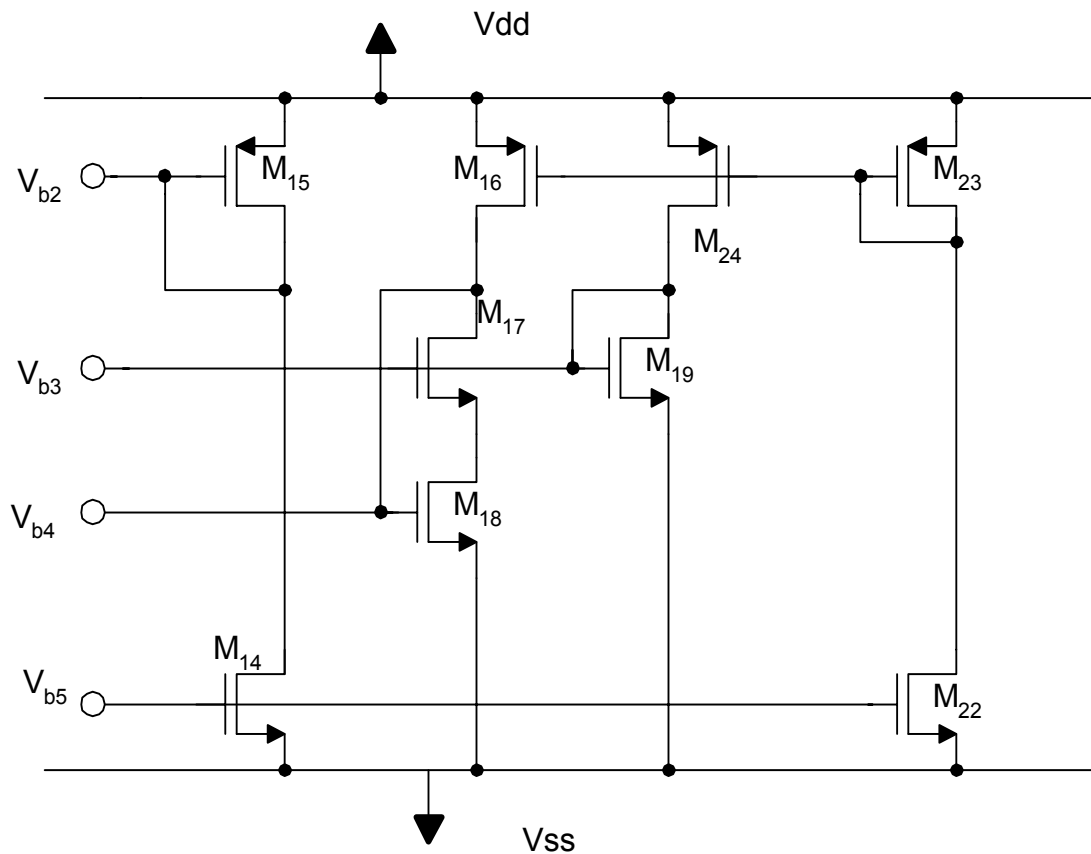
Figure 5.2b Bias Circuit

Figure 5.2b shows the bias network for the opamp. M_{14} is a current mirror which mirrors a scaled version of the current flowing through master current mirror M_{12}. The current is scaled by the by the W/L ratios of M_{12} and M_{14}. The current mirrored through M_{14} is then reflected the by P-channel diode-connected transistor M_{15}. The *Vgs* of M_{15} sets the bias voltage V_{b2} to bias the common gate amplifiers consisting of transistors M_5 and M_6. The transistors M_{16}, M_{17}, M_{18}, M_{19}, M_{22}, M_{23}, and M_{24} form a "wide-swing cascode current mirror" [7, 8]. This current mirror has the advantages of a cascode current mirror, such as increased output impedance without limiting the swing range because only one threshold voltage drop is needed across it. The sizing is determined by the current needed to satisfy the power budget requirements. The complete netlist of the fully differential folded cascode opamp is shown in appendix A.

5.3 Opamp Simulations and Specifications

All simulations in this section are of the extracted netlist of the opamp under nominal process and operating conditions. Information detailing the layout can be found in appendix B. Figure 5.3 shows the AC magnitude and phase response of the opamp.

Figure 5.3 Opamp Bode Plot

Figure 5.4 shows the transient response at the output under slewing conditions.
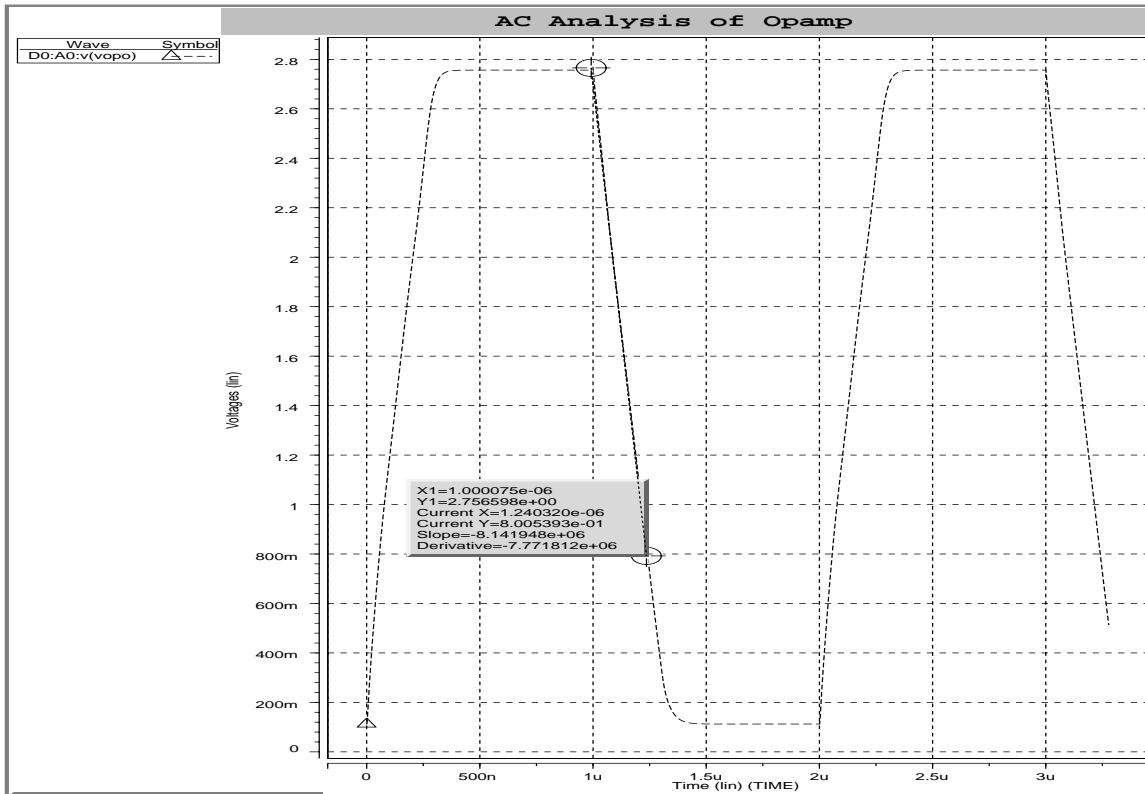
Figure 5.4 Opamp Slewing Transient

The unity gain frequency of the opamp is 15.7 Mhz. The phase angle measured at this frequency is -103 degrees. This gives a phase margin of 77 degrees. As figure 5.3 shows, the opamp is unity gain stable and has an acceptable phase margin. The low frequency gain of the opamp is 1570 which implies a low gain error under feedback. The slew rate of this opamp is 8 V/us. Table 5 lists a summary of the opamp's specifications as measured from the netlist extracted from the layout under nominal operating and processing conditions.

Table 1: Opamp Specifications

Specification	Value
Open loop gain	1,570
Bandwidth	15.7 MHz
Power consumption	218.7 uW (including bias circuit)
Phase Margin	77º
Gain Margin	39 dB
Maximum output swing	1.8 Volts
Slew Rate	8 V/ us

Chapter 6: System Simulation Results

6.1 System Linearity

Figure 6.1 shows a plot of the system linearity. A variable capacitor was used in this simulation to measure the differential output voltage for different values of the sense capacitor. The control signal to the variable capacitor was a piece-wise linear ramp which ramped the capacitance from 0 fF at time 0 to 50 fF at time = 1ms. The output of the amplifier was put through a first order lowpass filter in order to filter noise at high frequency. The Y axis is the system output voltage and the X axis is time.
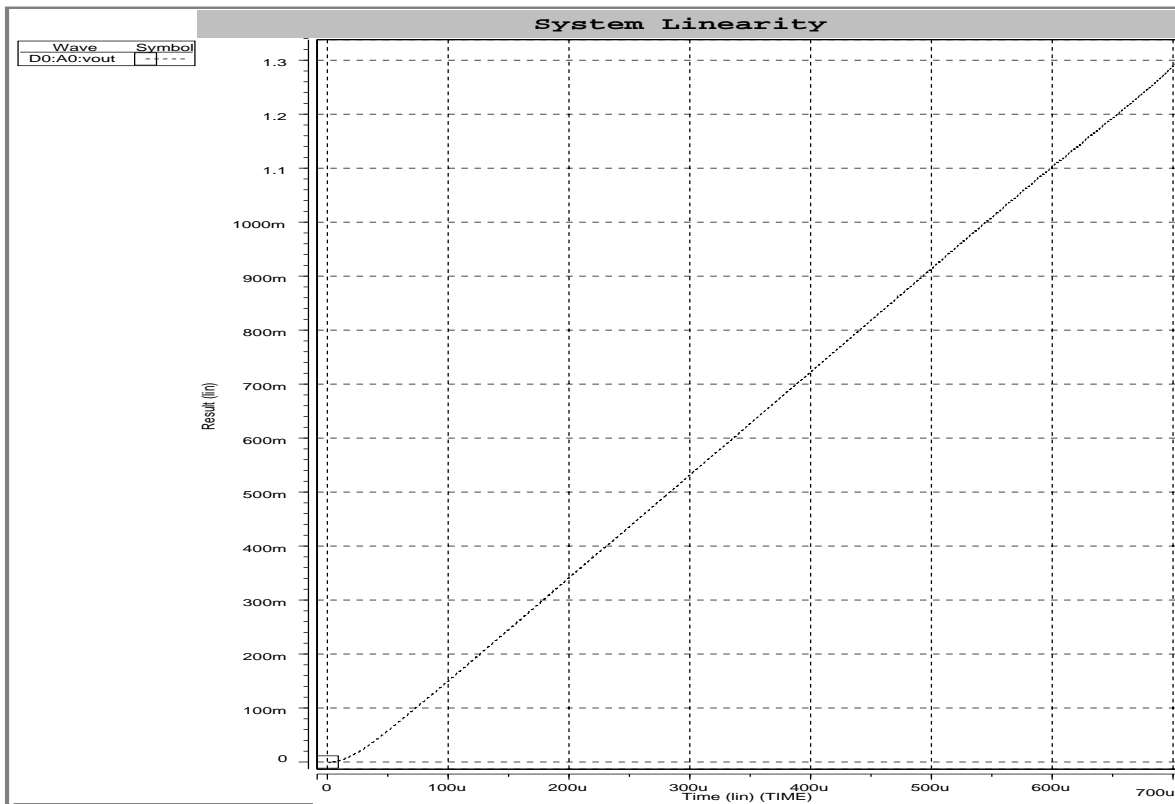
Figure 6.1 System Linearity

Overall the system is very linear with a slight deviation from linearity for very low values of Cs. This is due to parasitic capacitors that prevent the amplifier from reading zero capacitance. The overall linearity is

sufficient to servo the probe-to-media distance since the departure from linear response occurs only when the probe tip is furthest from the media.
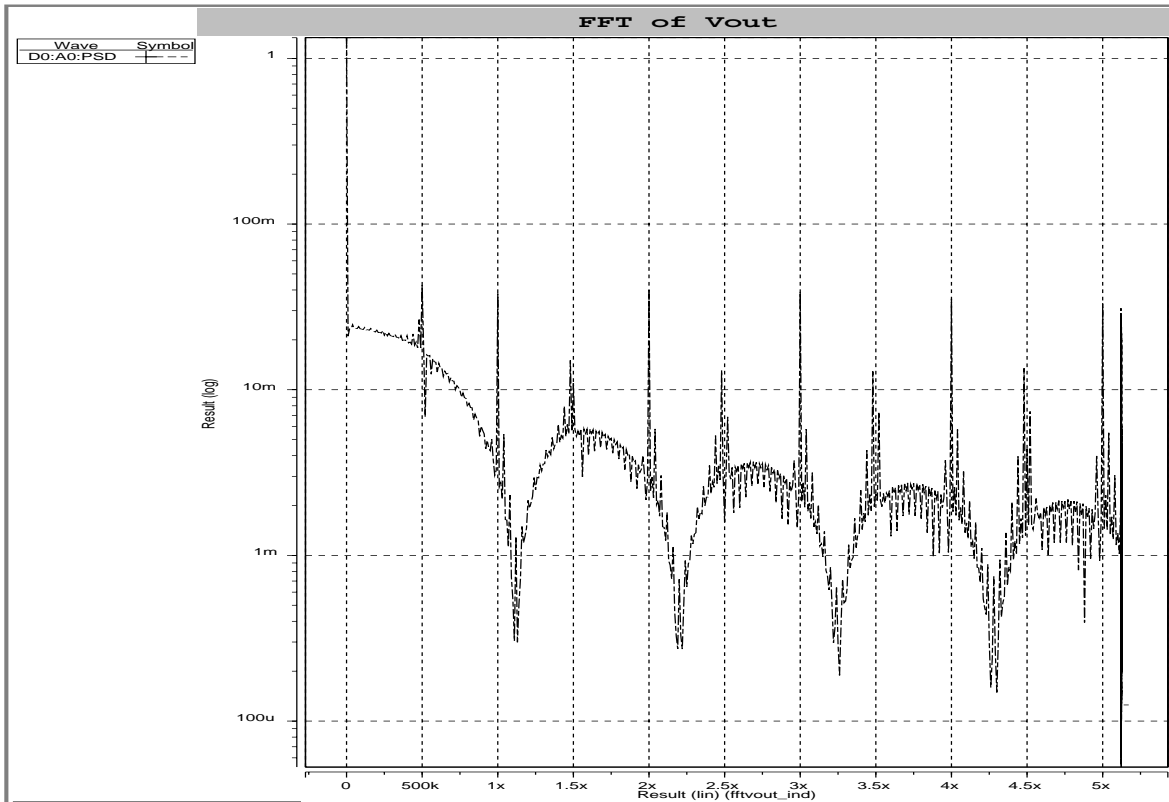
6.2 Power Spectral Density

An FFT (Fast Fourier Transform) of the output voltage before and after a simple first order low pass filter is shown in figure 6.2. For this simulation the sense capacitor was held at a dc value of 15 fF.
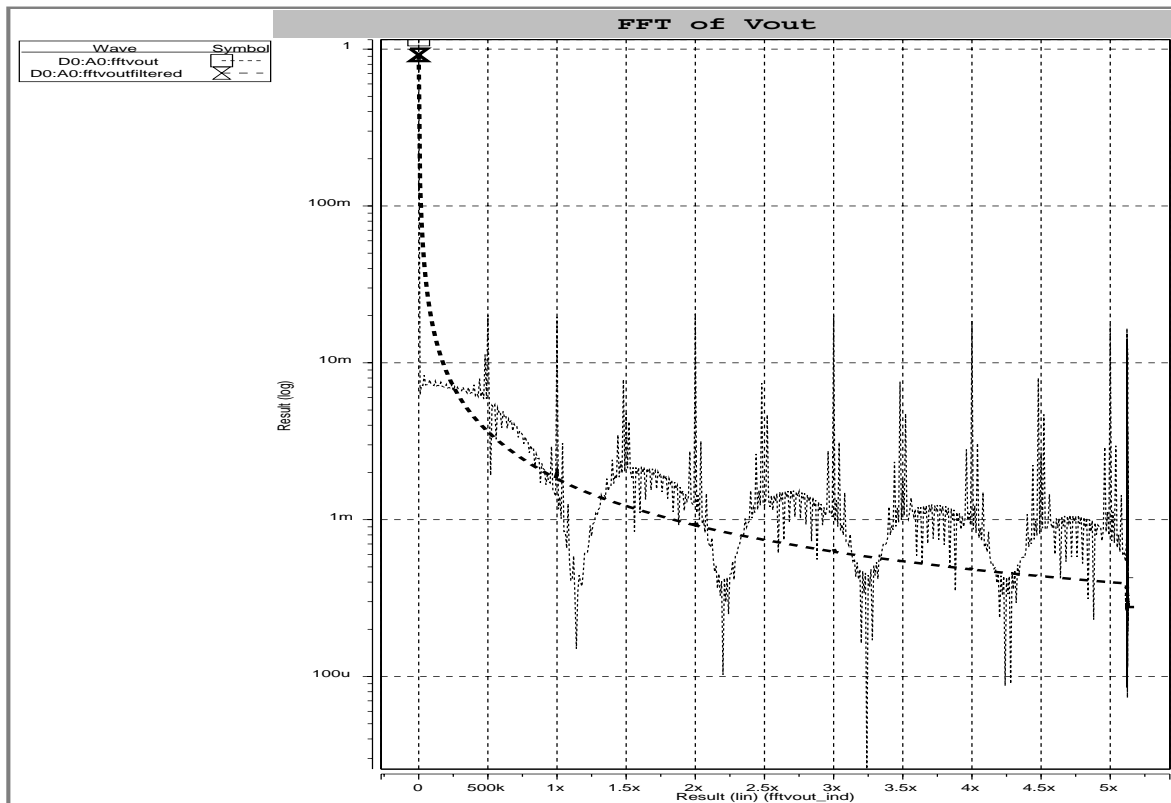
Figure 6.2 Output Voltage Spectrum

The unfiltered output shows the majority of signal at dc, with noise at the chopping frequency and harmonics of the chopping frequency. The smooth curve shows the same output after being passed through a first order low pass filter to remove the high frequency noise.

Figure 6.3 is a plot of the system power spectral density for the same test conditions.

Figure 6.3 Output Power Spectral Density

Again, the output is concentrated at dc, where the signal is present, with spikes of noise at the chopper frequency and it's harmonics.

6.3 System Transient Response

This section will demonstrate the transient response of the system and show outputs from various nodes within the system to demonstrate the system operation. For this example, the variable capacitor that was used to simulate *Cs* was modulated with a sine wave at 10 kHz. Figure 6.4 shows the control signal which is proportional to the ac value of *Cs*. Node *s11* is a voltage proportional to the value of *Cs*. *Cs* is defined as a variable capacitor with the following two spice commands:

Vctrl s11 0 SIN(.5 .5 10k 0 0)

Gcs s1 vb VCCAP PWL(1) s11 0 DELTA=.00001 -1v,1f 2,15f

When v(s11) is at it's peak *Cs* is equal to 10.3 fF and when it is at it's minimum the value of *Cs* is equal to 4.7 fF.
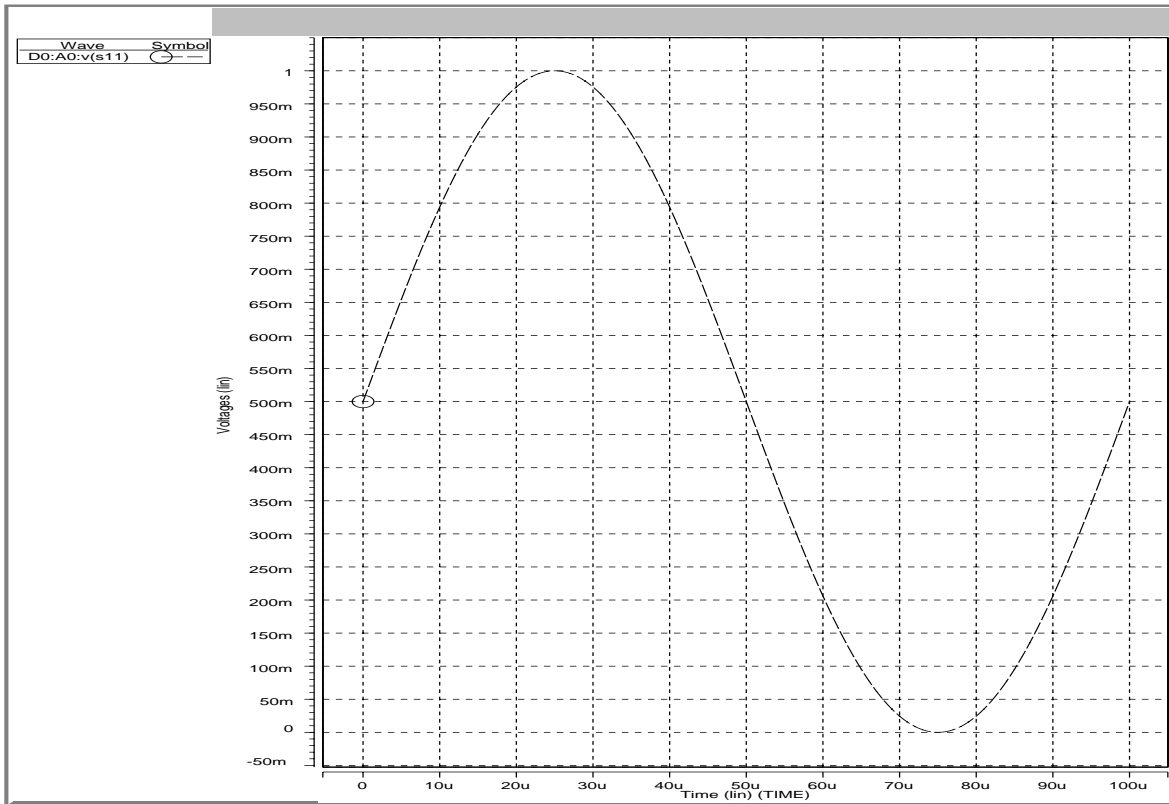

Figure 6.4 Variable Capacitor Control Signal

Figure 6.5 shows the high frequency output of the amplifier. The signal has been modulated by the square wave *Vb* and is visible as the envelope of the high frequency carrier.
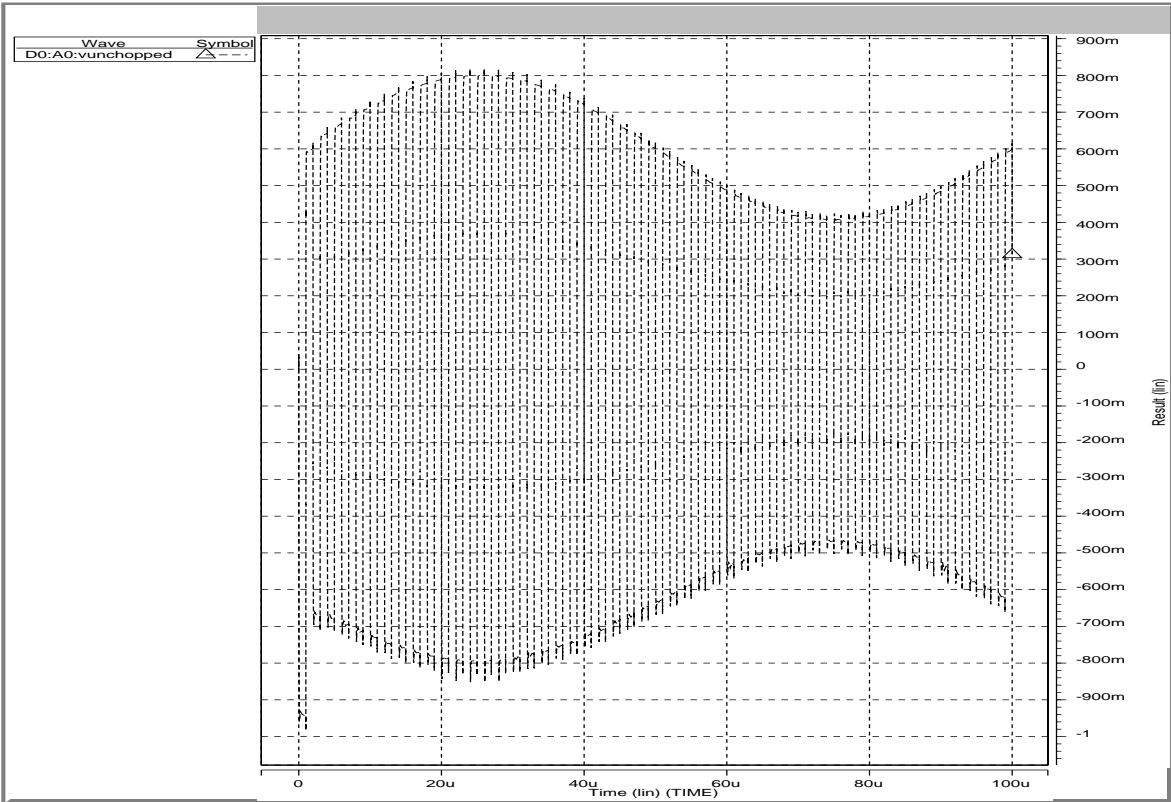
Figure 6.5 Amplifier Output Modulated

Note how the envelope tracks the change in capacitance of *Cs*.

Figure 6.6 shows the waveform after it has been demodulated by the chopper. Now the 10 kHz signal is present in the baseband. The high frequency content of this waveform is due to the reset clocks and charge injection.
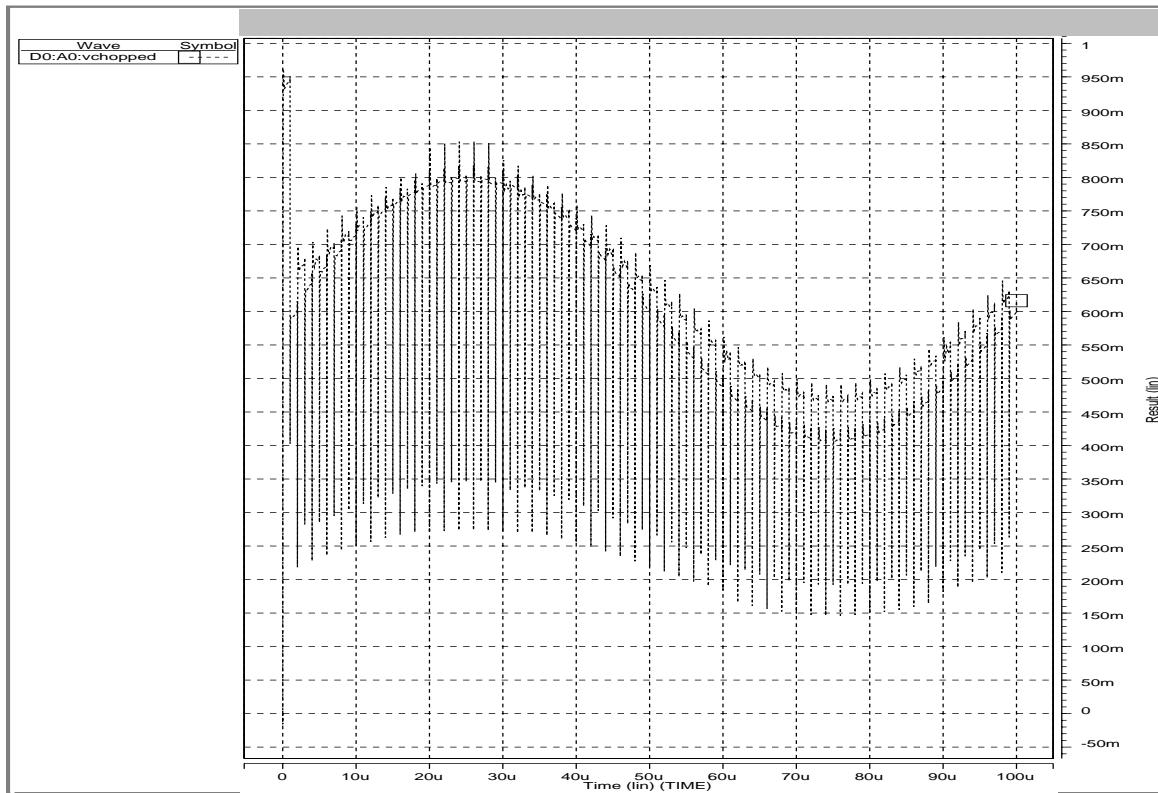
Figure 6.6 System Output Demodulated

Since the noise is at a much higher frequency than the signal output it can quite easily be filtered This filtering can take place in the digital domain, after the output is sampled or by using a first order low pass filter. In this example a simple 1st order low pass filter at 80 kHz is used. Figure 6.7 shows the output waveform after it has been filtered. The original 10 kHz waveform is apparent in the output. Several cycles of this waveform are shown.
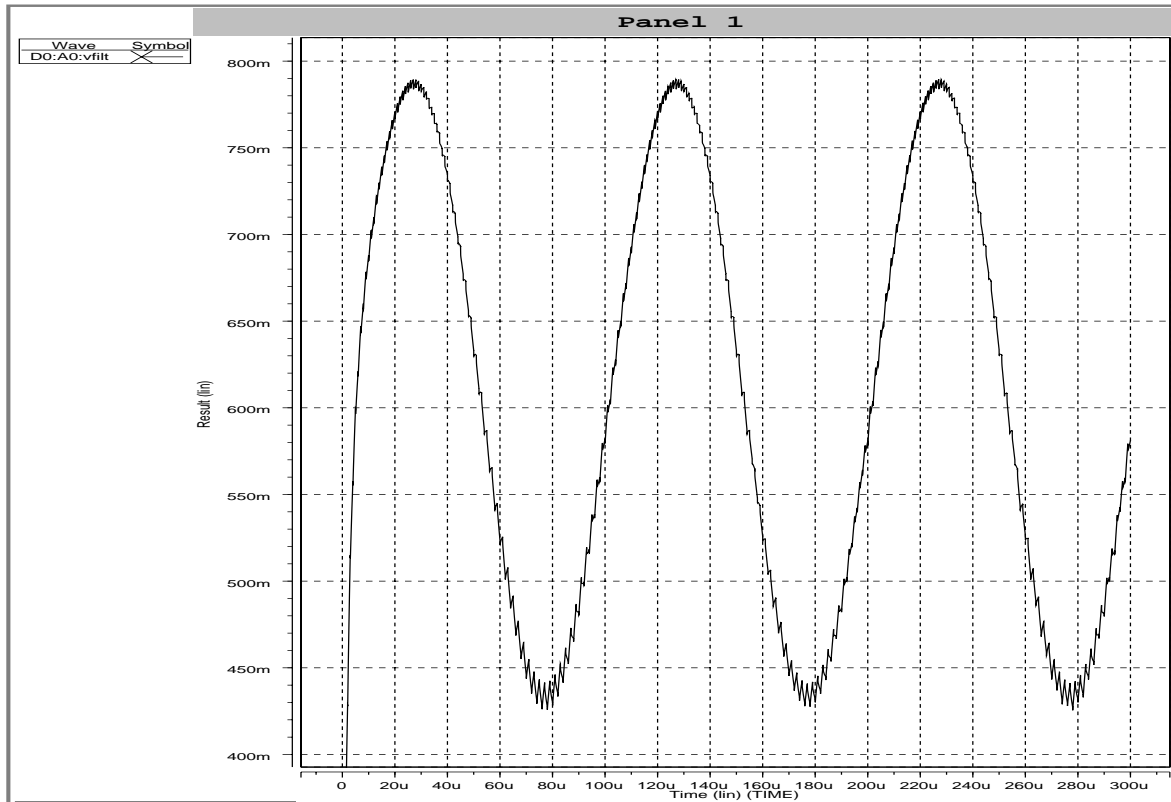
Figure 6.7 System Output Filtered.

6.4 System Simulation Summary

The variable capacitive sensing system showed no observable departure from linearity when measuring capacitance values greater than 5fF. The peak of the high frequency noise voltage is 34 dB below the dc signal level and this can be easily filtered. The modulation technique was demonstrated with a transient response of the variable capacitor control signal, the high frequency modulated signal, and the output base-band signal.

Chapter 7: Conclusions

This work describes the design of a capacitive sense amplifier system. A chopper stabilized system topology was discussed and implemented. The design utilized a fully differential folded cascode amplifier. The topology of the amplifier was discussed and explained. A detailed noise analysis of a chopper stabilized capacitive sense amplifier was presented. The system can be used to achieve a signal-to-noise ratio of 30dB and a data rate of 10 kpbs per probe when implemented in a MEMS data storage system. A scaling argument was also presented that showed the noise and power advantages of scaling the system to increase the number of data reading probes while decreasing the size of each probe. Finally, the system was laid out, extracted, simulated, and submitted for fabrication.

References

[1] R. Puers, "Capacitive Sensors: When and How to use Them", Sensors and Actuators A, vol. 37, pp 93-105, 1993

[2] D. Guillou, "Low-Noise Readout Amplifier for Variable-Capacitance Micromechanical Sensors with Non-Linearity Correction" unpublished report, Carnegie Mellon University, ECE Dept,1995

[3] C. C. Enz and G.C. Temes, "Circuit Techniques for reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," Proceeding of the IEEE. Vol. 84 No. 11, November 1996

[4] L. Richard Carley, et al., "Single-Chip Computers With MEMS-Based Magnetic Memory", *Journal of Applied Physics*, vol.87, no.9, pt.1-3, p. 6680-5

[5] K. Chun and K.D. Wise, "A High-Performance Silicon Tactile Imager Based on a Capacitive Cell", TRANSDUCERS *'85. 1985 International Conference on Solid- State Sensors and Actuators. Digest of Technical Papers*, p. 445, 22-5

[6] J.T. Kung, R.N. Mills, and H-S. Lee, "Digital Cancellation of Noise and Offset for Capacitive Sensors", *IEEE Trans. Instrum. Meas*,. vol 42, no. 5, pp. 939-942, Oct. 1993

[7] J. N. Babanezhad, "A Rail-to-Rail CMOS Opamp," IEEE J. of Solid State Circuits, Vol   23, no. 6, pp. 1414-1417, December 1988.

[8] N.S. Sooch, "MOS Cascode Current Mirror." U.S. Patent no. 4,550,284, October 1985

Appendix A: Opamp Netlist

```
vvdd vdd 0 dc 3
vvss vss 0 dc 0
Vvmid vmid 0 dc 1.5

m1  3  vi- 1   vss  cmosn w=3u     l=1.2u
m2  4  vi+ 1   vss  cmosn w=3u     l=1.2u
m3  3  5   13  vdd  cmosp w=6.4u   l=1.2u
m4  4  5   13  vdd  cmosp w=6.4u   l=1.2u
m11 1  2   vss vss  cmosn w=3.7u   l=1.2u
m12 2  2   vss vss  cmosn w=3.5u   l=1.2u
m20 13 7   vdd vdd  cmosp w=7.2u   l=1.2u
m21 13 8   vdd vdd  cmosp w=7.2u   l=1.2u
m5  7  6   3   vdd  cmosp w=1.5u   l=1.2u
m6  8  6   4   vdd  cmosp w=1.5u   l=1.2u
m7  7  9   11  vss  cmosn w=1.2u   l=2.4u
m8  8  9   12  vss  cmosn w=1.2u   l=2.4u
m9  11 10  vss vss  cmosn w=1.2u   l=2.4u
m10 12 10  vss vss  cmosn w=1.2u   l=2.4u
*biasnet
m13 5  5   vdd vdd  cmosp w=3.9u   l=1.2u
m14 6  2   vss vss  cmosn w=1.5u   l=2.4u
m15 6  6   vdd vdd  cmosp w=1.3u   l=8u
m16 10 17  vdd vdd  cmosp w=1.5u   l=1.2u
m17 10 9   16  vss  cmosn w=1.2u   l=2.4u
m18 16 10  vss vss  cmosn w=1.2u   l=2.4u
m19 9  9   vss vss  cmosn w=1u     l=12u
m24 9  17  vdd vdd  cmosp w=1.5u   l=1.2u
m22 17 2   vss vss  cmosn w=1.5u   l=2.4u
m23 17 17  vdd vdd  cmosp w=1.5u   l=1.2u
*slew transistors
m25 5  5   3   vss  cmosn w=2.5u   l=1.2u

m26 5  5   4   vss  cmosn w=2.5u   l=1.2u

cload 7 vmid 250f
cload2 8 vmid 250f

ibias  vdd 2 dc  16u
ibias2 5   vss dc 10u
```

Appendix B: Layout

B.1 Opamp Layout

The system was laid out in the HP .5 µm CMOS process. NeoCell, an automated layout tool was used for much of the layout and routing. Figure B.1 shows the layout for the fully differential folded cascode operation amplifier.
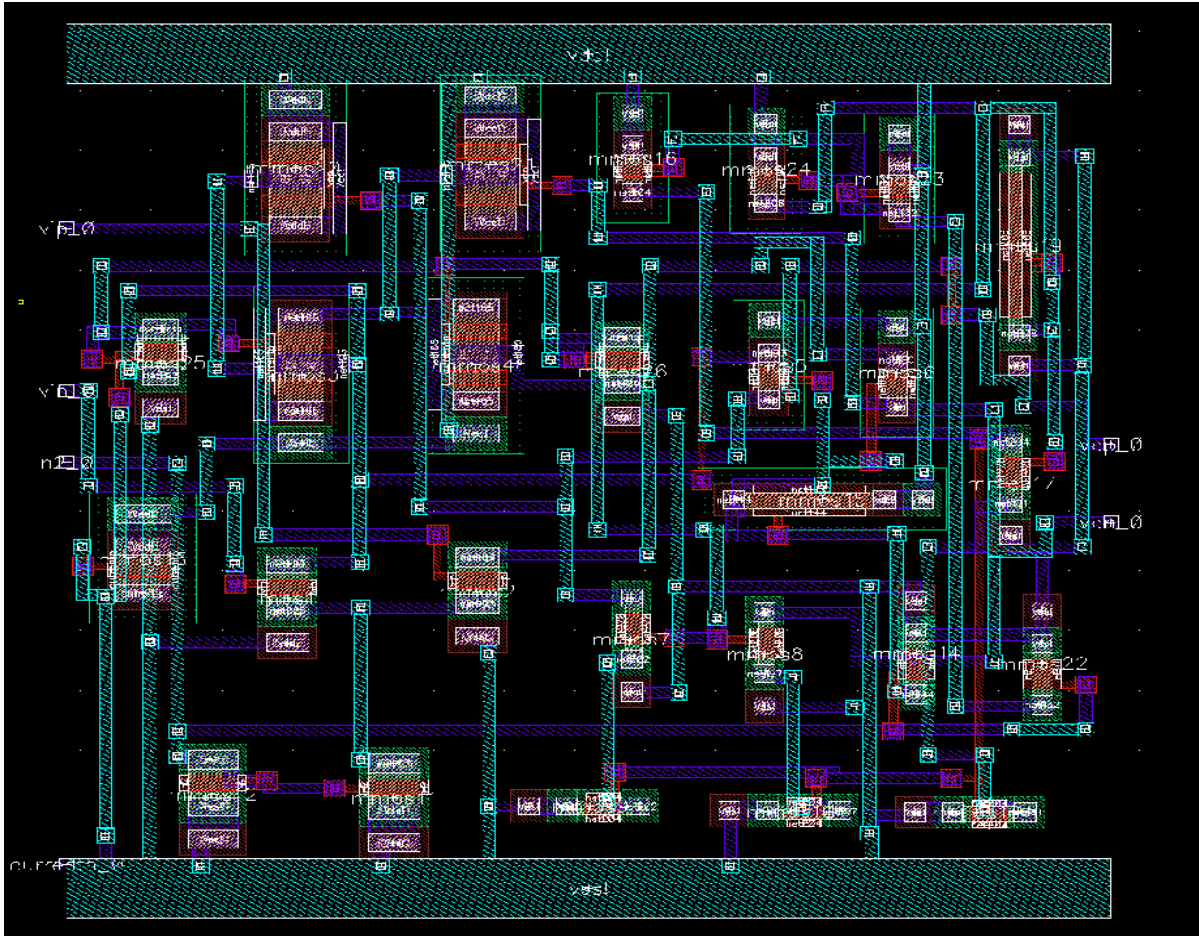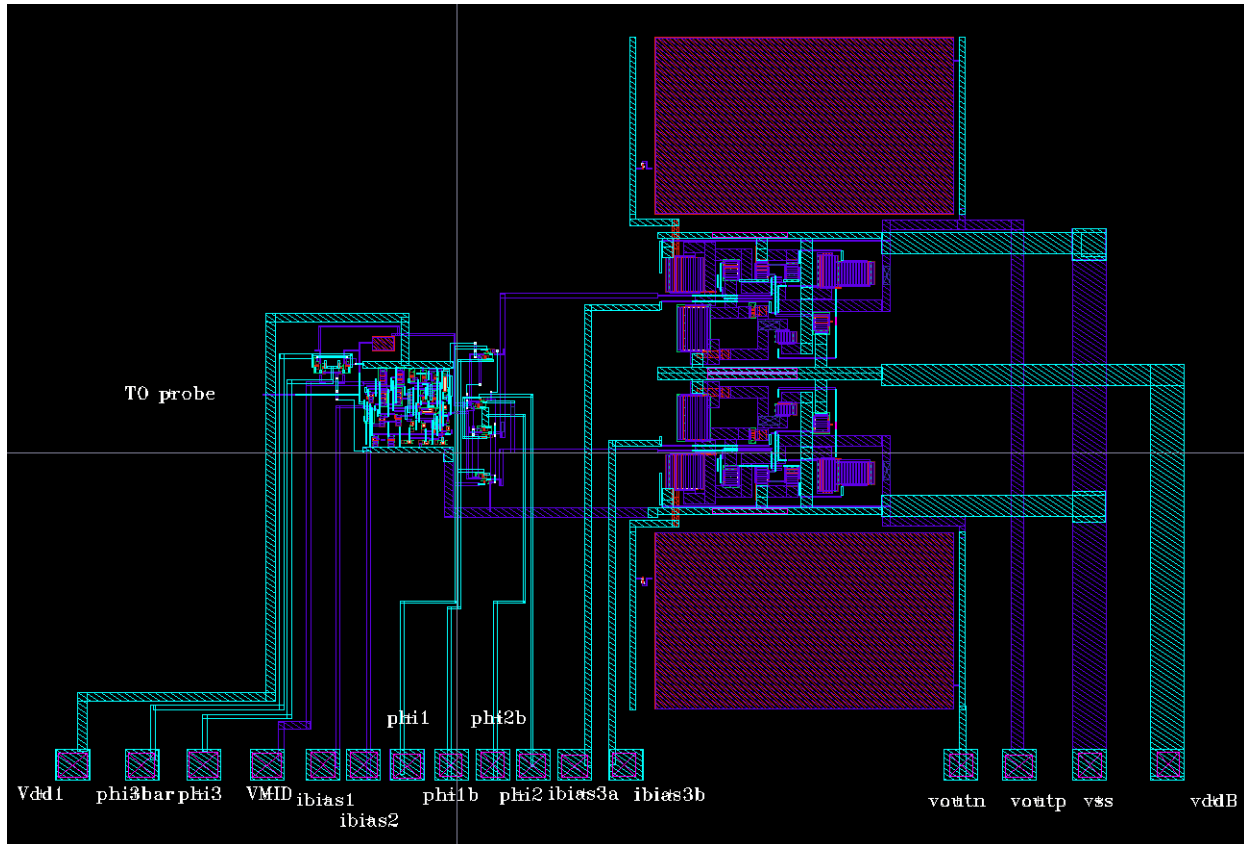

Figure B.1 Opamp Layout

The differential pair device constraint was used for the input transistors, M_1 and M_2. All current mirrors used the current mirror device constraint. All devices and rails were generated with NeoCell. Device placement was done by hand. NeoCell was used for automated routing. This layout is not space efficient, however, it is sufficient for the test chip. The eventual layout for the data storage system would be smaller and the bias network can be laid out separately so that it could be shared among several amplifiers.

The opamp layout can be found with the following path:

/afs/ece/usr/wloeb/neo_thesis/neothesis/opamp1fin/layout

B.2 System Layout

The layout for the entire system is shown in figure B.2.

Figure B.2 System Layout

This layout includes the chopper stabilized capacitive sense amplifier and two buffer amplifiers. The opamp that is used in the system is unable to drive large capacitances, such as the bond pad parasitics. In order to drive the pad parasitic capacitances, a buffer is necessary. Each buffer consists of a Miller-compensated two stage opamp with a source follower. The design of the opamp is not discussed in the body of this paper because it is not part of the Δ capacitive sensing system. Rather, it is part of the test circuit. The buffer's power consumption and die area do not factor into the final system. The schematic for the buffer can be found with the following path:

/afs/ece/usr/wloeb/neo_thesis/neo_thesis/bufferamp/schematic

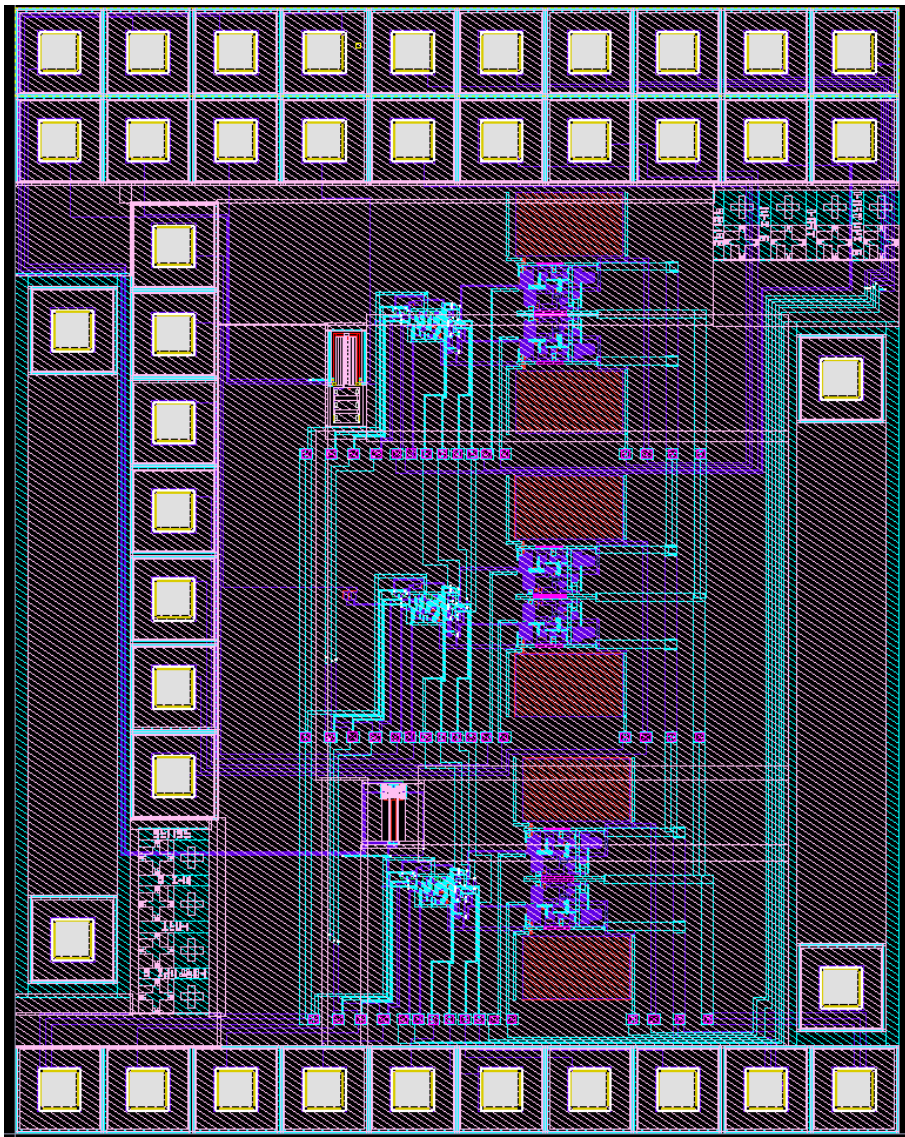The buffer was laid out automatically with Neocell. The buffer layout is available at the following path:
/afs/ece/usr/wloeb/neo_thesis/neothesis/bufferamp/layout

The system layout is available at the following path:
/afs/ece/usr/wloeb/neo_thesis/neothesis/system/layout

B.3 Die Layout

The die layout is shown in figure B.3

Figure B.3 Die Layout

On this die layout, there are three complete variable capacitive sensing systems. The top system is attached to a MEMS probe designed and provided by Mike Lu. The bottom system includes a MEMS probe designed by Dave Guillou [2]. The center system is for self testing and is connected to a fixed capacitor. To use the top probe the die should be released using the standard CMU CMOS MEMS release process. The bottom probe should be released using the CMU CMOS MEMS poly-silicon release process. No release is necessary for the center system.

The complete die layout is available at the following path:
/afs/ece/usr/wloeb/neo_thesis/neothesis/chipver2/layout

B.4 Fabrication Schedule

A layout of this chip was submitted to MOSIS for fabrication on April 3rd 2000. Unfortunately the chip yielded no results due to a layout error in the buffers of the test circuit. This error was corrected and the chip was extracted and simulated. At the time of this writing, the corrected layout is prepared for submission to the September 2000 MOSIS HP .5 μm run.

Appendix C: Testing Setup

This section includes information regarding the electrical testing of the circuit. It does not cover the mechanical placement of the variable capacitive sense amplifier test chip and the media test chip. Testing of the fabricated chip closely follows the simulated test deck. The Hspice simulation test deck is shown below:

```
*Chopper Stabilized Variable Capacitive Sense Amplifier Test Deck
.option ingold=1 post
*include process parameters
.inc mod523_nominal.bsim

*power supplies
vvdd1 vdd1 0 dc 3
vvddb vddb 0 dc 3
vvss vss 0 dc 0
Vvmid vmid 0 dc 1.5


*bias currents
ibias1  vdd1  ibias1  dc 16u
ibias2 ibias2   vss  dc 10u
ibias3a  vddb  ibias3a  dc 350u
ibias3b  vddb  ibias3b  dc 350u

*Capacitor control signal
Vctrl s11 0 SIN(.5 .5 10k 0 0)
Gcs s1 vb VCCAP PWL(1) s11 0 DELTA=.00001 -1v,1f 2,15f

*Vb control
gm7 s1 vmid  VCR PWL(1) phi4 0 0v,100MEG 3v,1m
gm8 vs s1 VCR PWL(1) phi1 0 0v,100MEG 3v,1m
gm8a vs s1 VCR PWL(1) phi2 0 0v,100MEG 3v,1m
 Vb vs vmid PULSE(-.5 .5 0ns 1ns 1ns 998ns 2us)
Vphi4 phi4 vss PULSE(0 3 990n 1ns 1ns 8ns 1us)

*insert circuit netlist here

*clocks
Vphi1 phi1 vss PULSE(0 3 0u 1ns 1ns .99us 2us)
Vphi1bar phi1bar vss PULSE(3 0 0u 1ns 1ns .99us 2us)
Vphi2 phi2 vss PULSE(0 3 1u 1ns 1ns .99us 2us)
Vphi2bar phi2bar vss PULSE(3 0 1u 1ns 1ns .99us 2us)
Vphi3a phi3 vss PULSE(0 3 992n 1ns 1ns 4ns 2us)
Vphi3bar phi3bar vss PULSE(3 0 992n 1ns 1ns 4ns 2us)

.option gramp=9
.op

.tran .1u 300u
.end
```

Each input and output node has a pad associated with it. First, one must choose which of the three systems on the die is to be measured and post-process the chip accordingly. Also bond wires must be attached to the pads of that system. Bonding pads are labeled on the die layout.

To set up the chip for measurement, it is useful to rely on the Hspice test deck as a guide. This setup procedure will walk through the Hspice test deck and discuss the analogous physical connections.

The four power supplies, *Vdd1, Vddb, Vss*, and *Vmid*, can be provided by laboratory dc power supplies. There are separate positive rails for the variable capacitive sense amplifier and for the on-chip buffers so that the power consumption of the system can be measured without including the power consumption of the buffers. *Vdd1* is the positive supply rail for the system; *Vddb* is for the buffers. Both of these should be attached to 3 volt supplies. *Vss* is the common ground for the entire die. It should be grounded with respect to the 3 volt supplies. *Vmid* should be set at 1.5 volts.

There are four bias currents for each system that must be set, *ibias1, ibias2, ibias3a*, and *ibias3b*. The simplest way of providing these bias currents is by attaching resistors between the bias current nodes and an appropriate supply rail. Variable resistor boxes or potentiometers can be used to "dial in" the resistor value until the correct current is flowing through them. A resister should be placed between the *ibias1* node and *Vdd1*. A second resistor should be placed between the *ibias2* node and *Vss*. Finally resistors should be placed between the *ibais3a* and *ibias3b* nodes and *Vddb*.

The variable capacitor control signal is used only for simulating a variable capacitor. It should not be used for testing. Rather an actuation signal should be applied to the Z actuation terminal of the probe that is being tested.

The elements listed under *Vb* serve to create the modulation clock. The clock is a square wave that is interrupted during the reset phase of the system. During the reset phase interruption the modulation signal should be held at Vmid. This clock can easily be generated by using one channel of a LeCroy 9210 pulse generator.

The system clocks are described by Vphi1, Vphi1bar, Vphi2, Vphi2bar, Vphi3, and Vphi3bar. These clocks can be programmed and generated by a pair of Lecroy 9210 pulse generator. The clocks should be programmed to match the clocks generated by the Hspice test deck.