

Design of a MEMS-Based Capacitor for Radio Frequency Applications

Masters Project Thesis

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1. Introduction

As the world relies more and more on information technology and quick access to data, radio frequency (RF) technologies for fast wireless data transfer and communications will become increasingly significant. With the continuing push to integrate complete systems on a single integrated circuit (IC), RF design has become increasingly difficult. One challenge in RF IC design is the implementation of on-chip passive devices such as inductors and capacitors with high quality factors. In order for tuned RF circuits to perform well and have good selectivity, linear high Q passive devices are required. While it is possible to get reasonably good Q factors from on chip capacitors comprised of metal-metal layers, on-chip inductors are still difficult to implement, only allowing for Q factors of 5 to 10 [1]. In addition to their poor Q-values, on-chip inductors also take up a large area, prohibiting the design of on-chip inductances greater than 10nH. Although active circuits can sometimes be used to synthesize inductors with better Q factors, they tend to have higher noise, distortion, and power consumption. Bondwire inductors offer high quality device characteristics but are not well controlled [2]. One advantage of bondwire inductors is that they offer very high Q values (on the order of 50 at 1GHz). Unless the bonding process is tightly controlled, bondwires can end up being different lengths ultimately resulting in different values of inductance. As a result, circuits using bondwire inductors must be designed to handle these variations, and hence tend to get fairly complex. In practice, use of these inductors requires a wide range capacitive tuning element.

Several strategies have been used to achieve wide tuning range, which include the implementation of MOS varactors or banks of capacitors that are switched into or out of circuit. While these approaches do work and are used in many current designs, they tend to have some performance drawbacks and a limited tuning range. Distortion and linearity are the two main problems associated with these approaches. In the case of MOS varactors [3], the devices are fairly large in order to permit wide tuning ranges. In addition to the area usage, their capacitance value of a CMOS varactor changes significantly with the voltage applied across the varactor. In the case of an oscillator, the voltage across the varactor is constantly varying. Thus, the value of the capacitance is changing during these voltage

swings, so distortion and frequency drift (jitter) are a problem. There has been some investigation into designing better varactors [4], but the improvements have only been marginal.

The second popular approach for achieving a wide tuning range, switching in or out banks of capacitors, also suffers from similar problems. While the fixed capacitors themselves offer good performance, the problem with this approach lies in the switches. Since switches are built from transistors, they generate noise and can behave nonlinearly when faced with large signal swings. Low frequency flicker noise and thermal white noise are reflected up to and around the VCO's center frequency, causing poor phase noise performance. Good switches can be designed, but this usually means that a great deal of die area must be spent in order to build switches with low on resistance, low noise, and immunity to large signal swings.

When these switches are switched on or off, charge injection from the switches can cause additional phase and frequency glitches in the oscillator waveform. Finally, due to the digital nature of this approach, only discrete values of fixed capacitance can be switched in or out of circuit (the tuning characteristic is nonlinear). However, this limitation can be offset with the use of an additional small varactor.

For these reasons, this project investigates the feasibility of a MEMS-based continuously tunable variable capacitor tuning element. Bondwires can be used as the oscillator's inductor, to offer a very high Q and low phase noise as mentioned previously. The capacitor design will limit the effect of bondwire variability because of the wide tuning range offered by the capacitor. An on-chip variable MEMS capacitor will be implemented that will be part of the voltage controlled oscillator's resonant tank. The MEMS capacitor will offer a high quality factor, wide tuning range, and excellent linearity. The capacitor is a novel thermally controlled parallel-plate device built over the linear capacitor well layer in the Hewlett-Packard/Agilent 0.5 μ m process available through MOSIS. The device is released using the CMU MEMS poly-release process.

This report describes the design of the MEMS capacitor, VCO circuitry, low frequency test circuitry, and the layout of the test chip. A section with measurement results and a brief conclusion will then follow these sections. Appendices provide MATLAB scripts and code.

2. MEMS Capacitor Design

We considered several approaches while designing a suitable MEMS capacitor for this application. These approaches included both ‘traditional’ electrostatically actuated devices (z-plane and comb-drive) as well as less traditional thermally actuated devices. Initially, an electrostatically actuated capacitor looked fairly straightforward to implement, but further investigation revealed significant complexity for this application. A thermally actuated device was therefore chosen because it offered simpler implementation, easier control, better performance, and a smaller die area, at the expense of power consumption.

2.1 Comparison

Initially, two electrostatically actuated capacitors were compared. These capacitors were based on designs that have been used in previous work at Carnegie Mellon and have proved successful in the CMU MEMS poly-release process. Electrostatically actuated capacitors offer very low power consumption for position control. Because it has no static power dissipation, a DC bias voltage is all that is required to hold the capacitor in position. Power consumption is low for the capacitor alone, however the control circuitry needed to generate the position control voltages can use a significant amount of power, resulting in lower efficiency.

The first capacitor design considered here is a standard comb-drive type. In this kind of capacitor, fixed comb fingers surround a movable plate with inter-digitated comb fingers, as shown in Figure 1.

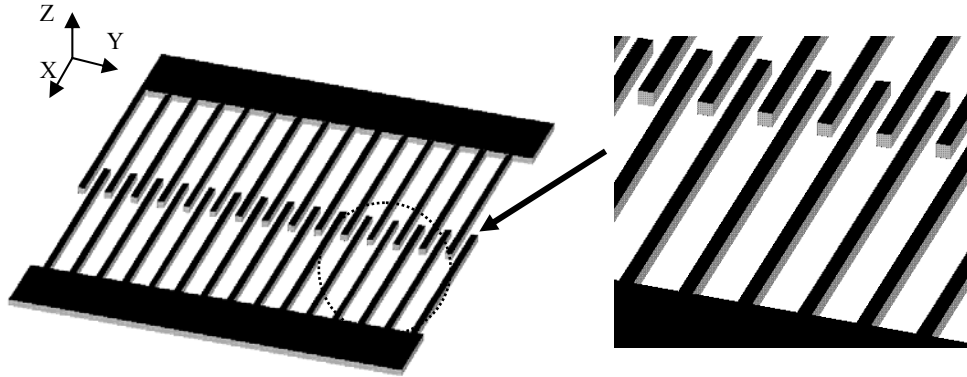


Fig. 1: Comb drive actuator and close-up

Since it is easy to separate the low frequency actuation control signals from the VCO's high frequency signals by assigning these signals to different groups of fingers, this capacitor structure has low parasitic coupling between the control and high frequency nodes. There are at least two metal layers also available for use on the MEMS structure, so the parasitic resistance can be low, resulting in a high Q-factor. Finally, capacitors of this type are easy to control, and have a tuning characteristic below mechanical resonance of $\Delta x \propto V^2$. Because the only thing that changes during the motion of the device is the area of overlap between the comb fingers, the capacitance can be approximated as follows:

$$C(x) \approx \frac{\epsilon_o L x}{gap}, \quad (1)$$

where L is the width the finger and x is the amount of overlap. However, this implementation has a very low capacitance per unit area. This problem is exacerbated by the curling of the structure upon release [5], causing the comb fingers to be misaligned in the z -axis. The tuning range of this structure would therefore be extremely limited, and a very large structure would be required to meet the desired requirement of a wide tuning range. For these reasons, this solution was abandoned.

The second type of electrostatically actuated device considered here is the z -plane parallel-plate capacitor, shown in Figure 2. This device is built over a linear cap well in the HP/Agilent $0.5\mu\text{m}$ process and offers excellent capacitance per unit area, but has even more negative drawbacks than the comb-drive actuator.

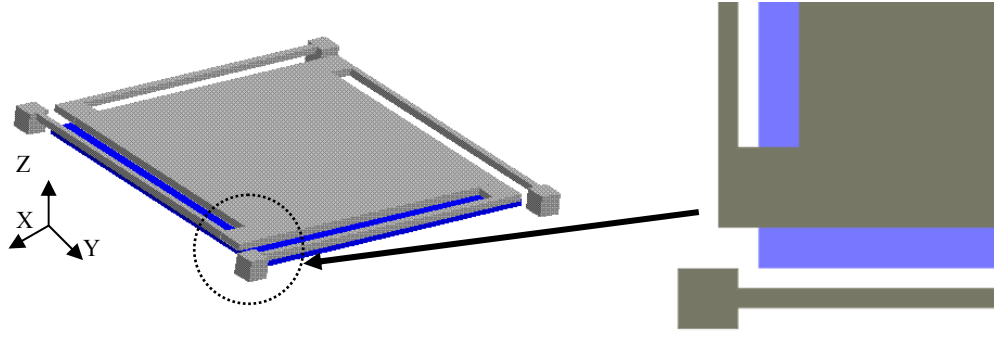


Fig. 2: Z-plane capacitor with close-up

First, a device in this configuration has a non-linear control voltage to capacitance relationship. The ‘control voltage’ is a low frequency voltage signal applied to the plates of the capacitor where $\Delta z \propto V^2$. The capacitance is proportional to the inverse of the distance between the capacitor plates,

$$C(z) = \frac{\epsilon_o A}{z}, \quad (2)$$

where A is the plate area in x and y and z is the distance between the plates.

Second, the parasitics on the upper and lower plates of the capacitor are different, and it is therefore impossible to implement a balanced capacitor as is. While it is possible to operate it in a quasi-differential manner (bottom plate is small-signal ground and the top plate is separated into two separate matched capacitors), it would require matching to be extremely good between the two halves of the capacitor. In order to achieve this, a very complex control system would need to be implemented to control the height of the capacitor from the bottom plate. Third, when released, the top plate of the capacitor will curl upward. Due to deviations in spring stiffness and material properties, it is highly likely that it will not sit evenly in Z, and the two capacitances would differ greatly. Assuming a square plate, and uniform curling (i.e. the center of the plate is at the lowest point in Z), it would be best to sense and servo the plate at all four corners, as shown in Figure 3.

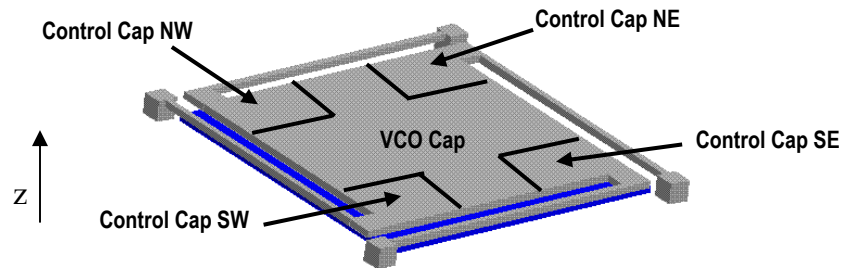


Fig. 3: Z-plane capacitor with control sections

The complexity of implementing four well matched circuits for controlling the four corners of the plate (Figure 4) as well as the parasitics and coupling that would result from getting the control signals and the VCO signals onto the plate through the four springs would result in a severe degradation in Q and overall performance.

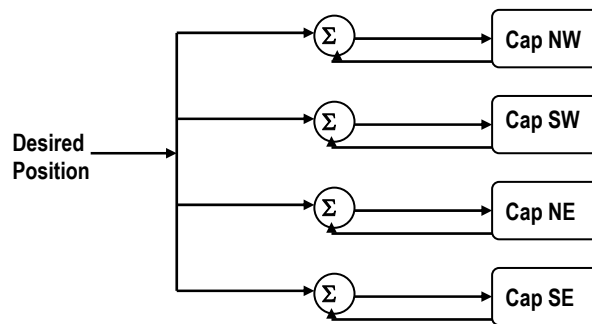


Fig 4. Z-plane control block diagram (simplified)

It should also be noted that both the comb-drive as well as the z-plane actuator types generally require high drive voltages, sometimes greater than 5V for positioning purposes. This is difficult to achieve in a standard 5V CMOS technology, and would generally require a high voltage process as well as a charge pump to generate these higher voltages.

Thermally actuated capacitors offer a much simpler overall system complexity than electrostatically actuated devices and are therefore easier to implement. Drawing on the advantages of the z-plane electrostatically actuated capacitor (good capacitance per unit area), and the fact that all of a single metal layer can be used to carry the VCO signal; higher Q and better RF performance are a result. Heating a resistive serpentine built on top of the

upper plate actuates the structure by causing it to deflect downward, increasing the capacitance. While not as efficient on power and somewhat slower mechanically than an electrostatic actuator, the advantages of good RF performance outweigh these minor disadvantages.

In conclusion, an electrostatically actuated capacitor is not suitable for this type of application due to the complexity of a control system and poor performance. A thermally actuated capacitor meets the necessary electrical requirements and keeps implementation straightforward. The design of a thermally actuated capacitor is discussed in the next section.

2.2 Capacitor Design

The concept of our thermally actuated capacitor is as follows. Using the property that a cantilevered structure fabricated in the laminated CMOS MEMS process bends upward after being released, we use this as the base minimum capacitance. The upper plate of the capacitor is made out of Metal 1, and Metal 2 is used to create a serpentine resistive heating element on top (Figure 5). When current is passed through the serpentine, it heats

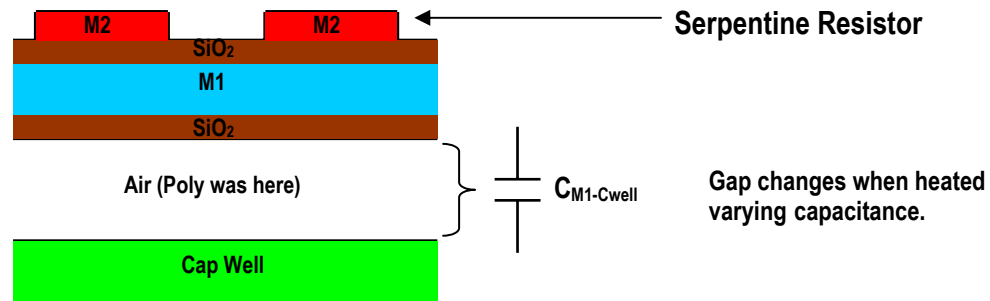


Fig. 5: Cross Section of Capacitor

the entire structure. Increasing the temperature of the structure causes it to bend downward, as shown in Figure 6. As a result, the capacitance increases [6].

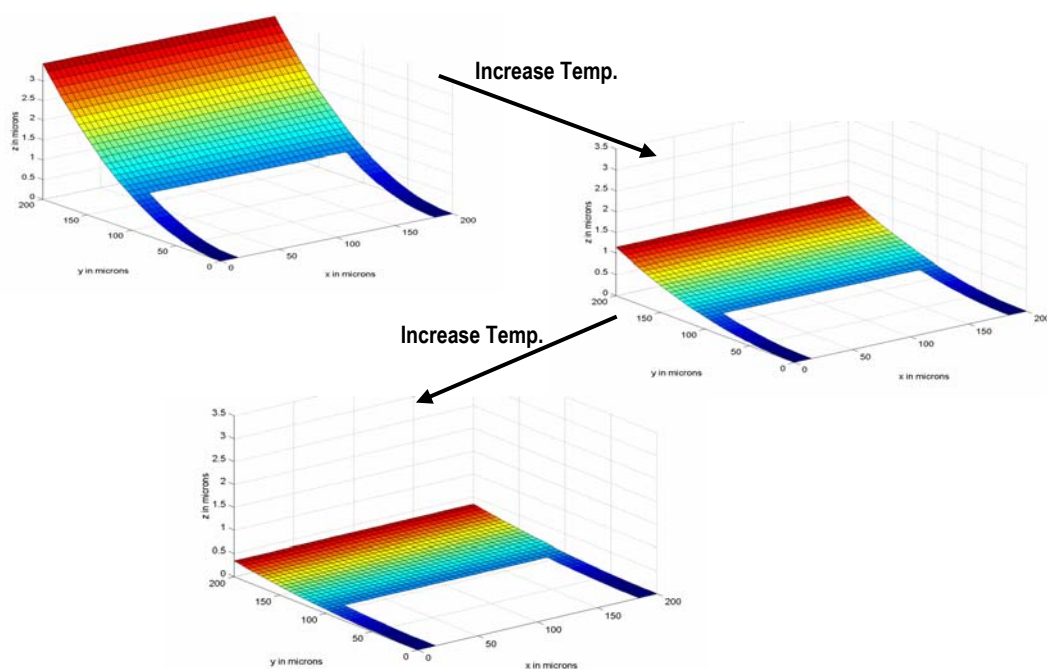


Fig. 6: Capacitor thermo-mechanical response

2.2.1 Design Tradeoff Analysis

Several tradeoffs have to be considered in order to design a capacitor that meets the required mechanical, thermal, and electrical specifications. For this capacitor design, these requirements all eventually lead to the spring design (Figure 7). Because the electrical characteristics of this capacitor are a primary design goal, they were taken into consideration first. After the electrical design goals were determined, a layout was generated and some simulations were run to verify performance. When the design met the electrical specifications, mechanical and thermal properties were checked and verified.

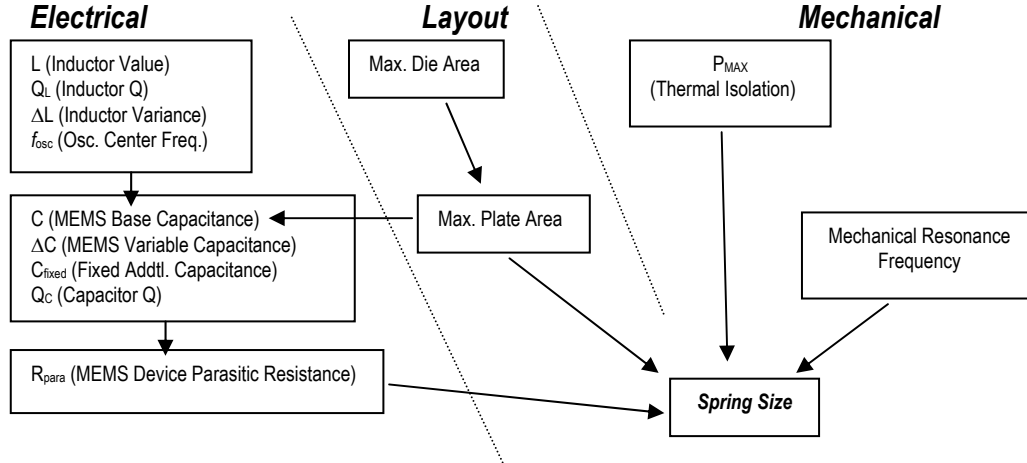


Fig. 7: Design tradeoff tree

2.2.2 Electrical Properties

The capacitor primarily needs to meet the electrical requirements for good RF performance (high Q and good linearity). High Q is needed in order to ensure that our oscillator has a very sharp peak at its center frequency. This guarantees that the oscillator will stay near that frequency and filter out other unwanted harmonics. It was determined from simulations (§2.2.3) that the springs were the dominant contributors of series resistance in the circuit, and hence the dominant factor of determining the Q of the device. Because of the decision to use high- Q bondwire inductors as part of the LC tank in the VCO, it isn't all that necessary for the capacitor to have an extremely high Q factor. Given that the bondwires have a Q of approximately 50, a device Q of 80-100 is reasonable in order to have enough overall tank Q and hence reasonable power consumption. Using the equation:

$$Q = \frac{1}{\omega_0 RC}, \quad (3)$$

for a series RC circuit, it was found that a tolerable spring resistance was 8 ohms at a center frequency of 1GHz. This maximum resistance sets the maximum suspension length, which in turn defines the mechanical and thermal properties of the device. The mechanical and thermal properties will be discussed for the final design of the capacitor (see section 2.2.4).

In order to have a reasonably wide tuning range; we must attain a certain ΔC , the MEMS variable capacitance. The LC tank in the oscillator determines its frequency of oscillation from the following equation:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \quad (4)$$

The total capacitance needed with 4nH bondwire inductors in the tank is approximately 6pF. Obviously our MEMS capacitor will not meet this requirement, so a fixed capacitor will be needed and implemented using highly linear, high Q metal-metal capacitors on chip. The variable MEMS capacitor is designed to give a ΔC of 200fF, which at a center frequency of 1GHz corresponds to a tuning range of approximately 20MHz.

Note that originally we were aiming for a VCO design with a center frequency of 2.4GHz, at which this capacitor would give us a frequency tuning range of roughly 200MHz. Due to the limited f_T of the HP 0.5 μ m process (approximately 1.3GHz according to my calculations and simulations), it was necessary to lower the operating frequency of the circuit down to 1GHz because the transistors would not operate at 2.4GHz. At this lower frequency, this ΔC gives us a much more limited tuning range, as can be seen. Note that the capacitor can be redesigned to be larger and hence give us a larger tuning range at this frequency. However, due to the cost of silicon ‘real estate’, MEMS mechanical/thermal CAD simulations, and post-processing complexity, it was decided that leaving the capacitor at this size and taking measurements on a smaller range would be adequate for proof of concept purposes.

The MEMS capacitor will yield very good linearity since none of the capacitor values change with the signal voltage applied. Since the mechanical time constant is much greater than the 1GHz RF signal, the capacitor stays in position and its capacitance is held constant, and as a result it has excellent linear behavior.

In order to meet the required ΔC and Q factor determined above, a plate size of 100 μ m x 200 μ m was chosen for the MEMS capacitor. The springs were sized to be 100 μ m x 10 μ m to undercut our maximum allowable R by a factor of 10. Layout of these devices was completed in Cadence and some simulations were run to verify performance.

2.2.3 Device Layout and Simulation Methodology

Two electrically equivalent versions of the capacitor were created. The first design looks similar to a paddle, with springs attached to the two front corners. The other design is a torsion bar structure with the springs attached on the sides (see Figure 8). Both devices have a plate size of $100\mu\text{m} \times 200\mu\text{m}$ and spring size of $100\mu\text{m} \times 10\mu\text{m}$.

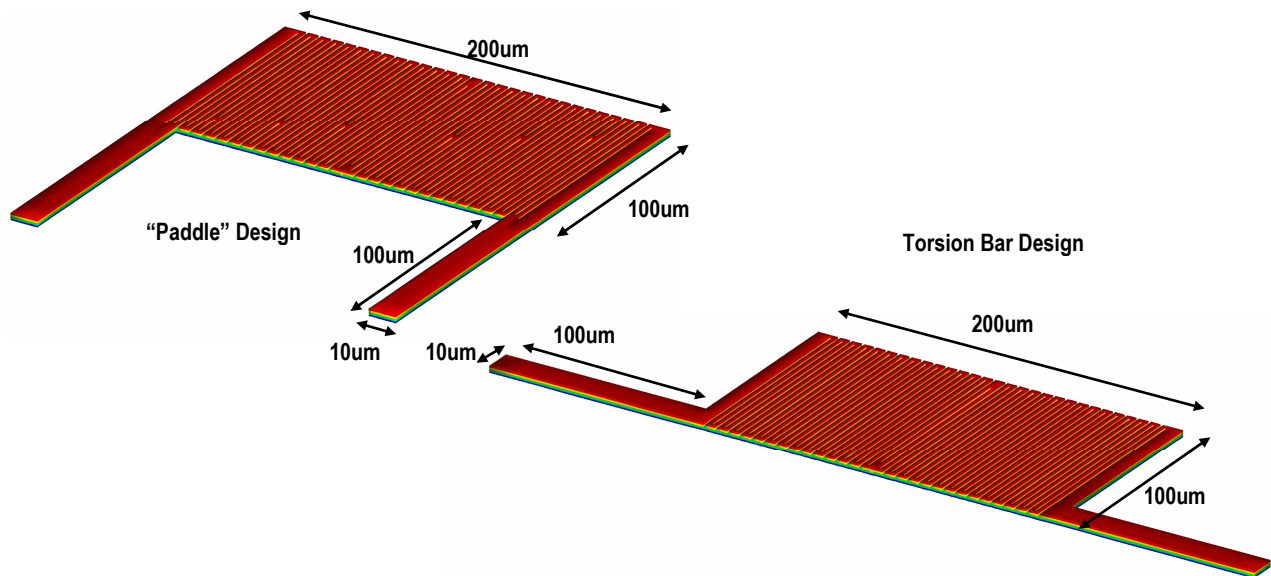
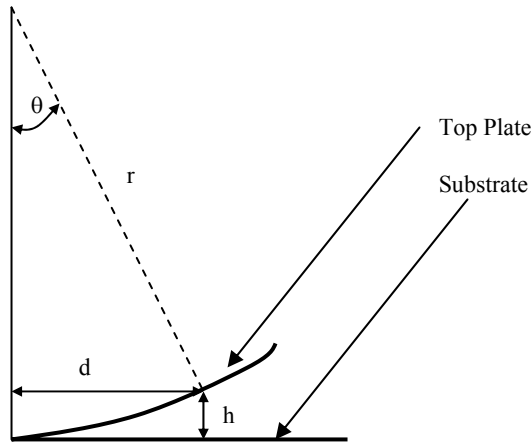


Fig. 8: Capacitor Layouts

In order to accurately simulate the electrical properties of the capacitor, it was necessary to find out how much the capacitor would curl when released. The radius of curvature determines exactly how much our structure will curl when released. Using data and information from [5], we were able to get a first order estimate of this curl. Assuming our structure had a radius of curvature that would approximate the largest beam experimentally measured in [5], we were able to come up with the simple model and equations (Figure 9), which were subsequently used in the design process of the capacitor.



$$\theta = \frac{360 \cdot d}{2\pi r} \cdot \frac{\pi}{180}$$

$$h = r \cdot (1 - \cos(\theta))$$

Fig. 9: Radius of Curvature Modeling

Using this information for how our structure would curl, it was now possible to accurately model the electrical characteristics of our MEMS capacitor. We wrote a MATLAB script (see Appendix A) to assemble a Spice netlist that models the distributed behavior of our device. A unit cell (Figure 10) models the distributed capacitance and resistance seen between all layers of the structure. The MATLAB program takes the plate size, spring size and radius of curvature and assembles many instances of the unit cell into a large distributed network that reflects the actual electrical and mechanical structure of the real capacitor, including the height of the top plate due to curl. The netlist produced also models the bottom plate (Cap well and substrate layers) of the capacitor and its distributed parameters and termination.

The capacitance of interest, C_{M1_Cwell} , is the variable air-gap capacitor in the MEMS device. Due to the two dielectrics (SiO_2 and air), this capacitor is actually comprised of two capacitors in series; one fixed metal-to-air capacitor (oxide dielectric) and one air dielectric oxide to cap well capacitor (see Figure 11).

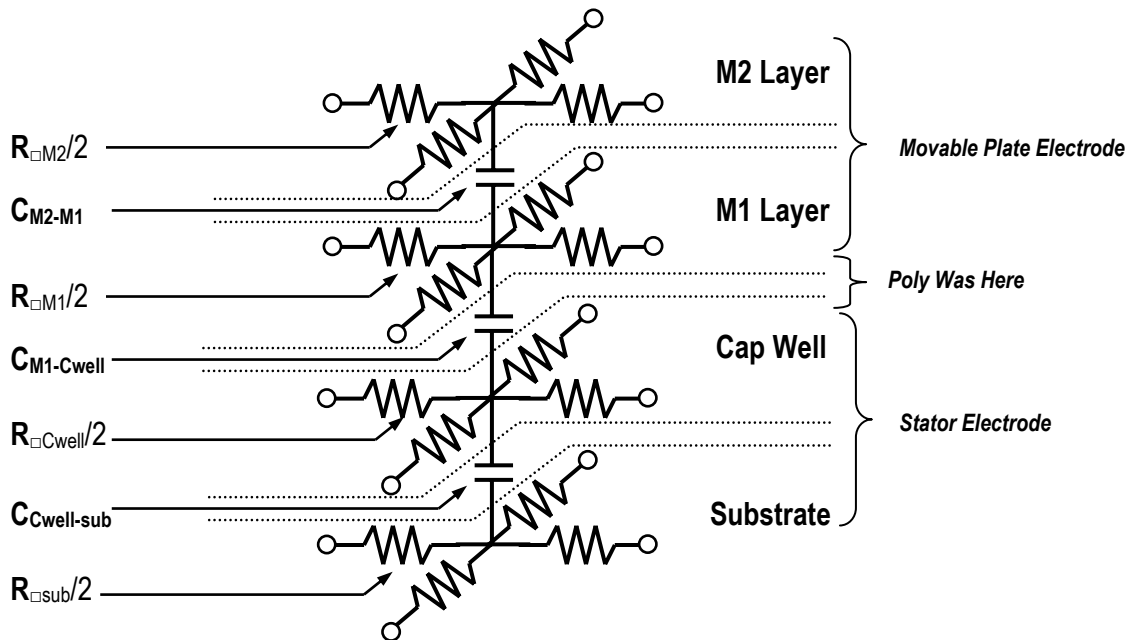


Fig. 10: Unit cell for electrical simulation of MEMS capacitor

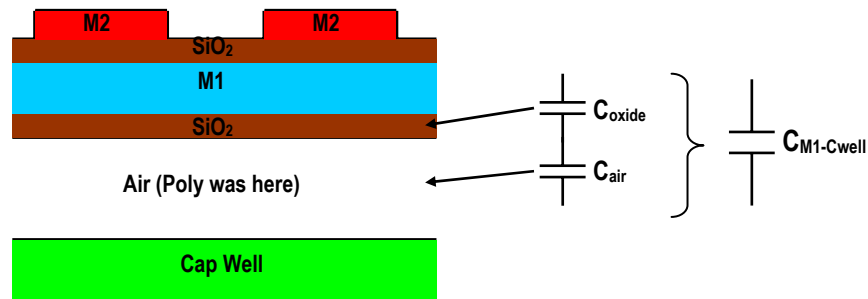


Fig 11: Cross section of thermally-actuated MEMS variable capacitor

The initial design of our MEMS capacitor was simulated and checked for the designed electrical characteristics. Preliminary simulations and results looked favorable and were close to hand calculated estimates. As an added precaution, a few additional devices were simulated using the MATLAB scripts to insure that our models were accurate. Simulated results for capacitance and Q of these devices again closely matched hand calculations, so we were confident that the program was producing good results.

After these simulations were carried out, some more thermo-mechanical simulations were run using the CoventorWare MEMCAD tool. CoventorWare is a flexible CAD package that simulates mechanical, thermal, and electrical properties of micro-machined structures. With

it, it was possible to verify the radius of curvature estimates and get a better picture of exactly how our structures would deform mechanically when released. Simulation results confirm that increasing the structure's temperature causes it to bend downward as desired. Some results from the CoventorWare tool are shown in Figure 12.

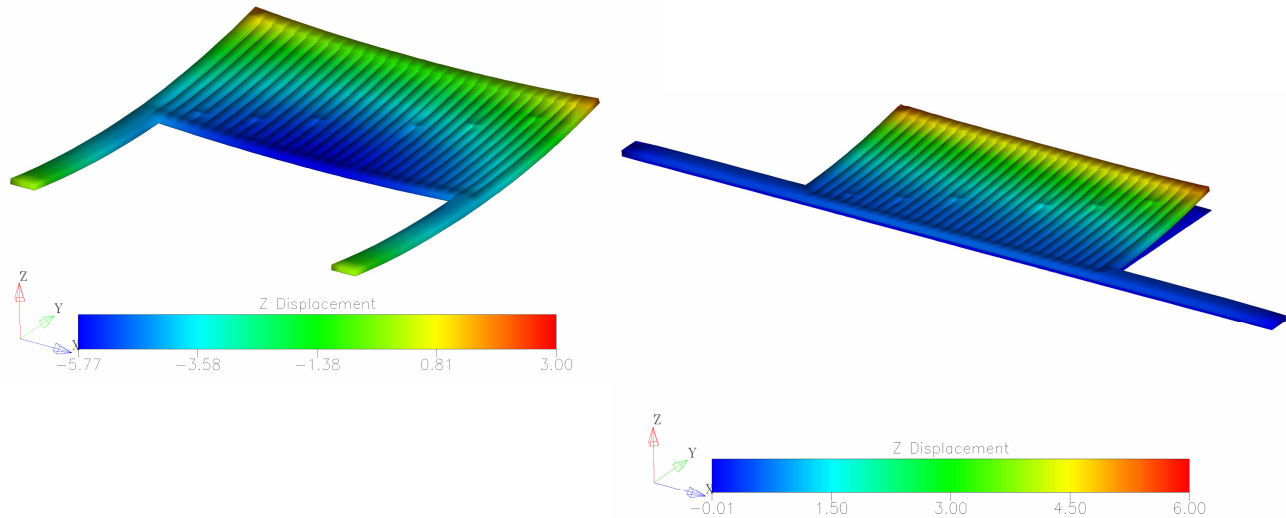


Fig. 12: CoventorWare simulation results (structure shape at room temperature)

It should be noted that for the “paddle” design, the displacement indicated in Z shows a negative value. For some reason, the CoventorWare simulator does not take into account reaction force from the substrate. As a result, the capacitor actually ‘breaks through’ the bottom plate (substrate) in the simulation. The lowest portion of this capacitor (at $-5.77\mu\text{m}$) should actually be at $0\mu\text{m}$. For this reason, the shape of our released “paddle” structure will probably be different in reality, and we should consider the results for this case inaccurate.

Several simulations were run to try and extract the actual capacitance of the device after the mechanical simulations were run. Due to limitations in the tool, it wasn't possible to get these results, but since the curvature of the CoventorWare simulations were close to the MATLAB results, a good estimation was made from the simplified model. (Figure 13).

After these simulations were completed, the device's thermal and mechanical properties were checked to insure that they were reasonable.

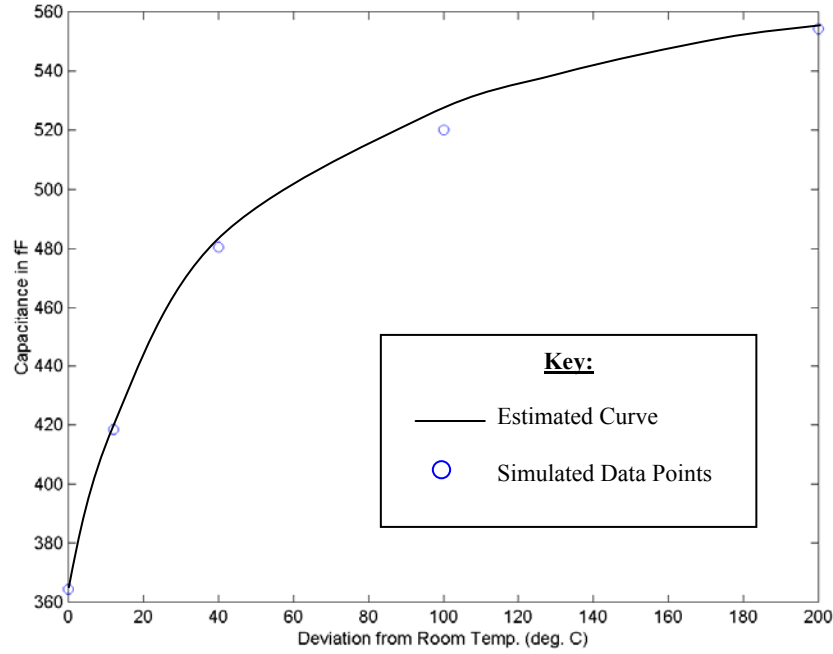


Fig. 13: Capacitance vs. Plate Temperature

2.2.4 Thermal and Mechanical Properties

Thermal resistance was considered in order to determine how much thermal isolation was provided by the springs in the capacitor structure. This is important to insure that a reasonable amount of power is spent to heat the device rather than letting it escape through the springs to the rest of the chip. Although our springs are composed of both aluminum and silicon dioxide, in a laminated structure, the aluminum is much more heat conductive than silicon dioxide. Aluminum has a thermal conductivity $\rho_{th}=2.36\text{W/cm}^\circ\text{C}$. Since the thermal resistance of the springs can be determined by:

$$R_{th} = \frac{l}{2\rho_{th}wh}, \quad (5)$$

where w is the width ($10\mu\text{m}$) of the spring, h is the thickness (14000\AA) of the Metal 1 layer, and l is the length ($100\mu\text{m}$) of the spring. The factor of 2 in the denominator reflects that there are two springs. The thermal resistance is 12000°C/W , which is comparable to results

given in [7]. In order to heat our structure 200°C, the amount of power needed in the heater is determined by:

$$P_{heater} = \frac{T_{plate} - T_{ambient}}{R_{th}}. \quad (6)$$

A 15mW heater would be needed to meet this specification. For a 5V power supply, a heater resistance of 230Ω is required. The serpentine resistor was laid out to meet this requirement.

The mechanical resonance frequency is determined by the equation:

$$f_{o-mech} = \frac{1}{2\pi} \sqrt{\frac{k}{m}}, \quad (7)$$

where k is the spring constant and m is the plate mass. The spring constant, k is

$$k = \frac{Ewh^3}{4L^3}, \quad (8)$$

where E is Young's modulus, w is the width of the springs (10μm), h is the thickness of the springs (28500Å), and L is the length of the springs (100μm). The mass of the plate is given by:

$$m = dabh, \quad (9)$$

where d is the density of aluminum (2760kg/m³), a is the plate width (200μm), b is the plate height (100μm) and h is the plate thickness (28500Å). This results in an $f_{o-mech} = 35$ kHz.

With a 10G shock, the device will deflect according to

$$\Delta x = \frac{10g}{(2\pi f_{o-mech})^2}, \quad (10)$$

where g is 9.8m/s². The deflection is 20.6nm. If the device was to be servoed in a feedback loop, the loop should have a bandwidth of about 1MHz to control microphonics and ultimately be above mechanical resonance.

2.2.5 Final Design Characteristics

The properties of the final capacitor are reflected in the following table:

MEMS Capacitor Characteristics

Plate Size	200 μ m x 100 μ m
Spring Size	100 μ m x 10 μ m
Base Capacitance (Total)	360fF
Variable Capacitance Range	+200fF
Q factor (actual)	510
Max Height (Room Temp.)	3.5 μ m
Height at 200°C	0.4 μ m
Thermal Resistance	12kW/°C
Mech. Resonant Freq.	35kHz
10G Shock Displacement	21nm

3. Test Circuit Design

We designed two test circuits to evaluate the performance of the MEMS ΔC capacitor. One was a 1GHz RF VCO, and the other a low frequency sawtooth oscillator. Both circuits would allow us to measure the change in capacitance our MEMS device provided.

3.1 VCO Circuit Topology and Design

The circuit topology chosen for this VCO design is that of a standard cross-coupled complementary latch. This particular architecture was chosen because of its relatively good phase noise performance, ease of implementation, and differential operation [8]. While phase noise was not a primary concern in this particular project, we still wanted to have good phase noise performance so that experimental measurements could be taken accurately. The latch is driven by a tail current source and is loaded differentially with an LC tank circuit. The tank consists of a pair of bondwire inductors connected differentially and a fixed capacitor and one half of the upper plate of the variable MEMS capacitor on each side of the circuit. The fixed metal-metal capacitors are sized to give the extra capacitance needed that is not provided by the latch transistors or MEMS capacitor for the appropriate 1GHz resonance frequency. The MEMS capacitor and bondwires are modeled using macro-models of the actual devices themselves. This speeds up simulation time and gives fairly accurate results. The schematic is shown in Figure 14.

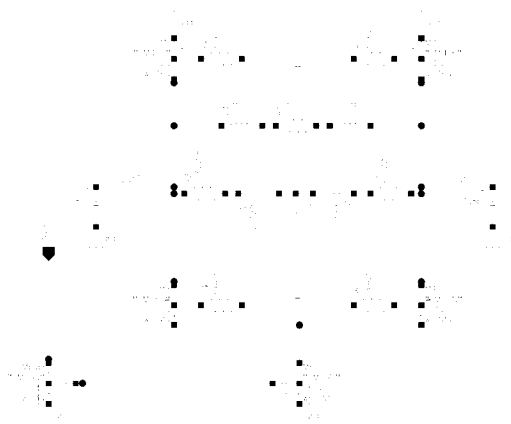


Fig. 14: VCO Core Schematic

According to Lee and Hajimiri [8], the L and C of the tank cancel at resonance leaving the parallel transformed series resistances of the inductor and capacitors. Harmonics of the input current are strongly attenuated by the LC tank and the output spectrum is mainly that of the fundamental. The tank amplitude in this current limited regime of operation can be approximated by:

$$V_{\text{tank}} \approx I_{\text{tail}} R_{eq} \quad (11)$$

In order to get a decent swing to drive the inverters that followed, it is necessary to force the transistors to switch back and forth quickly. The latch transistors were sized to give a transconductance of approximately 8mA/V when all the current is in one side of the latch. This transconductance would give us enough gain to keep the oscillator ringing. The tail current source was sized to have a reasonable gate drive ΔV_{gs} to insure strong saturation and good performance during oscillation. The circuit is biased externally using a resistor. Initial simulation results were good and the transistor sizes were adjusted slightly to produce a symmetrical waveform with low distortion. Simulation results can be seen in Figure 15 below.

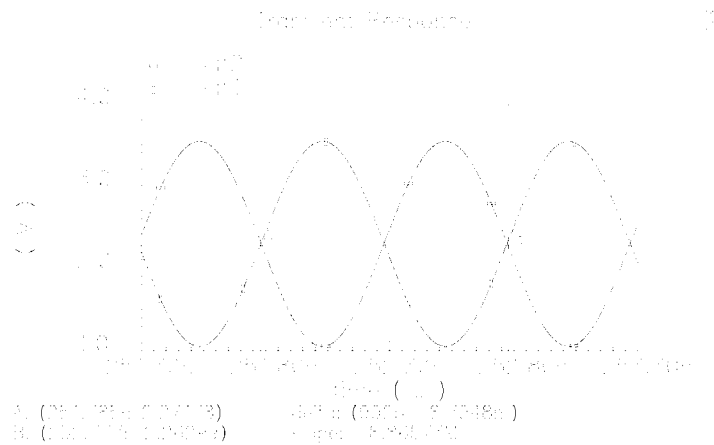


Fig. 15: VCO Core simulation results ($f_{\text{out}} \sim 1\text{GHz}$)

By varying the voltage across the heating element in the MEMS capacitor, the capacitor heats up and deflects downwards causing it to change its capacitance and hence the output frequency. The simulated tuning range is from 997MHz to 1.022GHz.

Note that in order to produce more accurate simulation results, a gate resistance was added to augment the BSIM3v3 models. Recent studies have started addressing the suitability of BSIM3v3 for RF and high frequency operation [9]. Because of the MOSFET's distributed behavior at high frequencies, it is necessary to model the distributed channel and gate resistance in each device. Fortunately, the added lumped gate resistance models these effects fairly accurately. This was added to the gates of the latch transistors used in the circuit.

The output of the VCO cross-coupled latch drives several cascaded inverters that are sized to appropriately drive the pads on the chip. The outputs are also fed into several D-latch dividers to offer a low frequency output waveform. These circuits consist of standard digital logic cells with some sizing adjustments and are therefore not included.

Simulations of these circuits show good performance with good margins for process variations. The circuits also passed all process corner simulations. The signals produced by this circuit will go off chip to an external VCO Analyzer and Spectrum Analyzer for testing and measurement.

3.2 Low Frequency Test Circuit Design

Because of the risk associated with the startup of high frequency RF circuits, an additional low frequency circuit was designed to test the change in capacitance the MEMS capacitor provides. It consists of a simple sawtooth oscillator circuit with some digital "glue" logic. A schematic is shown in Figure 16.

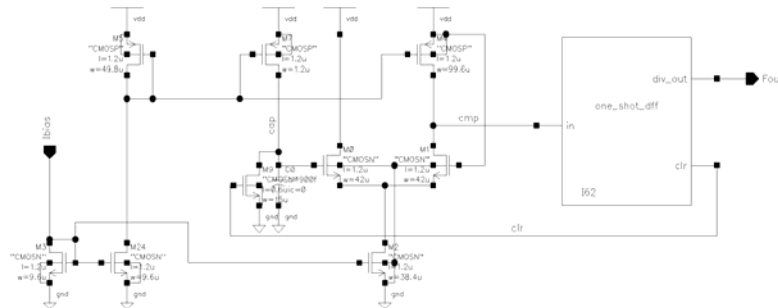


Fig. 16: Low Frequency Sawtooth Oscillator

A constant current is steered onto the MEMS device and this resulting signal is fed into a simple comparator. Once the threshold of the comparator is exceeded, a one shot is triggered to close a switch and discharge the capacitor. This trigger signal is fed into a D-latch and sent to a pad for external measurement (Figure 17).

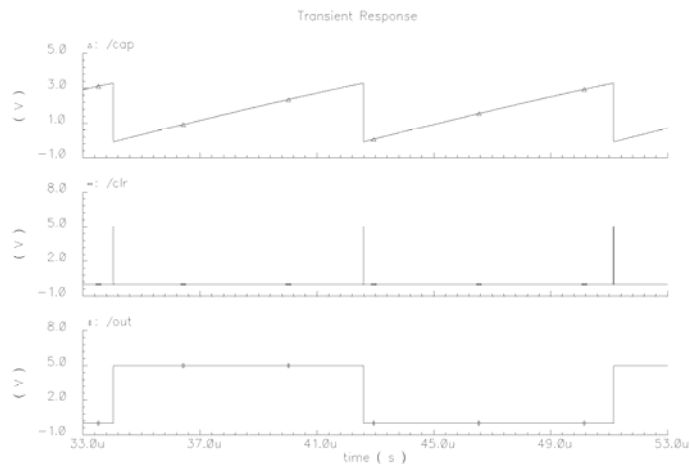


Fig. 17: Comparator Circuit waveforms

As the heater voltage is changed on the MEMS capacitor and its height varies, the frequency of the output waveform varies as well. The basic operation obeys the following principle:

$$v(t) = \frac{1}{C} \int_{t_{reset}} i_{ref} dt \quad (12)$$

The clear signal (pulse from the one-shot) is fed to a D-flip flop, so its actual frequency is divided by 2. Where I is approximately 600nA, and the comparator reset voltage is approximately 3.5 volts, the output frequency is given by:

$$f_{out} = \frac{75e-9}{C_{MEMS}} Hz \quad (13)$$

Using our actual values and considering parasitics, the output frequency for an unreleased MEMS structure should be approximately 80kHz. The entire tuning range should span a frequency change of about 12.5kHz. Simulation results agreed with the hand calculations. Simulations of this circuit also produced the desired results and passed all process corners.

4. Chip Layout and Measurement Results

4.1 Layout

Extensive consideration was given to ensure good matching during the layout process. Transistors that were to be well matched (differential pairs, latch transistors, etc.) were placed in the common-centroid configuration to ensure good matching over surface gradients. High frequency signal lines were kept short, metal lines were given the appropriate widths for peak switching currents, and power supply bypass capacitors were used whenever possible. The chip contained two 1GHz VCOs, each with one of our MEMS capacitor layouts. Two instances of the low frequency circuit were also included. Each layout was extracted and then re-simulated to verify operation and performance. All of the extracted circuits appeared to operate flawlessly after the layout process. The final die size was 4mm x 2mm. The chip layout is shown in Figure 18 with each individual section highlighted.

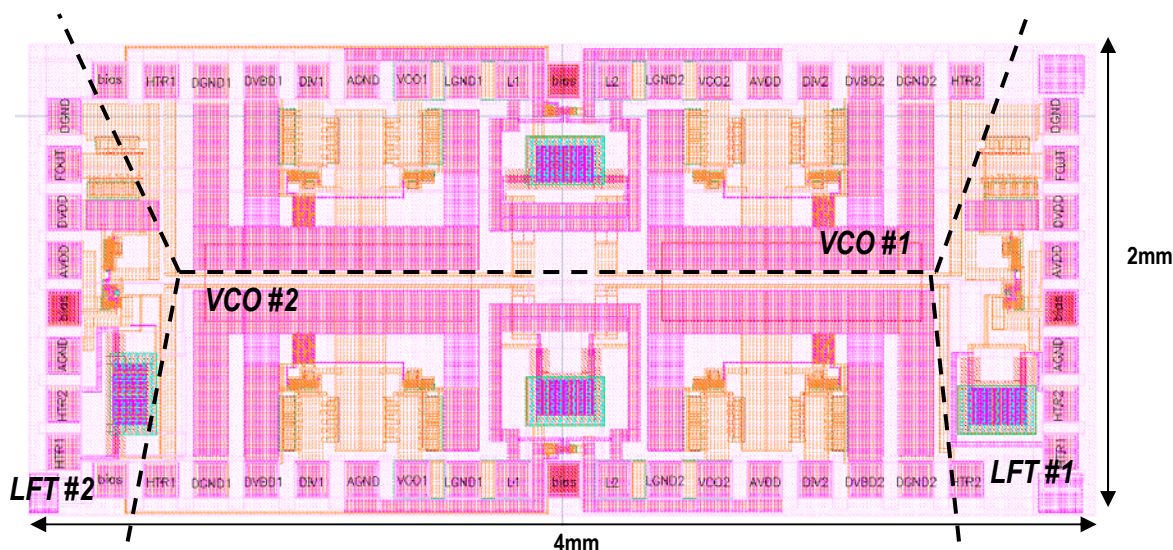


Fig. 18: Chip Layout

4.2 Measurement Results

Initial testing of only the circuitry was performed on chips with unreleased structures. Tests were conducted on both the RF VCOs and low frequency oscillator circuits. After these tests were completed, another set of dies with released structures were bonded and tested.

4.2.1 Low Frequency Sawtooth Oscillator

All instances of the low frequency sawtooth oscillator circuit operated as expected on all of our test dies. Each of them output a square wave at about 80kHz as in our simulations and performed consistently across all of our test samples. The output is shown in Figure 19 below.

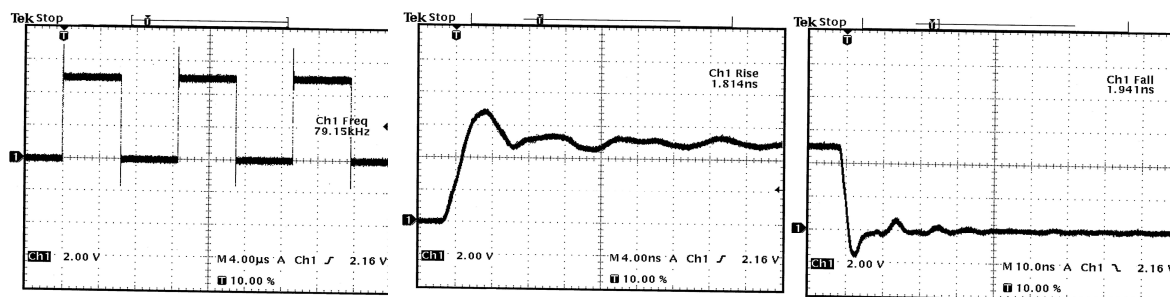


Fig. 19: LF oscillator output waveform

4.2.2 1GHz RF VCO

It was found that the RF VCO unfortunately had startup trouble. While everything appeared to bias correctly, the circuit would refuse to oscillate. Some further experimentation was conducted to try increasing the gain and exciting the tank circuit externally, but unfortunately nothing happened. Verification of the layout extraction revealed no major errors and the extracted view simulated properly in Spectre, but the real circuit just would not start. This could have been due to the fact that we so closely approached the f_T of the process or tank Q wasn't as expected. Although the circuit was carefully laid out, it could have also been caused by unknown parasitics not extracted by the simulator.

4.2.3 Testing of Released Structures

After the MEMS release procedure was perfected, four dies with released structures were tested using the low frequency sawtooth oscillator. Since the base oscillation from the sawtooth circuit for all of our released structures increased from 80kHz to somewhere in the range of 100kHz-200kHz, it was fairly certain that the structures had been released.

When trying to heat the structures through the serpentine resistor to change the capacitance, it was found that only one instance of the capacitor on one of the dies actually carried current. All of the other devices appeared to be open circuits. For the device that was actually burning power, the output frequency did change, but in the opposite direction than expected. Further investigation under a microscope revealed that only half of this structure was released, and when heated the half of the capacitor that was released buckled in the wrong direction. The output frequency from the sawtooth circuit went up instead of down as a result, as can be seen in Figure 20. This capacitor actually had different response curves while heating and cooling, probably due to the fact that half of the structure was still unreleased.

Investigation of the devices that did not carry current showed that the serpentine resistor on top of the plate became delaminated from the rest of the structure, causing it to break into many pieces, as seen in Figure 21.

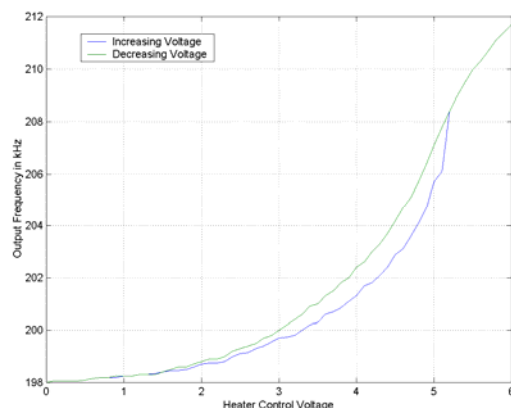


Fig. 20: LF sawtooth oscillator output frequency vs. heater control voltage

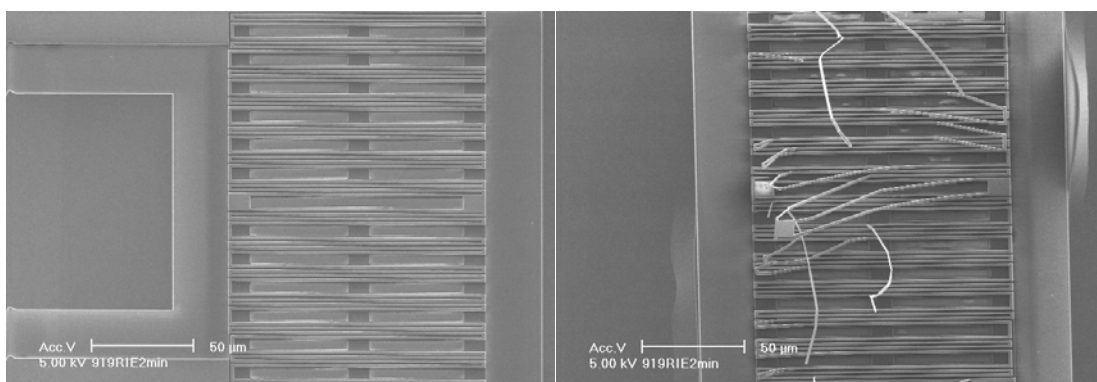


Fig. 21: SEMs of released structures with minor and major delamination

In order to prevent this from occurring in future designs, it is possible to put a layer of Metal 3 on top of the entire plate structure, since Metal 3 is immune to the release process and protects what is underneath it. The only disadvantages of using Metal 3 are that the structures will not curl as much when released because of the added thickness and stiffness of the Metal 3 layer. This will result in a reduction of tuning range. Additionally, the thermal resistance of the springs will be significantly reduced, requiring more power to heat the movable plate.

5. Conclusions

A high-Q, wide tuning range, thermally actuated MEMS capacitor has been designed and fabricated for on-chip radio frequency applications. From the analysis and discussion

presented in this paper, it appears that such a device will provide excellent RF performance in most applications. Although MEMS processes require special attention initially to get set up properly, once the process is tuned and streamlined MEMS devices offer repeatable robust performance. Although it was impossible for us to test our devices as desired, the author has the opinion that after some further investigation and development MEMS devices will become extremely useful in the RF IC arena.

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Appendix: MATLAB Code

```

function C=mkcap(b,w,enddist,sprwdth,indx,indx,len,A)
% 2-D Finite Element Capacitor Creator
% mkcap.m
% Ver. 0.1 04/05/01
%
% To be used as a function call from buildmems.m
%
% The subcircuit punched by this deck is already created
% in hspice, and elements are already appropriately sized in
% the subcircuit. The subckt has this as its definition:
% Xxy n11 n12 n13 n14 n21 n22 n23 n24 n31 n32 n33 n34 n41 n42 n43 n44 block2d h=x
% nab is defined where a is the layer top to bottom (m2, m1, capwell, substrate)
% and b is the 'rotational' contact from the 'left' going clockwise. h is the
% distance between the plates because of curl.
%

format long e;
wblk=w/b; % Computes the width of each block
d=len/wblk;
stitchnum=sprwdth/wblk;
rcir=100*5.8e-3;
ccir=2*pi*rcir;
rsqwell=2.9;
rctct=2.4;
numspred=floor(wblk/1.5e-6);
rincr=0;
cincr=0;
sres=((2*rsqwell)+rctct)/numspred;
spredres=[num2str(sres)];
ccapval=(3.7*8.854188e-12*wblk*1400e-10)/(.9e-6);
[t,crap]=size(A);
for (x=1:d) % X blocks
    for (y=1:b) % Y blocks
        output=[];
        for (z=1:4) % Z Layers (M2=1, M1=2, Capwell=3, Subst.=4)
            nx1=['R' num2str(z) ' ' num2str(x) ' ' num2str(y)];
            nx2=['R' num2str(z) ' ' num2str(x) ' ' num2str(y+1)];
            ny1=['C' num2str(z) ' ' num2str(x) ' ' num2str(y)];
            ny2=['C' num2str(z) ' ' num2str(x+1) ' ' num2str(y)];
            dl=enddist+((x*(w/b))-(w/(2*b)));
            dll=enddist+((x*(w/b))-(w/b));
            dlh=enddist+(x*(w/b));
            angle=(360/(ccir/dl))*(pi/180);
            angh=(360/(ccir/dlh))*(pi/180);
            angl=((360*dll)/ccir)*(pi/180);
            height=rcir*(1-cos(angle));
            hhigh=rcir*(1-cos(angh));
            hlow=rcir*(1-cos(angl));
            if (z==1)
                if (x==1)
                    if (y <= stitchnum)
                        nyl=['outm1'];
                    elseif (y >= (b-stitchnum+1))
                        nyl=['outm2'];
                    else
                        rincr=rincr+1;
                        nyl=['term' num2str(rincr) ' ' ''];
                        res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
                        disp(res);
                    end
                end
                if (y==1)
                    rincr=rincr+1;
                    nx1=['term' num2str(rincr) ' ' ''];
                    res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
                    disp(res);
                end
                if (x==b)
                    rincr=rincr+1;
                    ny2=['term' num2str(rincr) ' ' ''];
                    res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
                    disp(res);
                end
                if (y==b)
                    rincr=rincr+1;
                    nx2=['term' num2str(rincr) ' ' ''];
                    res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
                    disp(res);
                end
            end
        end
        if (z==2)
            if (x==1)
                if (y <= stitchnum)
                    nyl=['outp1'];
                elseif (y >= (b-stitchnum+1))
                    nyl=['outp2'];
                else
                    rincr=rincr+1;
                    nyl=['term' num2str(rincr) ' ' ''];
                    res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
                    disp(res);
                end
            end
            if (y==1)
                rincr=rincr+1;
            end
        end
    end
end

```

```

        nx1=['term' num2str(rincr) ' '];
        res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
        disp(res);
    end
    if (x==b)
        rincr=rincr+1;
        ny2=['term' num2str(rincr) ' '];
        res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
        disp(res);
    end
    if (y==b)
        rincr=rincr+1;
        nx2=['term' num2str(rincr) ' '];
        res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
        disp(res);
    end
    if (y==b/2)
        cincr=cincr+2;
        nx2=['ccap' num2str(cincr) ' '];
        ccap=['Ccpl' num2str(cincr) ' (ccap' num2str(cincr) ' ccap' num2str(cincr+1) ' ) capacitor c=' num2str(ccapval)];
        disp(ccap);
    end
    if (y==(b/2)+1)
        nx1=['ccap' num2str(cincr+1) ' '];
    end
end
if (z==3)
    if (x==1)
        rincr=rincr+1;
        ny1=['term' num2str(rincr) ' '];
        res=['R' num2str(rincr) ' (term' num2str(rincr) ' gnd!) resistor r=1e18'];
        disp(res);
    end
    if (y==1)
        rincr=rincr+1;
        nx1=['spred' num2str(rincr) ' '];
        res=['R' num2str(rincr) ' (spred' num2str(rincr) ' layer3) resistor r=' spreadres];
        disp(res);
    end
    if (x==b)
        rincr=rincr+1;
        ny2=['spred' num2str(rincr) ' '];
        res=['R' num2str(rincr) ' (spred' num2str(rincr) ' layer3) resistor r=' spreadres];
        disp(res);
    end
    if (y==b)
        rincr=rincr+1;
        nx2=['spred' num2str(rincr) ' '];
        res=['R' num2str(rincr) ' (spred' num2str(rincr) ' layer3) resistor r=' spreadres];
        disp(res);
    end
end
if (z==4)
    if (x==1)
        ny1=['gnd!'];
    end
    if (y==1)
        nx1=['gnd!'];
    end
    if (x==b)
        ny2=['gnd!'];
    end
    if (y==b)
        nx2=['gnd!'];
    end
end
output=[output nx1 ' ' ny1 ' ' nx2 ' ' ny2 ' '];
end
output = ['X' num2str(x) '_' num2str(y) ' (' output ') block2d h=' num2str(height)];
disp(output);
xx=(x-1+t);
A(xx,y)=hlow;
A(xx+1,y)=hhigh;
A(xx,y+1)=hlow;
A(xx+1,y+1)=hhigh;
end
end
C=A;
function [endidx,B] = mkspr(blk,l,w,wplate)
% 2-D Finite Element Spring Netlist Puncher
% makespring.m
% Ver. 0.1 06/07/01
%
% This program punches out a SPICE/Spectre deck which models
% the distributed capacitance of a MEMS spring. The way it works
% is by finding the complete lumped resistances and capacitances
% and divides them up into blocks.

format long e;
rp=70e-3; % Base Resistance (per square)
rm=70e-3;
rcir=100*5.8e-3;
ccir=2*pi*rcir;
N=round(l/(wplate/blk));
A=l*w;
stitchnum=w/(wplate/blk);
rpblk=l*rp/(w*N);
rmblk=l*rm/(w*N);
B=NaN*ones(N+1,blk+1);
for (j=1:2)

```

```

for (i=1:N)
    dl=((i*1)/N)-(1/(2*N));
    dlh=(i*1)/N;
    dll=((i*1)/N)-(1/(N));
    angle=(360/(ccir/dl))*(pi/180);
    angh=(360/(ccir/dlh))*(pi/180);
    angl=((360*dll)/(ccir))*(pi/180);
    h=rcir*(1-cos(angle));
    cp=((8.854e-12)/((5600e-10/3.7)+(2500e-10+h))); % Base Cap. to Sub. (F/(m^2))
    cpblk=A*cp/N;
    cm=44e-18*1e12;
    cmblk=A*cm/N;
    hhigh=rcir*(1-cos(angh));
    hlow=rcir*(1-cos(angl));
    if (i==1 & i~=N)
        res=[ 'Rp' num2str(i) ' ' num2str(j) ' (inp' num2str(j) ' ' num2str(i) num2str(j) ' ) resistor r=' num2str(rpblk)];
        cap=[ 'Cp' num2str(i) ' ' num2str(j) ' ( ' num2str(i) num2str(j) ' gnd! ) capacitor c=' num2str(cpblk)];
        res1=[ 'Rm' num2str(i) ' ' num2str(j) ' (inm' num2str(j) ' m' num2str(i) num2str(j) ' ) resistor r=' num2str(rmbk)];
        cap1=[ 'Cm' num2str(i) ' ' num2str(j) ' ( ' num2str(i) num2str(j) ' m' num2str(i) num2str(j) ' ) capacitor c='
num2str(cmbk)];
    elseif (i==N & i~=1)
        res=[ 'Rp' num2str(i) ' ' num2str(j) ' ( ' num2str(i-1) num2str(j) ' outp' num2str(j) ' ) resistor r=' num2str(rpblk)];
        cap=[ 'Cp' num2str(i) ' ' num2str(j) ' (outp' num2str(j) ' gnd! ) capacitor c=' num2str(cpblk)];
        res1=[ 'Rm' num2str(i) ' ' num2str(j) ' (m' num2str(i-1) num2str(j) ' outm' num2str(j) ' ) resistor r=' num2str(rmbk)];
        cap1=[ 'Cm' num2str(i) ' ' num2str(j) ' (outp' num2str(j) ' outm' num2str(j) ' ) capacitor c=' num2str(cmbk)];
    elseif (i==1 & i==N)
        res=[ 'Rp' num2str(i) ' ' num2str(j) ' (inp' num2str(j) ' outp' num2str(j) ' ) resistor r=' num2str(rpblk)];
        cap=[ 'Cp' num2str(i) ' ' num2str(j) ' (outp' num2str(j) ' gnd! ) capacitor c=' num2str(cpblk)];
        res1=[ 'Rm' num2str(i) ' ' num2str(j) ' (inm' num2str(j) ' outm' num2str(j) ' ) resistor r=' num2str(rmbk)];
        cap1=[ 'Cm' num2str(i) ' ' num2str(j) ' (outm' num2str(j) ' outp' num2str(j) ' ) capacitor c=' num2str(cmbk)];
    else
        res=[ 'Rp' num2str(i) ' ' num2str(j) ' ( ' num2str(i-1) num2str(j) ' ' num2str(i) num2str(j) ' ) resistor r='
num2str(rpblk)];
        cap=[ 'Cp' num2str(i) ' ' num2str(j) ' ( ' num2str(i) num2str(j) ' gnd! ) capacitor c=' num2str(cpblk)];
        res1=[ 'Rm' num2str(i) ' ' num2str(j) ' (m' num2str(i-1) num2str(j) ' m' num2str(i) num2str(j) ' ) resistor r='
num2str(rmbk)];
        cap1=[ 'Cm' num2str(i) ' ' num2str(j) ' ( ' num2str(i) num2str(j) ' m' num2str(i) num2str(j) ' ) capacitor c='
num2str(cmbk)];
    end
    disp(res);
    disp(cap);
    disp(res1);
    disp(cap1);
    for (q=1:stitchnum+1)
        B(i,q)=hlow;
        B(i,(blk+2-q))=hlow;
        B(i+1,q)=hhigh;
        B(i+1,(blk+2-q))=hhigh;
    end
end
end
endidx=N;

function mkblk(w,N,hinit)

% Unit Parameters
baseRm2=70e-3; % ohms/sq Metal2 Resistance
baseCmm=22e-6; %41e-6; % F/m^2 M1 to M2 Capacitance
baseRm=70e-3; % ohms/sq M1 Resistnace
baseCmc=58.4e-6; % F/m^2 M1 to Capwell Capacitance
baseRc=30; % ohms/sq Capwell Resistance
baseCcs=487e-6; % F/m^2 Capwell to Substrate Resistance
baseRs=2e3; % ohms/sq Substrate Resistance
eo=8.854188e-12; % Dielectric constant
e1=3.7; % Dielectric constant of capwell

cmmblk=((w^2)/(N^2))*baseCmm;
cmcblk=((w^2)/(N^2))*((eo)/((5600e-10/e1)+hinit));
ccsblk=((w^2)/(N^2))*baseCcs;
base=((w^2)/(N^2))*eo;
rm2blk=baseRm2/2;
rmbk=baseRm/2;
rcblk=baseRc/2;
rsblk=baseRs/2;

% 1-unit Subcircuit
disp(['subckt block2d (n11 n12 n13 n14 n21 n22 n23 n24 n31 n32 n33 n34 n41 n42 n43 n44)']);
disp([' parameters h=0']);
disp([' Rt1 (n11 mt12) resistor r=' num2str(rm2blk)]);
disp([' Rt2 (n12 mt12) resistor r=' num2str(rm2blk)]);
disp([' Rt3 (n13 mt12) resistor r=' num2str(rm2blk)]);
disp([' Rt4 (n14 mt12) resistor r=' num2str(rm2blk)]);
disp([' Cmm (mt12 mtl) capacitor c=' num2str(cmmblk)]);
disp([' Rm1 (n21 mtl) resistor r=' num2str(rmbk)]);
disp([' Rm2 (n22 mtl) resistor r=' num2str(rmbk)]);
disp([' Rm3 (n23 mtl) resistor r=' num2str(rmbk)]);
disp([' Rm4 (n24 mtl) resistor r=' num2str(rmbk)]);
disp([' Cmc (mtl cpw) capacitor c=' num2str(base) ' / ((5600e-10/3.7)+(2500e-10+h)) ']);
disp([' Rc1 (n31 cpw) resistor r=' num2str(rcblk)]);
disp([' Rc2 (n32 cpw) resistor r=' num2str(rcblk)]);
disp([' Rc3 (n33 cpw) resistor r=' num2str(rcblk)]);
disp([' Rc4 (n34 cpw) resistor r=' num2str(rcblk)]);
disp([' Ccs (cpw subs) capacitor c=' num2str(ccsblk)]);
disp([' Rs1 (n41 subs) resistor r=' num2str(rsblk)]);
disp([' Rs2 (n42 subs) resistor r=' num2str(rsblk)]);
disp([' Rs3 (n43 subs) resistor r=' num2str(rsblk)]);
disp([' Rs4 (n44 subs) resistor r=' num2str(rsblk)]);

```

```

disp(['ends block2d']);

% Main.m

A=[];
B=[];
pwdt=input('What is plate width? ');
plen=input('What is plate length? ');
blk=input('How many discrete blocks/side? ');
sprl=input('What is spring length? ');
sprw=input('What is spring width? ');
hstrt=0; %input('What is base height? ');
delete cap.inc;
diary cap.inc;
[eidx,C]=mkspr2(blk,sprl,sprw,pwdt);
C=mkcap2(blk,pwdt,sprl,sprw,eidx,plen,C);
mkblk2(pwdt,blk,hstrt);
diary off;
[a,b]=size(C);
for i=1:a
    A=[A pwdt/blk*(i-1)];
end
for i=1:b
    B=[B pwdt/blk*(i-1)];
end
A=1e6*A;
B=1e6*B;
C=1e6*C;
surf(B,A,C);
x=max([max(A) max(B)]);
y=max(max(C));
axis([0 x 0 x 0 y]);
xlabel('x in microns');
ylabel('y in microns');
zlabel('z in microns');
title('Finite-Element Capacitor Model/Analysis');

```