LNA and mixer trade-offs across 1.5 GHz, 2.4 GHz and 3.2 GHz bands and CMOS and SiGe processes

by

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- Chulmin Jung

Abstract

LNAs and mixers are designed for various processes using a synthesis tool (NeoCircuit). RF design considerations such as impedance matching guided the selection of a LNA and mixer topology that could be simultaneously used for 1.5 GHz, 2.4 GHz and 3.2 GHz bands. The sample processes include TSMC 0.18, 0.25, 0.35 μm, SiGe5HP and SiGe6HP. A total of 30 viable RF circuits are designed. A new technique named Local Power Distribution S-parameter (LPDS) is developed for faster IIP3 evaluation. RF front end design trade-offs such as power, noise, IIP3 and their trends across increasing RF frequency bands and evolving process feature size shrinks are identified, and can be used by wireless system architects to identify directions for future wireless front end circuit research.

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1. Introduction

RF design has become increasingly important due to rapidly growing wireless markets. Designers are faced with shorter design cycles and with increasingly difficult specifications. Low power operation is leading to M-QAM replacing M-QPSK, which, when combined with increased bit rates implies increasing increasing linearity requirements (1dB, IIP3) for the RF front end. As the operating frequency increases, IC parasitics become more dominant, further increasing design difficulty. Another important factor which makes RF design difficult is process evolution. CMOS technologies are shrinking continuously. The wide bandgap SiGe HBT and its compatibility with CMOS processing has made SiGe competitive with GaAs process for RF front end design [1]. Just as in the case of carrier frequency, each process has its own unique design trade-offs. The understanding of the trends in these trade-offs across generations of carrier frequencies and processes is crucial to the development of new generations of RF IC designs [2][3].

Recently developed circuit synthesis tools help the automate much of the design effort in RF design [4]. In this thesis, Neocircuit was used to design multiple circuits for various processes and carrier frequencies, and identify their impact on design trade-offs. Three carrier frequencies and five processes are selected. A 1.5 GHz is commonly used for GPS receivers [5], 2.4 GHz has been allocated for industrial/ scientific/medical (ISM) uses [6][7]; and 3.2 GHz is a commonly licensed band for wireless communications. The TSMC 0.18 μm, 0.25 μm, 0.35 μm, and IBM SiGe5HP and SiGe6HP processes are chosen as these process parameters are easily available through MOSIS. The LNA and mixer topologies are designed for each of the 3 carrier frequencies and 5 processes through NeoCircuit. The resulting 30 designs are then compared to identify the general trend of the specification dependence as a function of processes and carrier frequencies.

Manual topology design was combined with Neocircuit to develop a rapid understanding of topology limitations. A topology capable of being used for all of the frequency bands and processes of interest was identified through this process. This use of a single LNA and a single mixer topology, allowed the focus to be on the impact of process and carrier frequency trends. The bottleneck to the simulation-based synthesis approach embedded in NeoCircuit is usually the simulation time as well as convergence. The longest RF simulation for all the circuits is related to the IIP3 evaluation. A new method for reducing the simulation time was developed.

2. Background and focus

2.1 General consideration of RF design

RF IC design tends to focus on trade-offs between specifications for narrowband RF gain, low noise figure, impedance matching to a standard characteristic impedance (usually 50 Ω), wide dynamic range and low power operation.

2.1.1 Impedance matching

The impedance matching network, including bond pad capacitance, and wirebond inductance strongly determines the RF circuit performance through three primary parameters: center frequency, quality factor and effective impedance. To enable fair comparisons between the synthesis runs, a single matching network topology is used. Since the same matching network is to be used at all three carrier frequencies, the network should have adequate design freedom to enable optimal matching. Figure 1(a) shows the simple L-match with inductive source degeneration or series feedback scheme [8], commonly used in many LNA designs, because of its excellent noise performance [5]. This simple structure cannot meet the design goals for the three frequency bands, given pad capacitance and other parasitics, as the element size only sets the matching frequency. A π-matching network was adopted to allow independent design of Q and center frequency (Figure 1 (b)).

2.1.2 Inductor model

Matching network design depends strongly on inductor design, which is governed by three parameters: the inductance values, the inductor Q and self-resonance frequency. Inductance values depend on inductor shape and process parameters [9]. Due to the unavailability of the Q parameters for all the

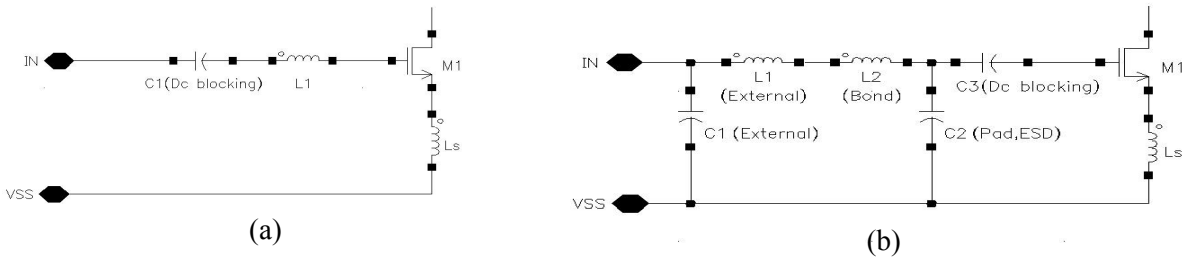


Figure 1: (a) L-matching network and (b) π-matching network for CMOS LNAs

processes, this thesis assumes a constant Q factor of 5 for all the processes. Also, the three frequencies for which the circuits are designed are assumed to be well below the inductor self resonance frequency. These assumptions effectively imply that the process comparisons in this thesis focus solely on the active devices.

2.1.3 Noise Figure

Noise Figure (NF) plays important role in RF IC designs, particularly for low noise amplifiers. Noise figure is specified with respect to a reference resistance (usually 50 Ω source resistance). As there is no resistive element looking into the gate of a MOS device, a series resistance is needed for impedance matching. Since this series resistance adds noise, inductive degeneration is usually used [8]. The remaining noise sources in the circuit are the device thermal noise [10] and the induced gate current noise [11]. Increasing the V_{GS} bias point increases the bias current and the transconductance, and reduces the MOS thermal noise. However, increased V_{GS} degrades output impedance and thus S_{12} performance. Increasing the transistor size increases C_{gs} thereby reducing Q, so there is not much improvement in the noise figure.

Noise in bipolar SiGe devices arises primarily from shot noise and the thermal noise in the base resistor. A large collector current generates more shot noise. The base resistance (hence base resistance noise) can be reduced by increasing the emitter area, which means increasing collector current. A large collector current also improves the gain of bipolar device thereby reducing NF. So there must be a trade-off between power consumption and NF.

The NF goal was set to 1.5 dB for the LNAs and 15 dB for the mixers from a survey of recent wireless IC publications [12][13][14].

2.1.4 Third order Input Intercept Point (IIP3)

When strong nearby channels accompany a weak desired signals, intermodulation distortion arising from circuit nonlinearity may overlap onto the desired channel. In narrowband RF circuits, the filtering effect normally has a bandpass characteristics, and only the third-order intermodulation distortion tends to lie within the passband. The nonlinearity is usually measured as an input-referred 3rd order intercept (IIP3) using a two-tone test. The intermodulation distortion can be considered a noise source, thus is often combined with the random process based analysis of noise at the circuit output to define Spurious-Free

Dynamic Range (SFDR) [11].

2.2 Circuit topology for optimization

2.2.1 Test benches

Figure 2 shows the two-port test bench used to characterize the LNAs during circuit synthesis. S-parameter analysis between PORT0 and PORT1, was used to evaluate the LNA S_{11}, S_{21}, S_{12}, S_{22} parameters and the noise figure. Power was measured directly from the LNA bias source (I_{bias} in Figure 4) and IIP3 was computed using a two tone test and a simplified LPDS approach as will be discussed later.

The mixer testbench is described in Figure 3. The mixer output is connected to a bandpass image rejection filter. The output load includes the dc blocking coupling capacitor, and the resistive and capacitive load of the IF filter. The parasitic capacitance due to the large dc blocking capacitor is also included in the capacitance in C_0 and C_2. The operation of the test bench is as follows. A single RF input is applied at one of the carrier frequencies (1.5 GHz, 2.4 GHz, and 3.2 GHz). The differential local oscillator input voltage LO_P/LO_N signal is generated with 180 degree phase difference at 50 MHz higher than the RF frequency. The IF frequency is set to 50 Mhz and SpectreRF's periodic steady state (pss) and periodic noise (pnoise) analysis is used to evaluate the mixer's conversion gain and noise. Conversion gain is obtained by adding 6 dB to VO_P instead of computing the differential output voltage. Noise is obtained

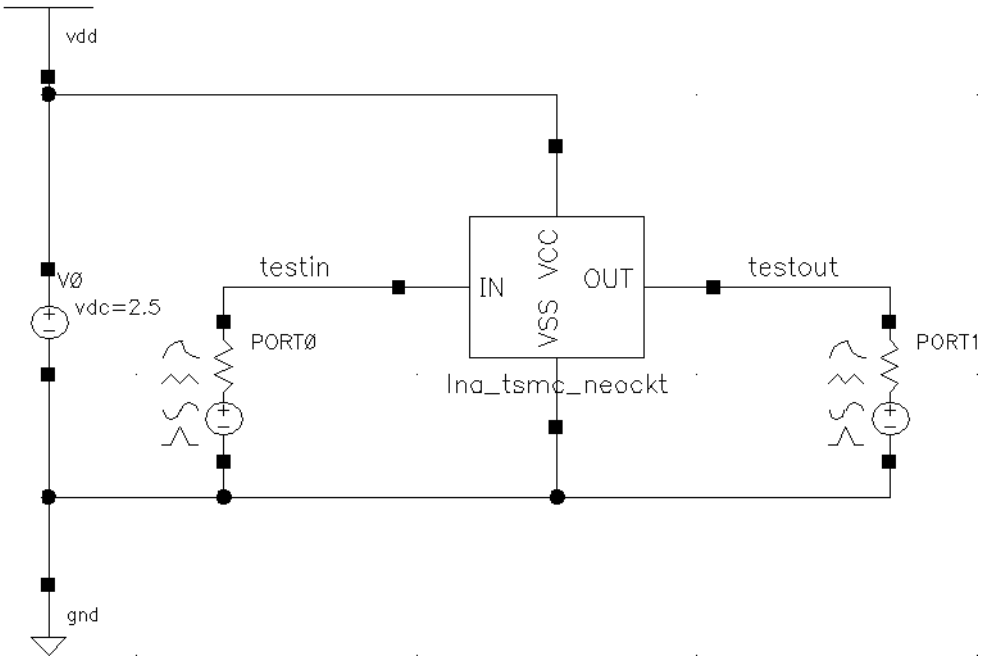


Figure 2: Test bench of LNAs

from 30 sidebands using a pnoise analysis for more accurate results [15]. The IIP3 of mixers can not be simulated in each NeoCircuit synthesis iteration because it takes a extremely long simulation time. The down conversion mixer characteristic leads to longer PSS and PAC analysis time. The synthesis engine times out on the IIP3 evaluations, and cannot converge to a design if this design constraint is included. Even though IIP3 is more important than Noise Figure (NF) in mixers, it remains as future research topic due to the limitation of synthesis framework.

2.2.2 CMOS LNAs

For CMOS LNAs, the widely used cascoded common source with inductor degeneration [16] was combined with a π−matching network interface as shown in Figure 4. This topology because of its ability to combine high gain, low noise, good stability and high reverse isolation. The input matching network is formed using an external capacitance (C_{extin}), an internal pad capacitance (C_{padin}), and an external inductance (L_{extin}) in series with bond wire inductance (L_{bin}). The real part of the input impedance arising from the series feedback inductor (L_s) and the common source transistor (M_{drive}) adds to the π matching network impedance for the total input impedance.

The bias circuit mirrors the bias current I_{bias} into M_{drive} with a 1:1 ratio, allowing the use of the value of I_{bias} to directly measure the power consumed in the circuit. In practical LNA design, a low bias current

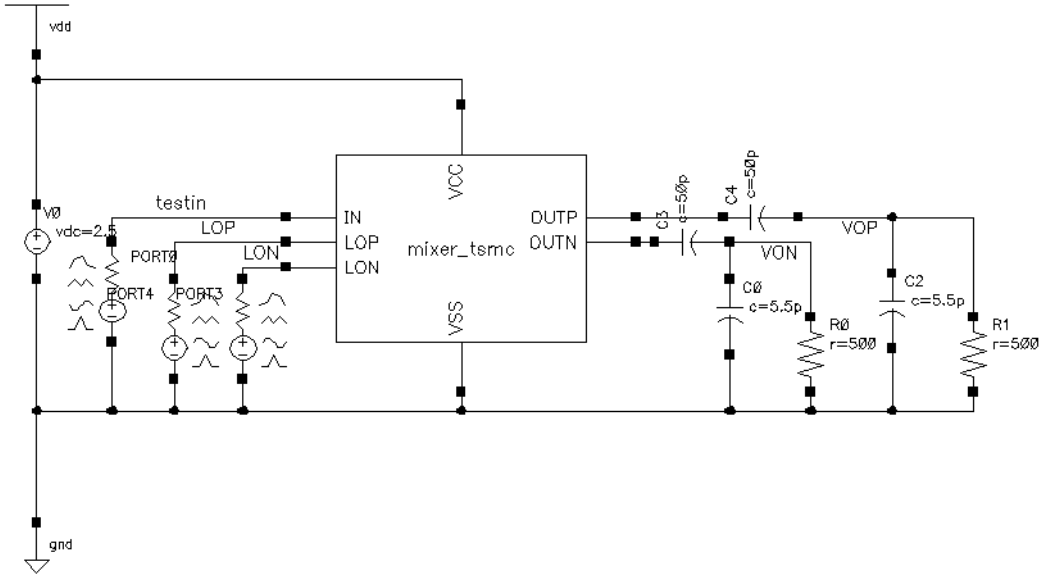


Figure 3: Mixer Test Bench

is used and width scaling in M_{bias} and M_{drive}; power consumption is then measured by averaging. The 1:1 ratio approach is used since the averaging approach to measuring power consumption is too slow for simulation-based synthesis. The 100pF capacitor (C_{bias}) filters off any high frequency noise generated by M_{bias} from affecting the LNA performance. R_{bias} delivers the bias voltage to M_{drive}, while at the same time presenting a high impedance for the input RF signal, so that the signal current flows to the signal transistors rather than the bias circuitry. A large value of R_{bias} is optimum for noise and RF decoupling; however an excessive value will make the bias current very sensitive to transistor matching due to the voltage drop across R_{bias}.

The feedback blocking cascode transistor (M_{series}) prevents the Miller capacitance from degrade S_{11} and S_{12} parameters. The load inductor was modeled with ideal inductor (L_{load}) and series resistance (R_{load}). Another series resistance (R_{match}) was inserted to add one more degree of freedom for S_{22} parameter optimization. It was observed that without R_{match}, it was to hard to meet all the specifications for select process and carrier frequencies. A π-match structure is also used at the output for design freedom

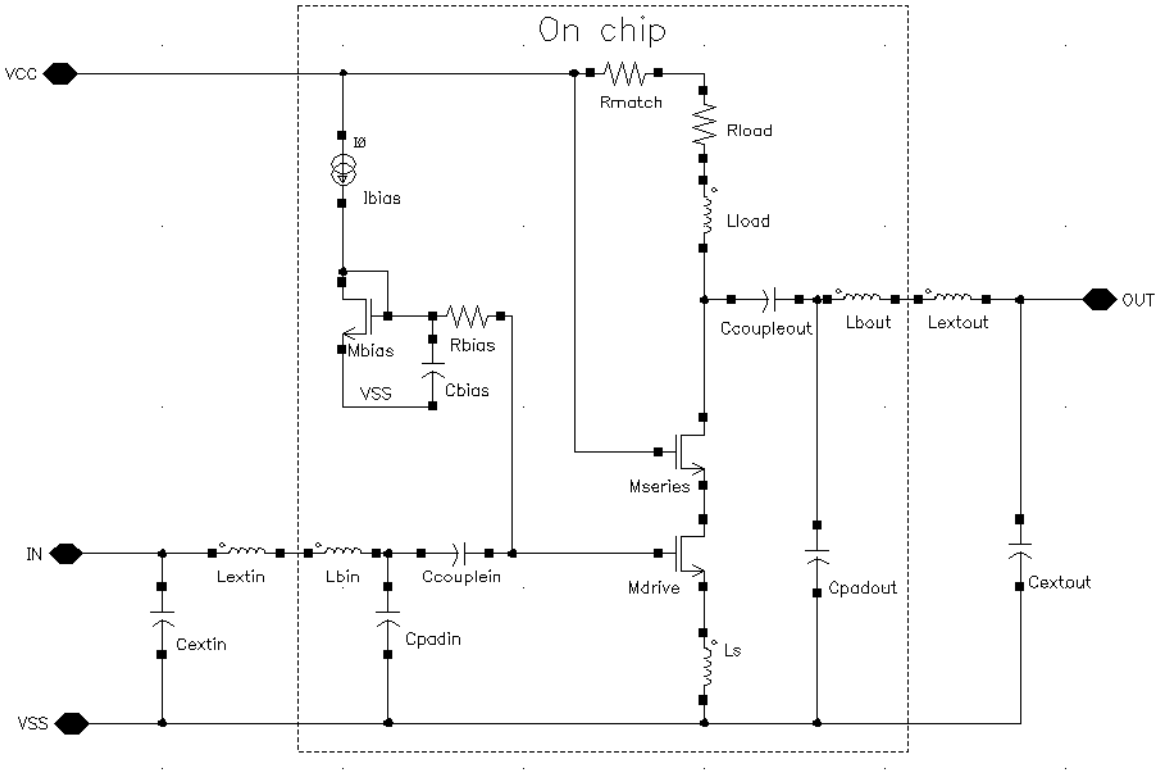


Figure 4: Topology of CMOS LNAs

during synthesis. The resulting circuit topology was used to synthesize 1.5 GHz, 2.4 GHz and 3.2 GHz designs for each of the TSMC 0.18 μm, 0.25 μm, and 0.35 μm processes.

2.2.3 Bipolar SiGe LNAs

The SiGe HBT has high gain and cut-of frequency characteristics that are important for RF IC design. The primary difference between the SiGe design and the CMOS design arises from the base input resistance and bias circuit design. The base resistance can be reduced by increasing emitter area, but still dominates the design of impedance matching compared to the small base-emitter junction capacitance. The π input matching network is versatile enough to handle this difference as will be shown in the synthesis.

Figure 5 shows the circuit topology of the SiGe LNAs. The bias circuit topology allows compromise between noise and gain, as will be discussed later. The bias circuit for Q_{series} is a simple resistive bias circuit using two identical resistors (R_{bup}, R_{bdn}) and a capacitor (C_b). With using above circuit topology, 1.5 GHz, 2.4 GHz and 3.2 GHz LNAs were synthesized for the SiGe5HP and SiGe6HP processes.

2.2.4 CMOS Mixers

Gilbert-cell CMOS mixer circuit topologies are widely used to reduce local oscillator voltage feed

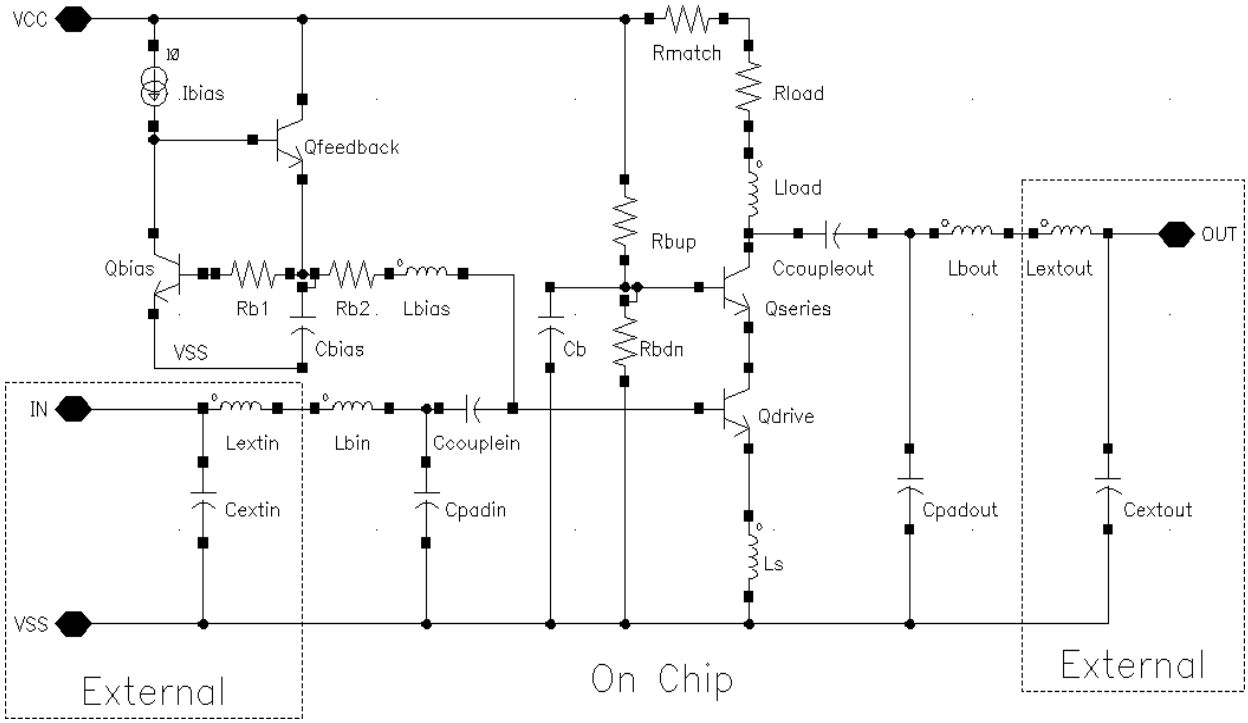


Figure 5: Topology of Bipolar LNAs

through to the output. The low-voltage LC tank (L_5 and C_6) based Gilbert-cell [17], with a π-matching network was adopted as the mixer topology (Figure 6). The LC tank is intended to resonate at the RF frequency, resulting in high equivalent impedance. The resulting Common Mode Rejection Ratio (CMRR) is better than that of a current source active device at low supply voltage because current source needs a certain amount of voltage drop for high output resistance.

From standpoint of input matching, it is same as LNA structure because the joint net (*A*) is a virtual short to ground in ac operation (the RF input (*IN*) was assumed to be differential into M1 and M2 — the figure shows just a single ended RF input). L_3 and R_1 models an on-chip inductor and R_2 is used for increased design freedom for input impedance matching.

2.2.5 Bipolar Mixers

This topology (Figure 7) is essentially the same as that of the CMOS mixer. Due to the difference in regions of operations of the MOS and bipolar device, there are differences in signal amplitudes. The bipolar differential pair needs is saturated with only a 20 to 30 mV differential input voltage. If the input voltage greatly exceeds 30 mV the bipolar devices enter deep saturation, slowing down the switching

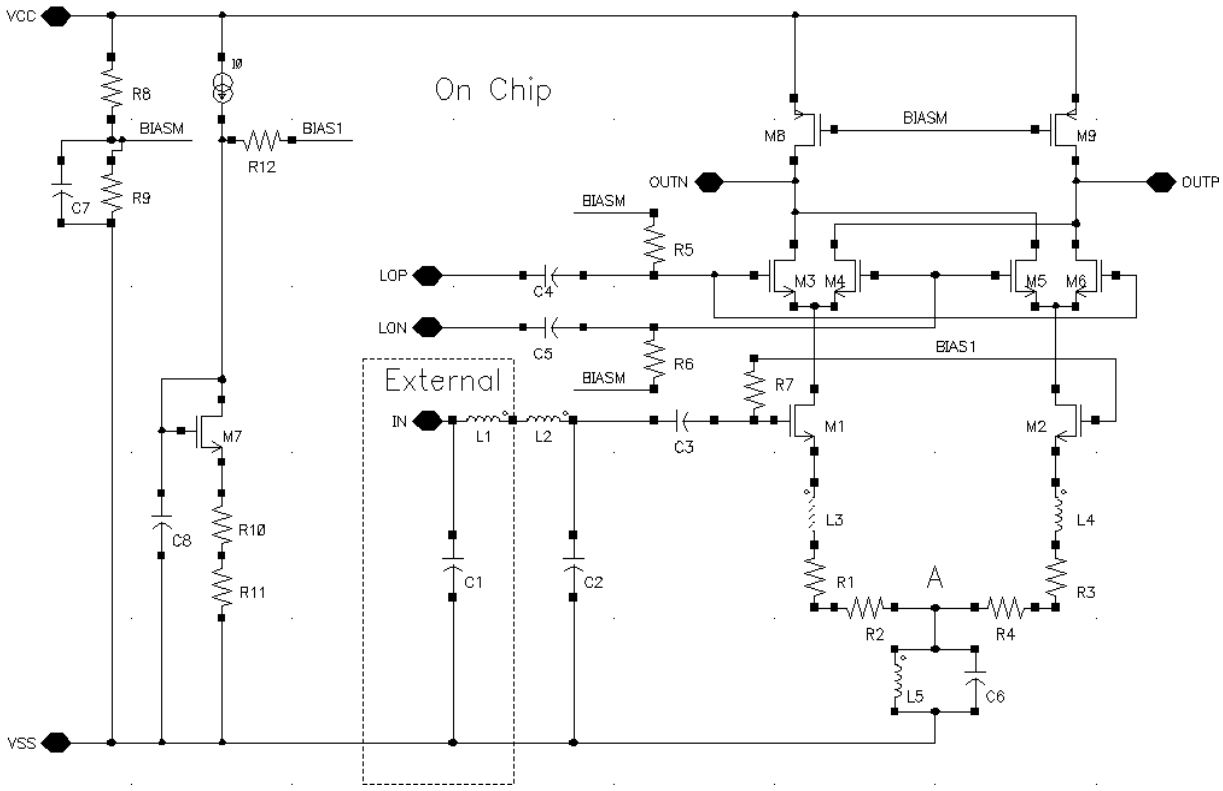


Figure 6: Topology of CMOS Mixers

operation due to excess charge in the base (which requires substantial time to recombine with majority charge — the holes in NPN device). Therefore, the differential LO amplitude is set to 0.2 V which is enough to act as a ideal switch, and can easily drain excess minority carriers (the electrons in NPN device).

2.3 Preliminary hand calculations

In addition to circuit topology and a test bench, NeoCircuit needs the range of values for each circuit element design variable. Hand calculations that capture the first order design trade-offs are used to identify suitable ranges. Here we include only the equations relevant to a CMOS LNA (see Figure 4). Similar equations for the other circuits are readily derived in [11][18]. The symbolic equations are general for LNAs; the numerical values relate to TSMC 0.25 μm CMOS process and 2.4 GHz carrier frequency.

The input impedance matching specification of 50 Ω sets the source degeneration inductance L_s. The impedance seen from the gate of M_{drive} to V_{SS} is

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}}Ls \approx sL_s + \frac{1}{sC_{gs}} + \omega_T L_s \tag{1}$$

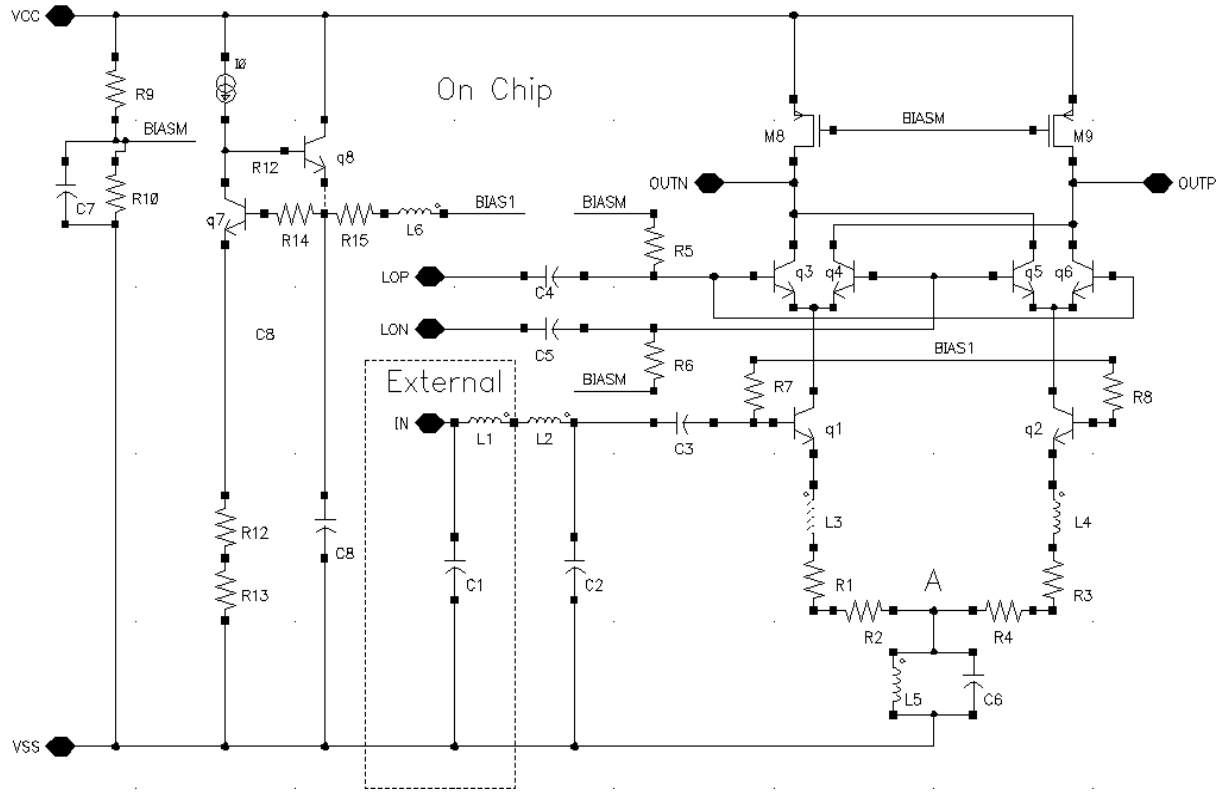


Figure 7: Topology of Bipolar Mixers

where ω_T is the unity current gain frequency of the MOS device. Z_{in} has a real resistance of $\omega_T L_s$ arising from the phase lag due to the source degeneration inductor. ω_T is proportional to the mobility of electrons of the NMOS device, and the transistor bias current, and inversely proportional to its gate length, leading to a unique constant value for each process (f_T = 10.1 GHz . for TSMC 0.25 μm)[1]. The total LNA input impedance is set by (1) and the Q of the π–matching network. By assuming that the input was applied directly to M_{drive}'s gate (thus Q=1) and by assuming that the RF signal is at the matching network's resonance frequency (thus the imaginary part of (1) is 0), the value of the source degeneration inductor can be obtained using

$$L_s = Z_{in}/\omega_T = 50/(2\pi \cdot 10.1\times 10^9) = 0.79 \text{ nH}. \quad (2)$$

Due to low quality factor in on-chip inductors, it is preferred to implement this inductance with a bond wire that connects the source of M_{drive} to off-chip RF ground. If L_s is different from 0.79 nH, the Q of the π-matching network will be changed by NeoCircuit to keep impedance to be around 50 Ω. The range of the design variable L_s was set to be 0.5 nH to 10 nH, with the range of practical bond wire inductances.

The transconductance from the RF input (*IN*) to the current through M_{drive} is

$$G_m = g_m Q_{in} = \frac{g_m}{\omega_o C_{gs} \omega_T L_S} = \frac{1}{\omega_o L_S} \quad (3)$$

where g_m is the transconductance of M_{drive}; ω_o is resonance frequency set by the input matching network, M_{drive} and L_S; $\omega_T L_s$ is series resistance due to inductive degeneration which adds to the source resistance R_s in a simplified series-resonant network model[2]. G_m is independent of the drive transistor size as a consequence of two competing effects that cancel each other [5]. Consider narrowing the NMOS input transistor without changing any bias voltages. The device transconductance, g_m, decreases according to the width. However the gate capacitance, C_{gs}, also shrinks by the same factor. The total inductance, $L_{extin} + L_{bin} + L_s$ therefore has to increase to

1. RF parasitics were ignored from the ω_T analysis.
2. the input circuit is a series-resonant network, thus, $Q_{in} = (\omega_o L)/R = 1/(\omega_o RC)$

maintain resonance at the specified RF signal frequency. Since the ratio of total inductance to gate capacitance increases, the Q of the input π-matching network must increase. This increase in Q cancels the reduction in device transconductance, so that the overall transconductance remains unchanged.

Including the load, the output circuit can be obtained from G_m as

$$Gain = \frac{G_m \omega_o L_{load}}{Q_{out}} \tag{4}$$

where Q_{out} is the Q of the output π-matching network, looking in from the output port (R_{load} has been neglected). Assuming Q_{out} to be 1 (it can't get too large because of stability and IIP3 issues) (2), (3) and (4) can be combined to $Gain = L_{load}/L_S$. The gain seems to be independent of device parameters; the device parameters affect the gain through L_S which depends on ω_T. The specified gain target is 15 dB, thus L_{load} is

$$L_{load} = Gain \cdot L_s = 5.6234 \cdot 0.79 \text{ nH} = 4.44 \text{ nH}. \tag{5}$$

The range of L_{load} was set to be 1 nH to 50 nH during synthesis.

The minimum LNA noise figure for a given power constraint, NF_{minP} is derived in [5][10][16]

$$NF_{minP} \approx 1 + 2.4\frac{\gamma}{\alpha}\left(\frac{\omega_o}{\omega_T}\right) \tag{6}$$

where γ is the coefficient of channel thermal noise and α is ratio of the device transconductance to the zero-bias drain conductance ($\alpha = g_m/g_{d0}$). The width of M_{drive} under this fixed power constraint is

$$W_{minP} = \frac{3}{2}\frac{1}{\omega_o L C_{ox} R_S Q_{inP}} \tag{7}$$

where Q_{inP} is the Q of input matching network with the power constraint, R_S is the source resistance, ω_o is the resonant frequency at the input, and L is M_{drive}'s length. For TSMC 0.25 μm CMOS, $C_{ox} = 6.2$ fF/μm^2. Assuming minimum device length and $Q_{inP} = 1$ for a first order

analysis

$$W_{minP} \approx \frac{3}{2} \frac{1}{2\pi \times 2.4\times10^{9} \times 0.25\mu m \times 6.2 f/\mu m^{2} \times 50} = 1283.5\ \mu m \tag{8}$$

leading to the appropriate range for width of M_{drive} during synthesis to be from 50 μm to 4000 μm.

The above hand calculations assumed a quality factor of 1 for both the input and output transformers that match the LNA impedance to the source at the input and the RF filter at the output. Next, hand calculations of the π-matching network transformer elements will be used to set the range for the inductors and capacitors forming the matching networks. Stability, IIP3 and 1 dB compression specifications limit the maximum allowable Q. Another potential limit for maximum Q is the lower bound on capacitance set by the input pad parasitic capacitance (primarily set by the ESD structure).

The π-matching is analyzed as in Figure 8. The Q of the right hand side is

$$Q_{right} = \sqrt{\frac{R_p}{R_{eq}} - 1} \tag{9}$$

where R_p is the real parallel resistance which was calculated as $\omega_T L_S$ by (1), and R_{eq} is equivalent series resistance assuming serial L-C-R for the right half network. From (2) *Rp* is 50 Ω. Assuming an input pad (including ESD) capacitance (C_2) of about 1 pF, the equivalent series resistance at 2.4 GHz is

$$R_{eq} = \frac{R_p}{1 + \omega^2 R_p^2 C_2^2} = \frac{50}{1 + (2\pi \cdot 2.4\times10^{9} \times 50 \cdot 1\times10^{-12})^2} = 31.8778\ \Omega. \tag{10}$$

This transform is valid at only one frequency so it is not an equivalent circuit. Thus $Q_{right} = \sqrt{50/31.8778 - 1} = 0.7539$. Similarly, $Q_{left} = \sqrt{R_{IN}/R_{eq} - 1} = \sqrt{50/31.8778 - 1}$

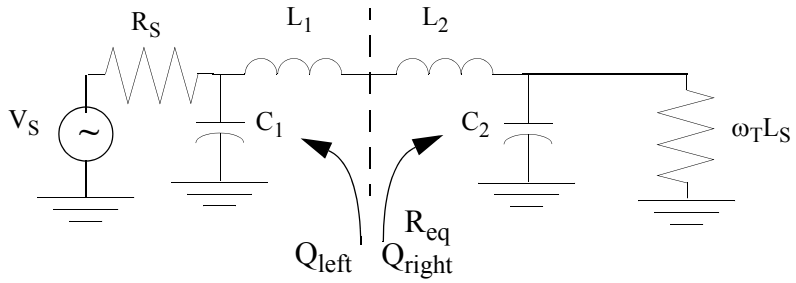


Figure 8: Input matching network

$= 0.7539$. The total input matching network Q is $Q_{in} = (\omega_o(L_1 + L_2))/R_{eq} = Q_{left} + Q_{right} =$ 1.5079.

The total inductance for π-matching network is

$$L_1 + L_2 = \frac{Q_{in}R_{eq}}{\omega_o} = \frac{1.5079 \cdot 31.8778}{2\pi \times 2.4\times 10^9} = 3.1876 \text{ nH}, \tag{11}$$

which sets the sum of external inductance and bond wire inductance.

The external capacitance is

$$C_1 = \frac{Q_{left}}{\omega_o R_{IN}} = \frac{0.7539}{2\pi \times 2.4\times 10^9 \times 50} = 1pF. \tag{12}$$

In summary, hand calculations for the input impedance, narrowband RF gain, noise figure, and transformer matching networks were used to set the design variable range for the synthesis. In addition to these specifications, the synthesis runs also included power and linearity specifications, however, these were not used to guide the choice of design variable ranges.

3. Synthesizing the circuit

3.1 NeoCircuit

NeoCircuit 1.3 [19] includes a synthesis engine, communication interfaces to commonly used circuit simulators, and a results analysis capability within Matlab. It was used for the sizing the circuit elements in the LNA and mixer circuits. As described above, the first step was choosing the circuit topology. Each of the device parameters is then defined as a design variable (or an equation combining several design variables) or a constant value (in this thesis no constant values were used). The ranges for each of the design variables are then defined. Next, the test bench circuit and the appropriate circuit analysis setup that is to be used to simulate and evaluate circuit performance is defined. After that, NeoCircuit's RF computation functions are used to extract scalar values from simulation waveforms, and to set the circuit goals. Finally, the designer sizes the design using NeoCircuit's synthesis capability.

3.2 RF circuit synthesis using NeoCircuit

The synthesis of RF circuits tends to take between half a day to two days and often needs to be repeated based on the quality of the synthesis results generated. One of the focus issues in this thesis was to identify potential time saving techniques. Some of the time saving approaches used are listed below:

- The periodic steady state (PSS) and transient (TRAN) analyses were avoided as they require long simulation times. Instead, S-parameter (SP) or AC analysis were used if possible. If this was not possible, a synthesis run that only included these faster analysis was first run, and the best resulting circuit was then used to evaluate the non-linear transient specifications. If they met their specifications, no further work was necessary. If they did not, a subsequent synthesis run that included the slower simulation analyses was run. An example of how transient analysis was avoided is described for power evaluation in section 2.2.2.
- NeoCircuit works best when it has design freedom, thus all the device element parameters were set by design variables (only the bond wire inductances had fixed values as they are physically constrained in any practical implementation). If fewer design variables are used, there is increased probability of conflict between the design goals.
- If NeoCircuit was unable to meet all the target goals, the goals were modified a little bit. A

subsequent NeoCircuit run tended to result in a circuit that meets the goals. This changes the infeasible path that NeoCircuit takes in its optimization process. Another similar approach that was taken was adding circuit elements that don't significantly change the total circuit operation.

- As the synthesis engine evaluates circuits that may have very large Q (depending on the inductor and capacitor choices made during synthesis), large RF input amplitudes tend to cause the transistor models to break down, particularly for IIP3 and 1 dB compression evaluation. Practical RF input power is between -20 dBm and -130 dBm, thus -30 dBm should be used instead of 10 dBm RF input.
- As noted in section 2.1.1, matching networks with many degrees of freedom are used. Without this freedom it is hard to satisfy the design goals.
- It is important to verify the units of the values (e.g. dB or dBm or magnitude or real number) produced by NeoCircuit computations with manual circuit simulation. NeoCircuit does not offer the flexibility of units found in many circuit simulators, leading to potential source of confusion.

3.3 Example synthesis process

3.3.1 Design variables

Figure 9 shows the SiGe5HP LNA circuit with arrows indicating the circuit elements NeoCircuit could size. The fixed elements include the bond wire inductance, and the resistance used to model the Q of the on-chip inductors. 16 design variables was chosen for the optimization with finite range from hand calculations.

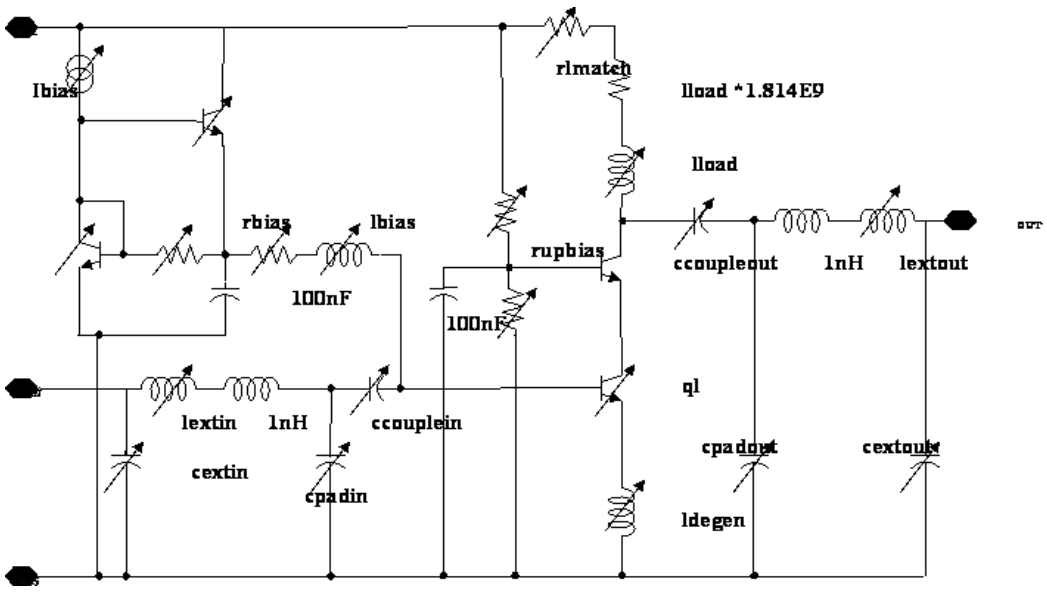
3.3.2 Design goal change during the optimization

Figure 10 shows the evolution of the circuit performance parameters as they move towards their specified targets in a NeoCircuit synthesis run. In this run, 102 evaluations were performed; each evaluation comprised of a circuit simulation followed by an Octave or Matlab computation that processed the simulation results to generate the target value. In this run it took 3 hours for NeoCircuit to meet targets.

3.4 Bias circuit revisions

The bias circuit for the Bipolar LNA is different from MOS LNA because of its impact in noise

generation. The basic difference is that the base current of the bipolar input flows through bias resistor, so some voltage drop is inevitable. So the bipolar bias circuit had to be modified, taking S_{11}, gain and noise



(a)

Name	Min	Step	Max
ccouplein	1e–12	1e-12	5e–11
ccoupleout	1e–12	1e-12	5e–11
cextin	5e–13	5e-13	2e–11
cextout	5e–13	5e-13	2e–11
cinpad	6e–13	2e-13	8e–12
coutpad	6e–13	2e-13	8e–12
ibias	0.0005	0.0005	0.05
lbias	1e–08	1e-9	5e–08
ldegen	5e–10	1e-10	1e–08
lextin	5e–10	5e-10	5e–08
lextout	5e–10	5e-10	5e–08
lload	5e–10	5e-10	5e–08
ql	1e–06	1e-6	0.0002
rbias	100	100	1000
routmatch	0.5	0.5	20
rupperbias	100	100	10000

(b)

Figure 9: The SiGe5HP LNA showing (a) the circuit element variables and (b) the upper and lower bound of the design variables

figure into account.

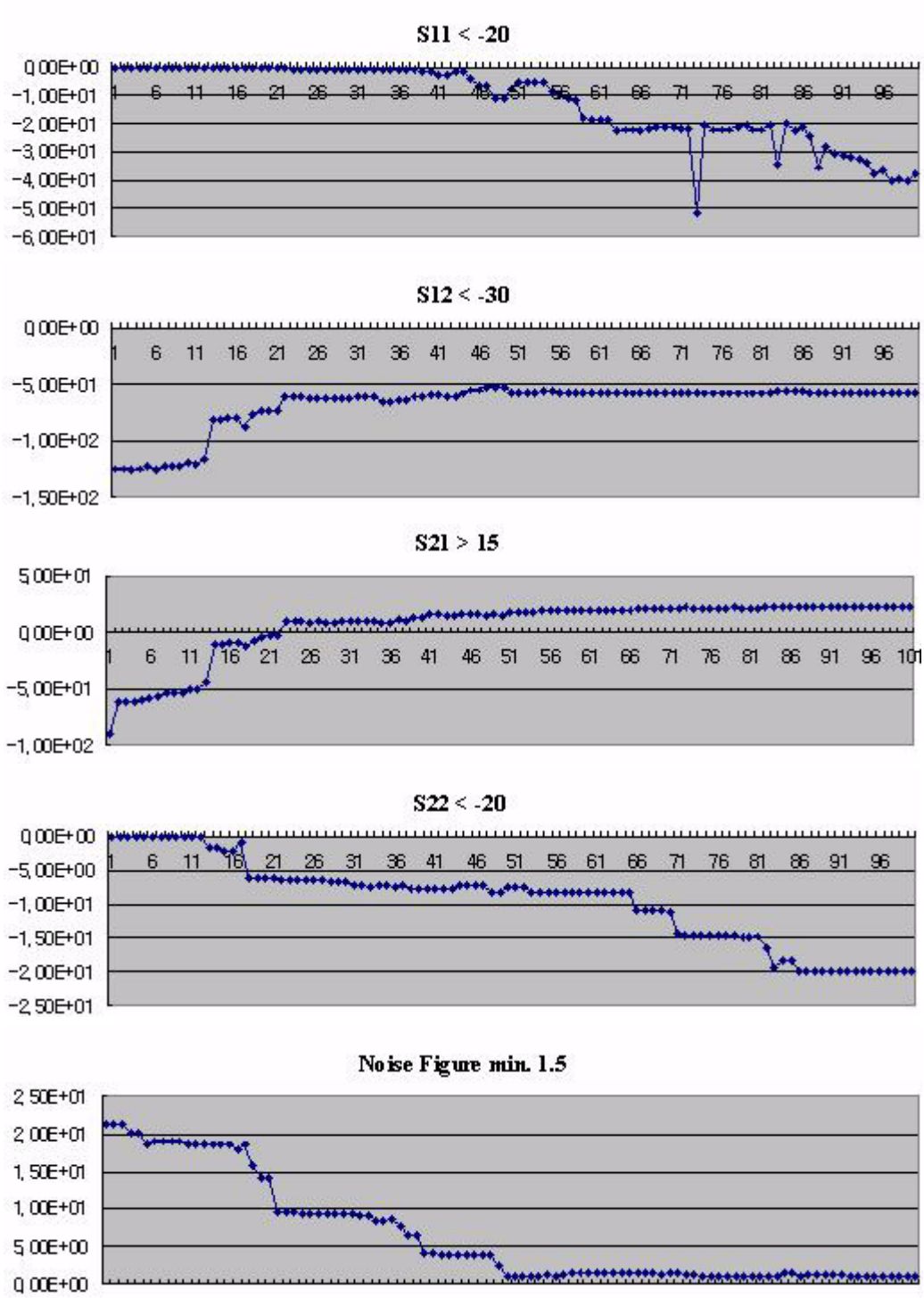


Figure 10: Goal value changes at each optimization step

3.4.1 Basic bias circuit for CMOS LNAs

In the CMOS LNA circuit topology of Figure 11, I_{bias}, M_{bias}, and R_{bias} sets the bias current in M_{drive} using a current mirror topology. At DC, basically no current flows through the gate of M_{drive}, thus a large value of R_{bias} is preferred to minimize the coupling of bias voltage noise into the gate of M_{drive}. C_{bias} is also added to low pass filter the bias voltage noise. A large R_{bias} also ensures that the RF signal sees a smaller impedance between the gate and source of M_{drive}. During synthesis R_{bias} was nominally set around 5 kΩ which is large compared to 50 Ω of input impedance.

Synthesis experiments of the CMOS LNA confirmed that the bias circuit hardly affected the noise figure at all three carrier frequencies.

3.4.2 Revised bipolar bias circuit

Figure 12 shows the bipolar equivalent of the CMOS bias circuit. As in the CMOS bias circuit, R_{bias} must be large enough to decouple Q_{bias}'s noise source from the Q_{drive}'s base. As the base current of Q_{drive} flows through R_{bias}, a voltage drop appears across R_{bias} resulting in a difference between the reference voltage of Q_{bias} and the base voltage of Q_{drive}. This leads to I_{bias} being larger than the collector current of Q_{drive}. These trade-offs make it difficult to increase R_{bias}, and the resulting minimum noise figure obtained in the bipolar circuit is 5 dB for the three carrier frequencies investigated.

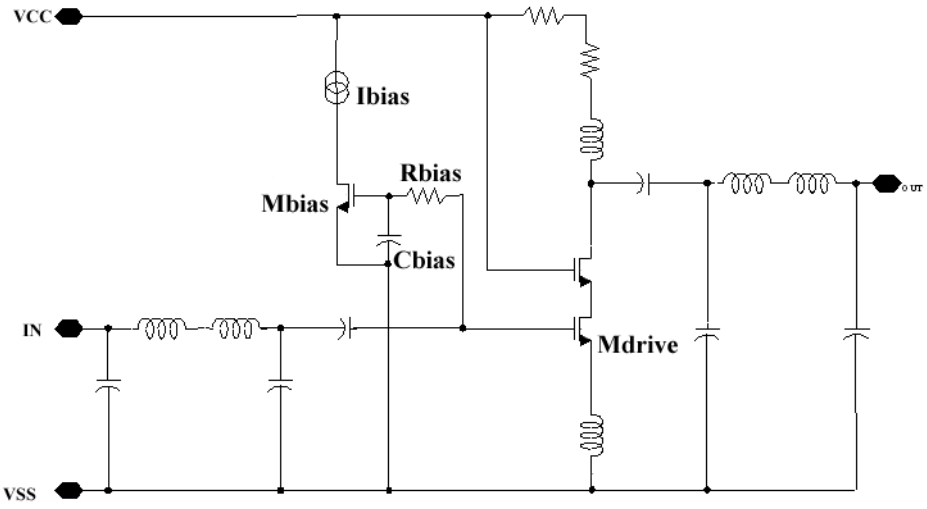


Figure 11: CMOS bias circuit

In contrast, several papers report sub 2 dB noise figure in SiGe LNAs [20][21]. An improved bias circuit was designed (Figure 13), in which a feedback transistor Q_{fb} and R_{bias1} was inserted to make a feedback path. R_{bias1} has the same value as R_{bias2}. The base current of Q_{drive} is compensated by R_{bias1} to guarantee I_{bias} and the collector current of Q_{drive} are almost same. The noise problem is still not solved because of large R_{bias2} is still needed to decouple the noise source in Q_{bias}. Large R_{bias2} means small Q_{drive} base current of which results in small ac current gain (of Q_{drive}). This low gain leads to a large noise figure. To increase the gain of $Q_{drive,}$ R_{bias2} must be reduced, which was not always possible for all the carrier

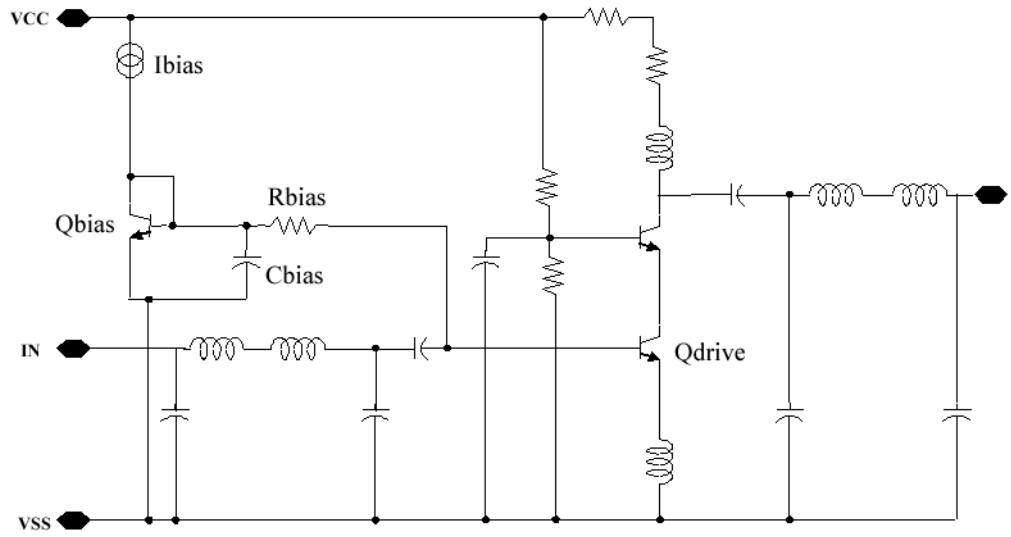


Figure 12: Simple bias circuit for SiGe LNAs

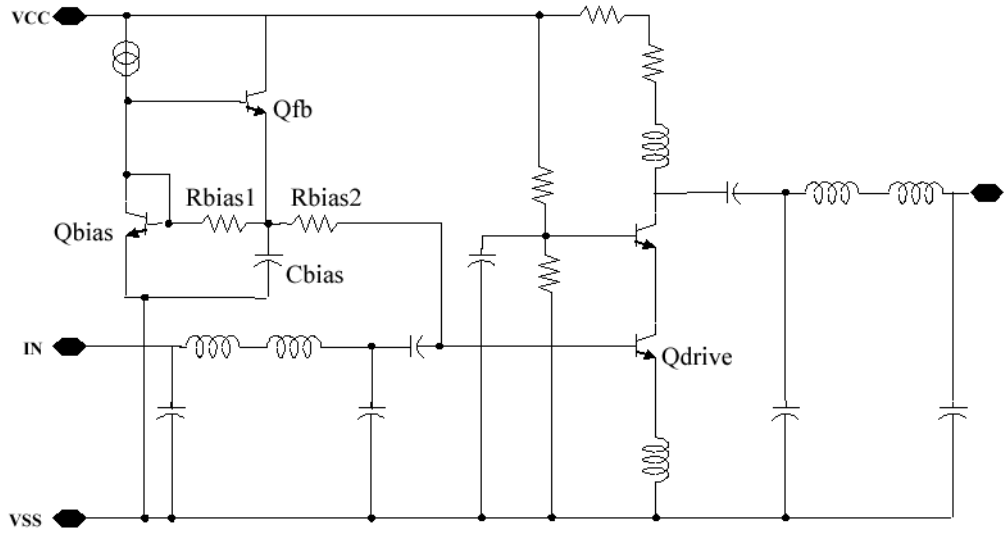


Figure 13: Bias circuit using feedback for SiGe LNAs

frequencies. Using this circuit, the noise figure was reduced to below 3 dB for all three carrier frequencies, but is still high compared to published reports.

At this point a further improved bias circuit that blocks noise from the bias generator from reaching Q_{drive} at RF frequencies was added, as shown in Figure 14. The blocking element, L_{bias}, prevents ac noise coupling. When this circuit is optimized using the S_{11}, S_{21} and noise figure constraints, R_{bias2} becomes very small (about 100-200 Ω) while noise transfer blocking L_{bias} is very large (about 20 nH-50 nH). The resulting noise figure of the bipolar LNA using the bias circuit of Figure 14 was about 1 dB to 1.5 dB for all three carrier frequencies. A large L_{bias} has large ac impedance to block the noise transfer but 50 nH is too large to achieve in practical design. L_{bias} must be traded-off with larger R_{bias} for practical layout that meets the desired noise figure.

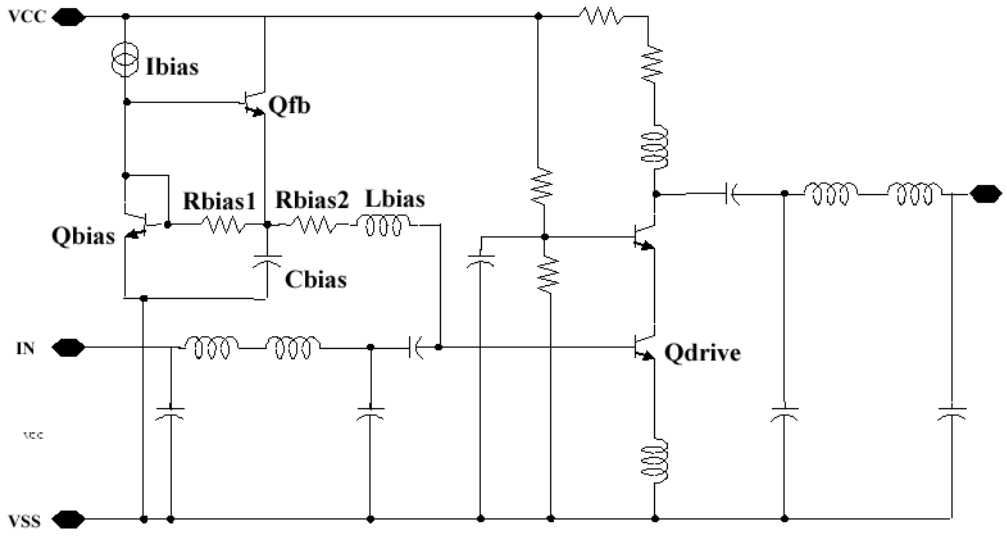


Figure 14: Bias circuit using feedback and blocking inductor

4. Local Power Disturbance S-parameter (LPDS) method for IIP3

4.1 Background

IIP3 calculation usually takes longer time than any other RF simulations. The typical method to determine IIP3 is a two tone test [18]. Two tone testing has a long history dating from the early days of RF engineering. For this discussion f_1 and f_2 are the two signals input into the device Δf is the frequency separation between the tones as shown in Figure 15. The third-order intermodulation (IM) products occur at a frequency of $2f_1 - f_2$ and $2f_2 - f_1$ show up as extra components Δf above and below the two input frequencies.

There are two primary ways to compute IIP3 in a simulation environment. In the first approach, the input power is swept, and the fundamental (either f_1 or f_2) and the third order IM product (either $2f_1 - f_2$

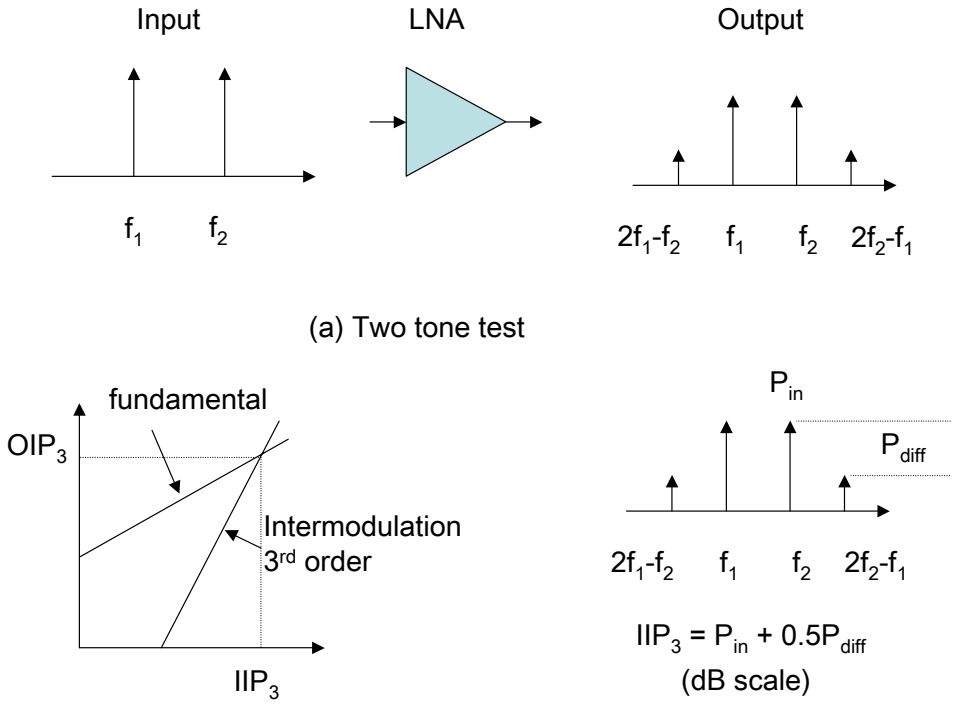


Figure 15: Two tone test to calculate IIP3

or $2f_2 - f_1$) are measured. The two measured quantities are plotted against the swept input power. The third-order intercept point or IIP3 is where the asymptotes of the two curves intersect. This can be implemented as a swept-PSS analysis in SpectreRF. The second approach involves taking the Fast Fourier Transform of the two tone output. This is implemented as a PSS in SpectreRF. Whatever method is used, the simulation times takes so much because many data points are needed. During the a typical synthesis run, IIP3 measurement usually took more than 80% of total optimization time.

4.2 The Local Power Disturbance S-parameter method

Lee suggests an analytical approach to evaluate IIP3 using a three point small-signal analysis [11]. In this section, a fast small-signal S-parameter simulation-based implementation of Lee's idea is proposed, called the Local Power Disturbance S-parameter (LPDS) method. The main idea behind this method is that a disturbance in the bias condition changes circuit gain. If the gain is exactly same for a small change in circuit bias, the IIP3 point would at infinity. If the gains are different, a finite IIP3 point exists.

Figure 16 shows the mechanics of this method. The ground for bias circuit (V_{SSB}) is separated from the RF ground (V_{SS}). A S-parameter analysis is performed around a disturbed V_{SSB}. To back out the gain due to the input matching network, the V_G output pin is added to measure Q_{in} exactly. Recall that Q_{in} was not exactly derived during hand calculations (primarily due to the complexity of π-matching network).

Figure 16(b) shows the testbench used to evaluate the intermodulation distortion. First, S-parameter analysis is performed between PORT0 and PORT1 to determine the gain of the entire circuit. Second, S-parameter analysis is performed between PORT0 and PORT2 to obtain the input transformer gain. The S-parameter analyses are an order of magnitude faster than even a single PSS analysis. Thus, this LPDS technique uses much less simulation time compared to either the swept-PSS method or PSS-FFT transient analysis method for finding IIP3.

4.3 Extracting equations for IIP3 calculations of LPDS

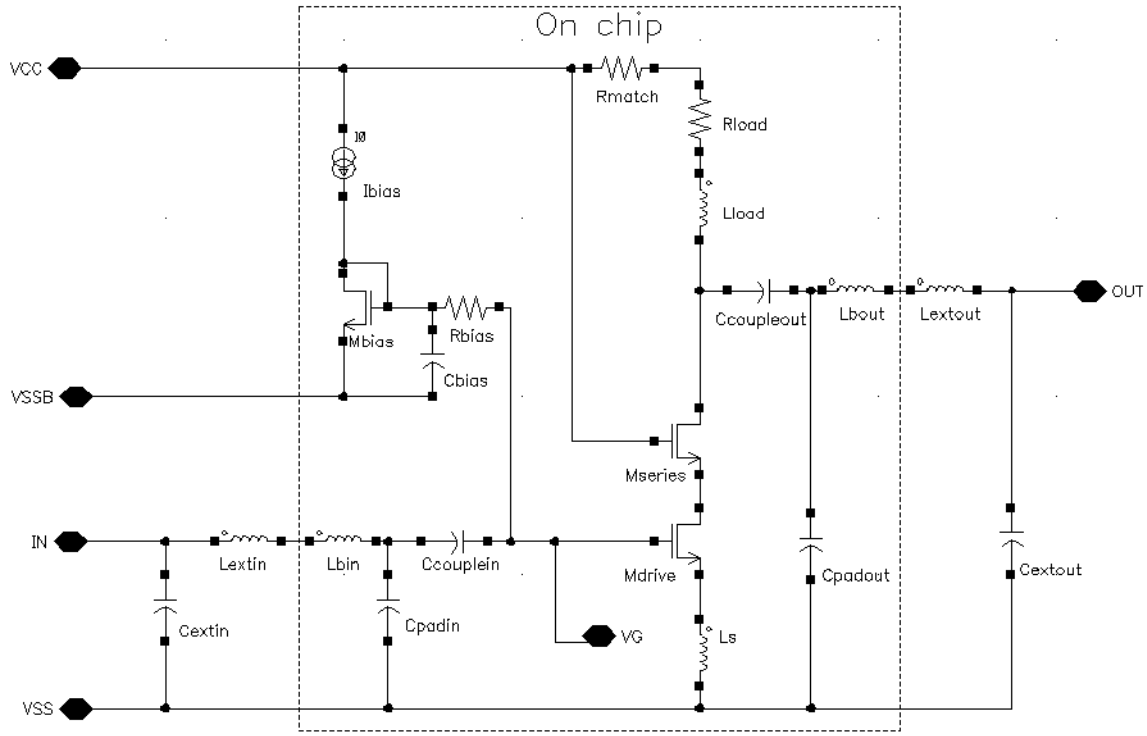
The derivation of IIP3 from the S-parameter analyses described below. The output voltage V_{out} for small voltage v around a dc bias point V_{DC}, can be obtained from a series expansion,

$$V_{out}(V_{DC} + v) = C_0 + C_1 v + C_2 v^2 + C_3 v^3 + \ldots . \quad (13)$$

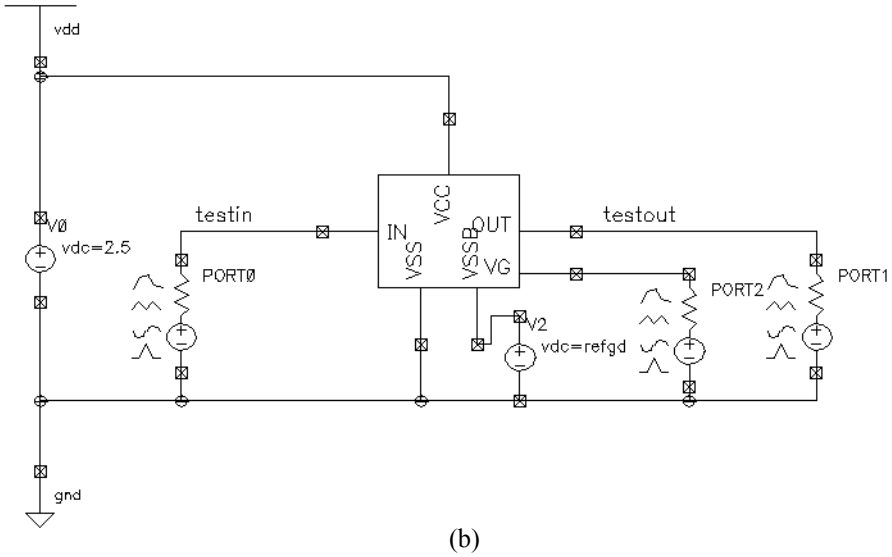
The gain is defined by

$$\left.\frac{dV_{out}}{dv}\right|_{v=0} = C_1 = \frac{S_{21}}{1+S_{11}} = extgain \tag{14}$$

The third harmonic term is defined by



(a)



(b)

Figure 16: The LPDS method: (a) topology and (b) S-parameter test bench

$$\left.\frac{d^3 V_{out}}{dv^3}\right|_{v=0} = 6C_3 . \tag{15}$$

To evaluate C_3, the relationship between the external voltage disturbance, v, and the internally transformed voltage v_g (the small signal voltage at the gate of M_{drive}) must be known. This relationship is the transformer gain,

$$intgain = \frac{v_g}{v} \tag{16}$$

which can be obtained from an ac analysis (or an S-parameter analysis with PORT2 as output port, in which case a two port voltage gain with arbitrary load and source impedance is needed). If v is small enough, C_3 can be approximated as

$$C_3 = \left(\frac{\left.\frac{S_{21}}{1+S_{11}}\right|_{v=-V_G} + \left.\frac{S_{21}}{1+S_{11}}\right|_{v=V_G} - 2\left.\frac{S_{21}}{1+S_{11}}\right|_{v=0}}{6V_G^2} \right) intgain^2 \tag{17}$$

where V_G is the gate voltage of the drive transistor. By definition of IIP3 (from [11]) $IIP3 = (2/3)\left|C_1/C_3\right|(1/R)$ where R, the real part of the input impedance, can be calculated as $R = R_S \cdot Re((1-S_{11})/(1+S_{11}))$ from R_S, the input port (PORT0) source resistance (which is set to 50 Ω in the test bench).

Thus, IIP3 can be computed by substituting into the definition of IIP3, [11]

$$IIP3 = \frac{2}{3}\frac{extgain}{R_S \cdot C_3 \cdot Re\left(\frac{1+S_{11}}{1-S_{11}}\right)} \tag{18}$$

Thus, each IIP3 computation only needs an two S-parameter analyses: one from PORT0 to PORT2 for (16), and a design variable swept S-parameter from PORT0 to PORT1 (with the ground voltage being swept, at the fixed fundamental frequency — this is in contrast to traditional S-parameter sweeps which sweep frequency). As the ground voltage of the bias transistor is swept, the gate voltage of the drive transistor changes in identical fashion since the V_{GS} of the bias transistor remains fixed by I_{bias}. The primary assumption in this method include a small value of v

in the series expansion which implies that the IIP3 extrapolation point is $-\infty$ (usual IIP3 measurements use a -30 dBm extrapolation point).

4.4 Verification of the LPDS method

Figure 17 shows the dependence of S-parameters with local power variations. In this analysis, *refgd* is the value of the local ground voltage V_{SSB}, and the IIP3 values on the graph are measured using the swept-PSS method. The S_{21} parameter curve with larger IIP3 (lower curve) also shows larger radius of curvature. This flatter curve implies lower C_3, which maps to higher IIP3 in (18) as expected. Intuitively, if gain changes rapidly with a change in the bias voltage, the circuit's linearity must be poor.

Table 1 and Table 2 details the IIP3 calculations detailing LPDS method for two example cases. The S-parameter and *extgain* columns are represented as radius and angle in the complex plane. $d(extgain)/dv$ is a cartesian complex number obtained from finite difference of the *extgain* column. The remaining columns are magnitudes of the complex numbers. A S-parameter analysis with PORT2 as an output port provides the internal gain of 1.37 for example 1 and 1.14 for example 2. The numbers in the table can be inserted into equation (18) to obtain IIP3 for the examples,

$$IIP3 = \frac{2}{3}\frac{6.3411}{945.48 \cdot 45.08} = 9.9182 \times 10^{-5} \approx -10.03 dBm, \tag{19}$$

$$IIP3 = \frac{2}{3}\frac{5.7261}{239.89 \cdot 51.58} = 3.0851 \times 10^{-4} \approx -5.1 dBm \tag{20}$$

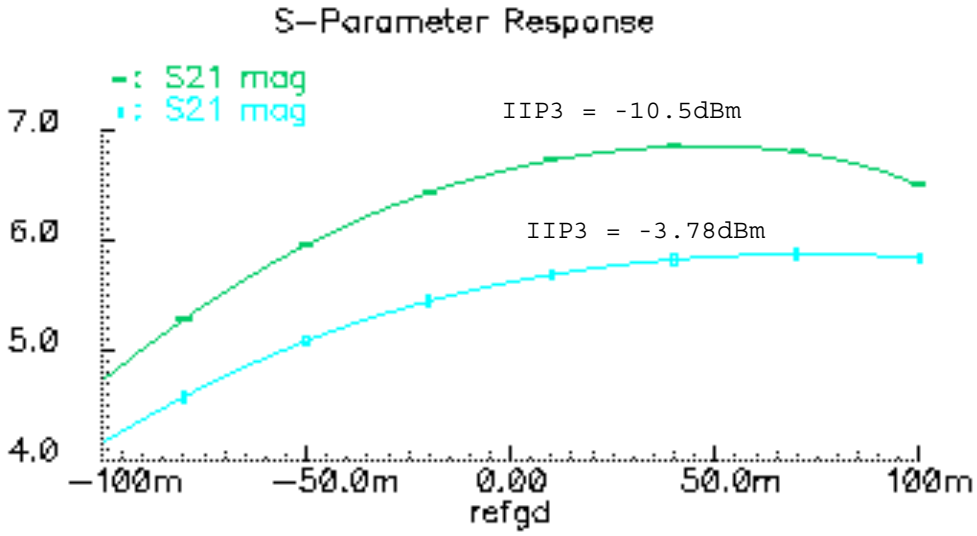


Figure 17: S-parameter response to Local Power Disturbance

The calculated values can be compared to the swept-PSS results shown in Figure 17, and are within 5-20% accurate. Computation functions that implement the LPDS method were not completed in time to use for synthesis, thus the results presented in the remainder of this thesis use the swept-PSS SpectreRF analysis for IIP3 evaluation.

Table 1: Example 1 LPDS Verification

V_{SSB}	S_{21}	S_{11}	$1+S_{11}$	*extgain*	$\frac{d}{dv}extgain$	C_3	R
-5mV	6.608 ∠176.9°	0.0841 ∠50.79°	1.0554 ∠3.55°	6.2671 ∠173.34°			
					-14.44 +3.92i		
0V	6.655 ∠176.9°	0.08215 ∠54.8°	1.0495 ∠3.65°	6.3411 ∠173.24°		1.37^2* 503.75	45.08
					-14.00 +6.40i		
5mV	6.696 ∠176.8°	0.08017 ∠58.73°	1.0493 ∠3.7626°	6.4144 ∠173.03°			

Table 2: Example 2 LPDS Verification

V_{SSB}	S_{21}	S_{11}	$1+S_{11}$	*extgain*	$\frac{d}{dv}extgain$	C_3	R
-5mV	5.584 ∠−132.9°	0.07357 ∠−102.2°	0.9871 ∠−4.170°	5.6570 ∠−128.7°			
					- 9.8932 -9.7797i		
0V	5.623 ∠−132.8°	0.07124 ∠−106.6°	0.9820 ∠−3.988°	5.7261 ∠−128.8°		1.14^2* 184.59	51.58
					-9.3443 -9.0377i		
5mV	5.658 ∠−132.7°	0.06958 ∠−111.1°	0.9771 ∠−3.808°	5.7906 ∠−128.9°			

5. Synthesis Results and Discussion

A single synthesized LNA is first presented to verify that the synthesized circuits meet the target specifications. Next, simulations of all the synthesized LNAs are presented without taking IIP3 into consideration, to compare the resulting gains, noise figures and power consumption. The IIP3 of the 2.4 GHz LNA design for selected CMOS and SiGe process was then analyzed (by simulation) to develop an understanding the non-linearities in the different processes. The same 2.4 GHz designs were re-synthesized to meet the same IIP3 target, to show how the other specifications change when IIP3 becomes the most important target. Finally, all the LNA results are summarized in one graph and a second graph presents similar results for the mixer designs.

5.1 Synthesis example

The TSMC 0.25 μm, 2.4 GHz synthesized circuit is analyzed to show the noise figure and S-parameters. Figure 18 shows NF and NFmin for the 1.9 GHz to 2.9 GHz frequency range. NF was not minimum at 2.4 Ghz which means that other specifications such as S_{11}, S_{21} and power has dominated the NF optimization. Note that NF is not far from minimum value.

Figure 19 shows the S-parameter for the 1.9 GHz to 2.9 GHz frequency range. The S_{11} and S_{22} parameters are resistive at 2.4 Ghz, but have reactance at other frequencies. S_{12} is independent of

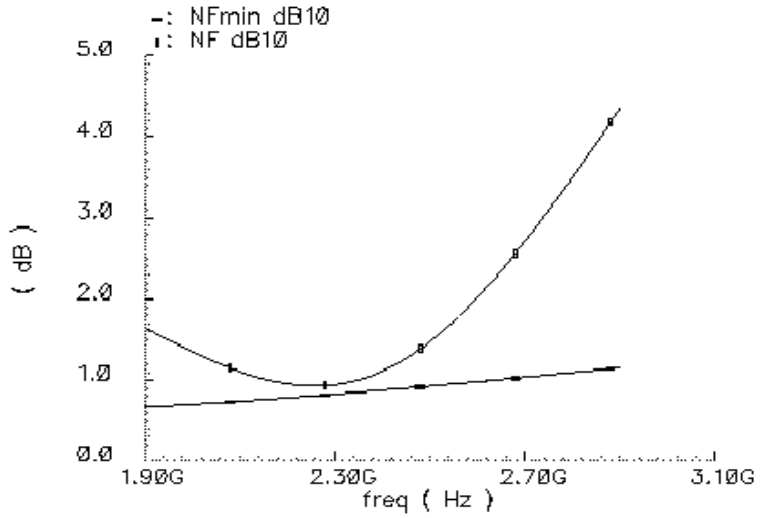


Figure 18: Noise figure of TSMC 0.25 μm 2.4 GHz LNA

frequency and S_{21} has a phase delay from the input. The S-parameters indicate that the synthesized CMOS LNA is operating normally.

5.2 Comparisons between synthesized LNAs

The LNA topologies described in section 2.2 were synthesized for each of the five processes and three carrier frequencies. These runs only considered the S-parameter, noise figure and circuit power specifications. In all the runs, both the circuit power was minimized and noise figure was minimized constraining the S-parameters (S_{11} < -20 dB, S_{12} < -30 dB, S_{21} > 15 dB and S_{22} < -20 dB). The resulting synthesis results are plotted as bar charts capturing power in Figure 20, noise figure in Figure 21 and narrowband gain in Figure 22. The results show that the SiGe processes have lower power consumption, while noise figure and gain are very similar across all the processes. From Figure 20, the TSMC 0.18 µm process has comparable power consumption with the SiGe processes. Also, each CMOS process shrink brings with it greatly improved LNA power consumption.

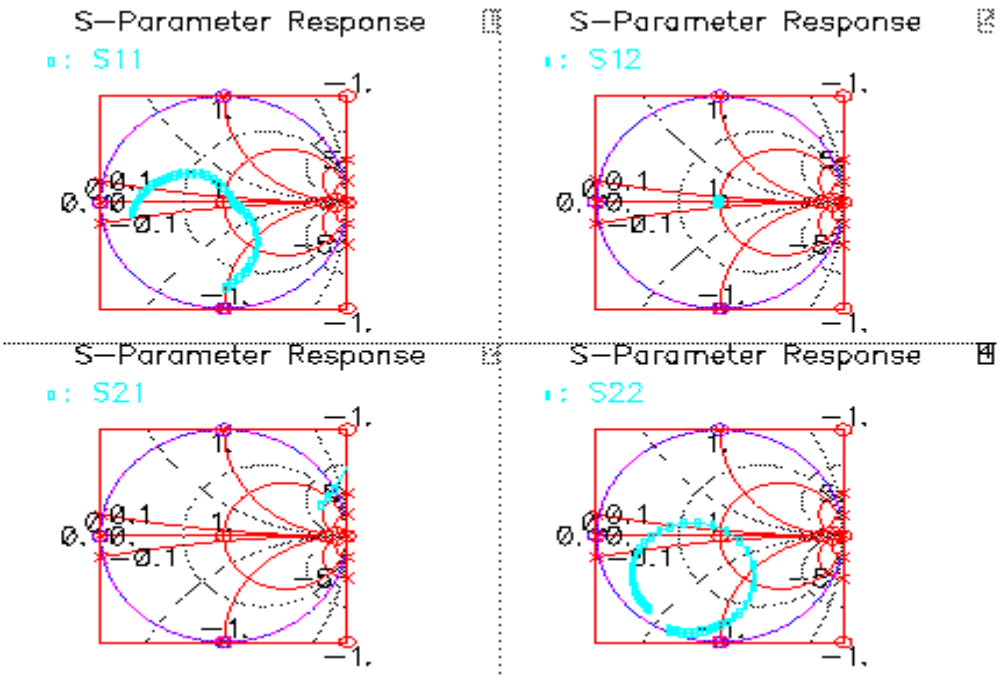


Figure 19: S-parameter of TSMC 0.25 µm 2.4 GHz LNA as a function of frequency from 1.9 GHz to 2.4 GHz

5.3 IIP3

5.3.1 Post-synthesis LNA IIP3 simulation

The IIP3 specification target was omitted during the synthesis of the fifteen LNAs in this thesis for reasonable synthesis run times. The IIP3 of two selected synthesized LNAs described in section 5.2 was computed via swept-PSS simulation. Figure 23 compares the IIP3 for the 2.4 GHz design for the TSMC 0.25 µm and SiGe5HP processes. The IIP3 of the TSMC 0.25 µm was much smaller than the SiGe5HP process. As larger IIP3 indicates better linearity, the SiGe process would be preferable.

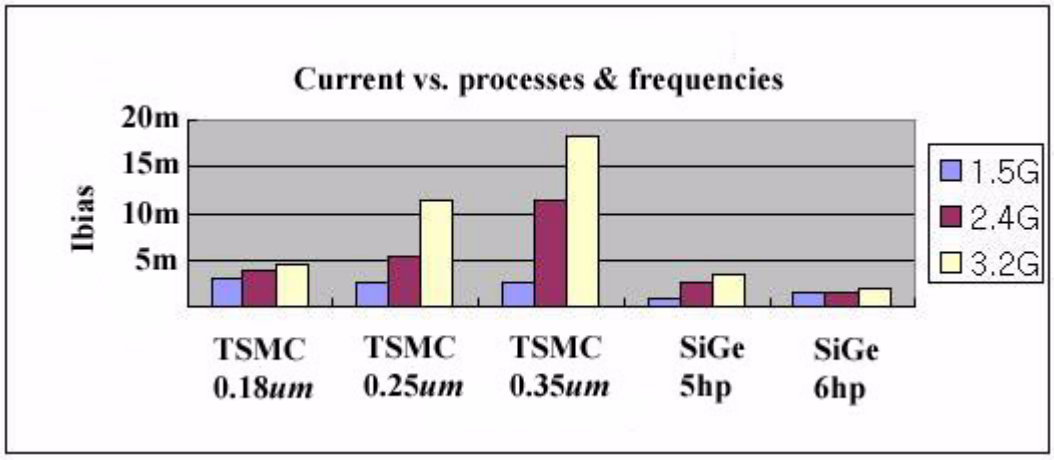


Figure20:

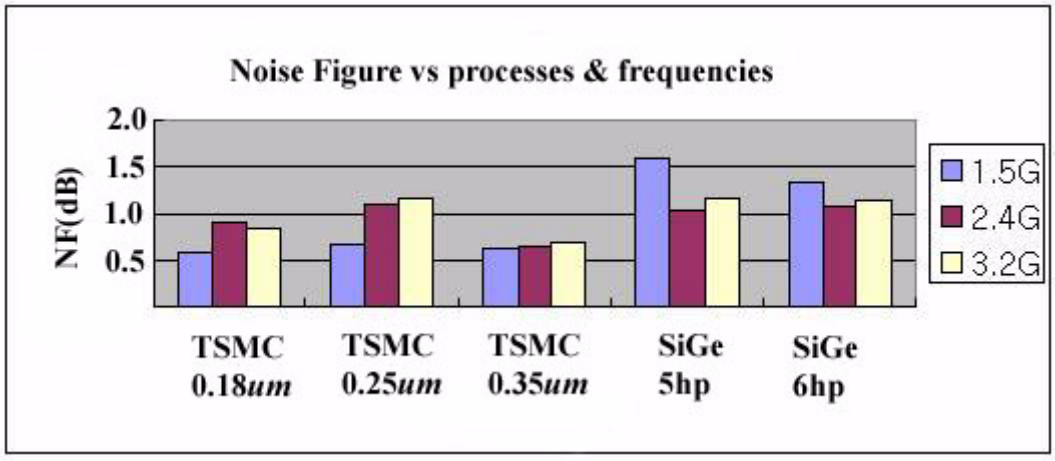


Figure 21:

5.3.2 Optimization with IIP3 goal

For a one-to-one comparison of the 2.4 GHz LNAs detailed in section 5.3.1, the CMOS LNA was re-synthesized to meet the better IIP3 value obtained in the bipolar design. This should show how the other specifications will change when IIP3 becomes the most important target. In the first try, the dual objectives of minimizing bias current and minimizing noise figure that was used for all the synthesis runs in section 5.2 was used to guide the synthesis. No feasible designs were found to simultaneously meet a $IIP3 > -5$ dBm constraint and a $NF < 1.5$ dB constraint. A second try, with the noise figure constraint replaced by the IIP3 constraint was attempted. Following synthesis the NF value was calculated by

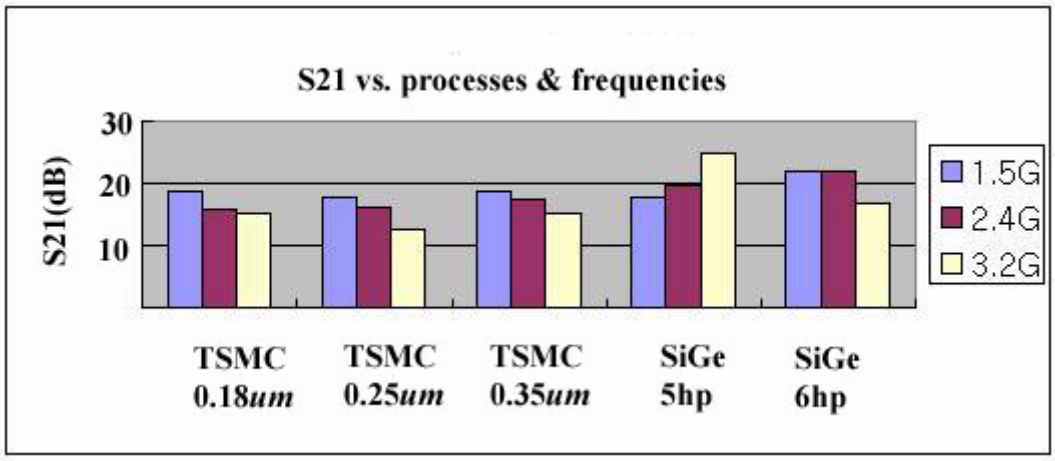
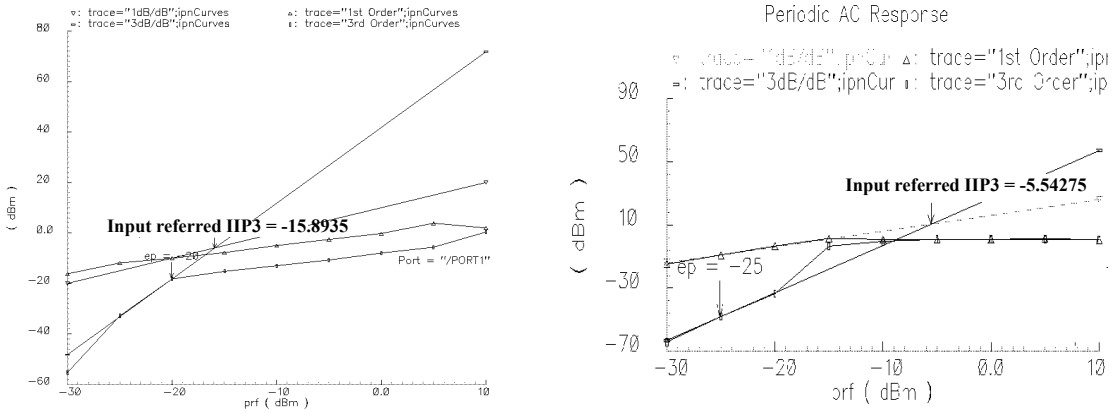


Figure 22:



(a) TSMC CMOS 0.25um (b) SiGe 5hp

Figure 23: IIP3 comparison between TSMC 0.25µm and SiGe5hp for 2.4 GHz

simulation. The resulting circuit performance values and design variables with the noise figure constraint and with the IIP3 constraint are reported in Table 3.

The synthesis which included the IIP3 constraint took about 1.5 days. The results show that I_{dc_goal} measuring the bias current increased from 5.5 mA to 12.5 mA. By inspection of the difference between the resulting design variables, the width of gate (w_{drive}) increased from 550 µm to 1100 µm. This implies that the Q of the input π-matching network decreased and active stage gain had to be adjusted by increasing the size of the gate width. The noise figure after synthesis with the IIP3 synthesis target was calculated by SpectreRF to be 1.46 dB for the TSMC 0.25 µm process. The noise figure increased as IIP3 increased. Thus, in the CMOS LNA, the synthesis is trading off IIP3 with NF.

5.3.3 LNA IIP3, NF, and Power Comparisons

As in section 5.3.1, the LNAs synthesized in section 5.2 were simulated using swept-PSS after

Table 3: The change of goals and variables after IIP3 optimization

NF optimization

Goals				
Met	Name	Current	Dir	Target
YES	s11_goal02524	-21.7074	<	-20
YES	idc_goal	0.0055	min	0.01
YES	s21_goal02524	16.4625	>	15
YES	s12_goal02524	-31.4344	<	-30
YES	s22_goal02524	-23.1653	<	-20
YES	nf_goal02524	1.11233	min	1.5

-->

IIP3 optimization

Goals				
Met	Name	Current	Dir	Target
YES	s22_goal02524	-22.1357	<	-20
YES	s12_goal02524	-30.9363	<	-30
YES	idc_goal02524	0.0125	min	0.015
YES	s11_goal02524	-22.7031	<	-20
YES	s21_goal02524	15.0001	>	15
YES	ip3_goal02524	-3.30305	>	-5

Design Variables			
Name	Min	Current	Max
ccouplein	1e-12	2e-12	5e-11
ccoupleout	1e-12	2.5e-11	5e-11
cextin	5e-13	2.5e-12	2e-11
cextout	5e-13	2.5e-12	2e-11
cpadin	6e-13	1e-12	1e-11
cpadout	6e-13	6e-13	1e-11
itotal	0.0005	0.0055	0.05
ldegen	5e-10	1.6e-09	1e-08
lextin	1e-09	3e-09	5e-08
lextout	1e-09	7e-09	5e-08
lload	5e-10	1.5e-08	5e-08
rmatch	0.5	3	50
wdrive	5e-05	0.00055	0.004

-->

Design Variables			
Name	Min	Current	Max
ccouplein	1e-12	3e-12	5e-11
ccoupleout	1e-12	7e-12	5e-11
cextin	5e-13	2.5e-12	2e-11
cextout	5e-13	5e-13	2e-11
cpadin	6e-13	6e-13	1e-11
cpadout	6e-13	6e-13	1e-11
itotal	0.0005	0.0125	0.05
ldegen	5e-10	1.1e-09	1e-08
lextin	1e-09	3e-09	5e-08
lextout	1e-09	8e-09	5e-08
lload	5e-10	5.5e-09	5e-08
rmatch	0.5	0.5	50
wdrive	5e-05	0.0011	0.004

synthesis was completed to calculate the IIP3 of each circuit. The resulting IIP3 values are presented with the noise figure (minimize, < 1.5 dB) and power (minimize, < 10 mA) performance parameters in Figure 24.

The CMOS processes show large variations at each carrier frequencies while SiGe processes show small variations. IIP3 increases as CMOS gate length and operating frequency increase at the expense of power consumption. IIP3 deterioration with deep submicron technologies has been reported [22][23] and coincides with the data in Figure 23. The large variation between the synthesized CMOS LNAs is due to large Q variations between the carrier frequencies. SiGe processes showed smaller variations with carrier frequency which means small change of the input matching network quality factor. CMOS Noise Figure decreases as the gate length shrinks. This can be explained by (6) with larger ω_T. The 6HP process had smaller power consumption compared to the 5HP LNAs. The TSMC 0.18 μm is competitive with SiGe

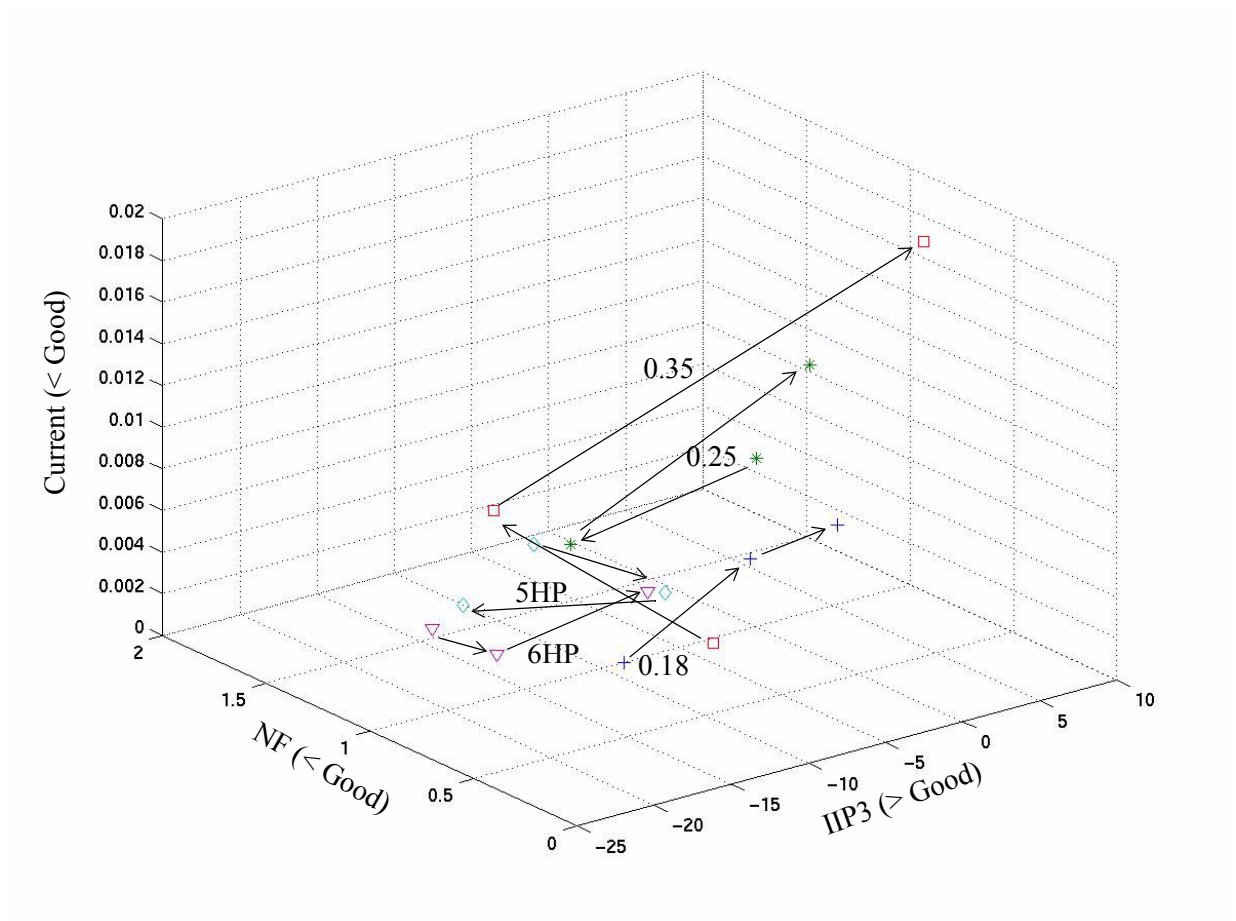


Figure 24: IIP3, NF and Current results of all LNAs of all processes and frequencies - Arrows represent the sequence of 1.5, 2.4 and 3.2 GHz

processes at moderately large current. Both these conclusions (increased suitability of newer CMOS processes for RF design and SiGe designs being better than CMOS designs for each process generation) have been reported by other researchers [3][16].

5.4 Mixer Synthesis

Mixer synthesis took 2 days for each carrier frequency because PSS was needed to simulate the down conversion and Periodic Noise (PNOISE) analysis with 30 sidebands of noise of internal node voltage to IF output [15]. The resulting designs did not change significantly between the RF carrier frequencies as the IF frequencies were always 50 MHz and the output loads remained identical (see test bench in Figure 3). As with the LNAs, IIP3 was calculated after synthesis with the design goal of current (minimize, <30mA), Noise Figure (< 15 dB), Conversion Gain (> 15 dB) and S_{11} (< -20 dB). The resulting performance parameters are plotted in Figure 25. The results of synthesized mixers follow the expected characteristics

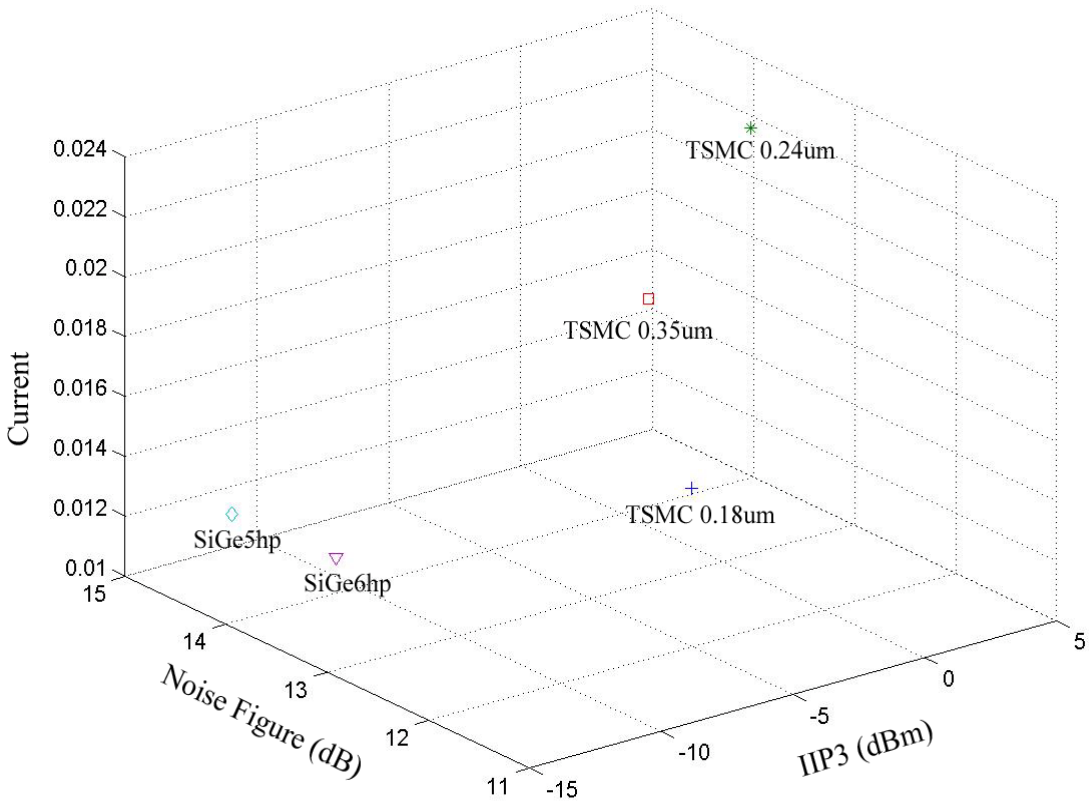


Figure 25: IIP3, Noise Figure and ICC of Mixers at 2.4 GHz (RF) and 50 MHz (IF)

of analog multipliers. SiGe processes showed lower operating current because they have a large transistor gain. CMOS processes show IIP3 deterioration and Noise Figure improvement as gate length shrinks.

5.5 Comparison Summary

The primary difference between MOS and Bipolar design is RF input impedance. MOS transistors have a capacitive input impedance and Bipolar transistor has a resistive input impedance. From the synthesis results, Q of input matching network and the gain of the drive device are traded of with noise figure and IIP3. In CMOS, Q must be reduced to increase IIP3 condition degrading the noise figure and overall gain. To increase gain, more power needs to be consumed by increasing drive transistor size. This degrades the efficiency of the CMOS device.

In the bipolar case, the matching network quality factor Q is low enough because the inherent gain of the bipolar is higher than MOS, leading to higher IIP3. More importantly, change in bipolar emitter area does not significantly change Q. So noise figure, gain and IIP3 can be optimized separately. The noise of the bipolar circuit is higher than its MOS counterpart at moderate RF carrier frequencies. This is mainly from the shot noise which was proportional to the current flow through the potential barrier.

6. Conclusions

In this research, the LNA and mixer topologies were identified for use in a synthesis-based exploration of the impact of process and carrier frequencies on RF IC design. The bipolar bias circuit was revised several times for minimizing Noise Figure with the help of NeoCircuit. The resulting SiGe LNA noise figures was reduced less than 1.5 dB. During the optimization, IIP3 calculations consumed significant simulation time leading to aborted synthesis runs. A faster approach based on Local Power Disturbance S-parameter (LPDS) method which only uses S-parameter analysis was introduced and verified by simulation examples.

Synthesis results showed that SiGe processes have good characteristics of power and IIP3 compared to CMOS processes, when all other design parameters meet the specifications. Analysis of the resulting synthesized designs showed that the relation of input Q and transistor size was dependent on process family, with SiGe process consuming lower power. Finally, SiGe 6HP is good for lower power consumption, long channel TSMC is better for large IIP3 while short channel TSMC is good for small Noise Figure. Finally 15 LNAs and 15 Mixers of TSMC 0.18 μm, 0.25 μm, 0.35 μm, SiGe5HP and SiGe6HP were designed at carrier frequencies of 1.5, 2.4 and 3.2 GHz.

6.1 Future Work

The 30 designs were synthesized over a period of 3 months, with significant concern about synthesis run times. This was appropriate as our focus was the understanding of process and carrier frequency evolution on RF IC design. Extending this work to generate designs with adequate confidence necessary for fabrication requires inclusion of detailed parasitic models for on-chip inductors, bond pads, and the power supply network. Additionally, for many wireless applications, the IIP3 design constraint may be very important. Other RF design specifications that should be added to the synthesis constraints include stability.

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