Design of a Variable Capacitance Sense Amplifier for use in a MEMS Probe-based Data Storage System

by

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Abstract

This thesis describes the design of a variable capacitance sense amplifier which is to be used in a MEMS probe-based data storage system being developed at Carnegie Mellon University. The basic operation of the data storage system and how a capacitive sensor is used is described. In order to achieve low noise requirements a sense amplifier system which uses correlated double sampling is designed. A folded cascode amplifier meets the needs of the correlated double sampling system. A chip is designed, submitted for fabrication and tested.

Acknowledgements

My first thanks go to my advisor, Professor Rick Carley for his many years of guidance and encouragement. An overwhelming debt of gratitude is due to my second reader, Professor Tamal Mukherjee whose suggestions greatly improved the caliber of this paper. Special thanks go to the Probe Group for their constructive feedback on my work and presentations, especially Art Davidson, Professor Jim Bain, and Suresh Santhanam. I would also like to thank those who have come before me for their suggestions and advice on what has already been done; Dave Guillou, Hao Luo, Jiangfeng Wu, Mike Lu and Wayne Loeb.

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Chapter 1

Introduction

Advances in fabrication technology have enabled the development of microelectromechanical system (MEMS) devices on silicon wafers. In particular, in the CMOS-MEMS process developed at Carnegie Mellon University, the mechanical structures are formed following commercial CMOS fabrication. This method enables MEMS devices to be produced at very low cost and integrated directly into the same chip as the circuitry they interact with [Fedder96]. MEMS devices are already widely used in many commercial applications such as accelerometers and various types of sensors [Nagel01].

One example of a system currently in development is a MEMS probe-based data storage system which involves using an array of MEMS probe tips for reading and writing bits on a plate of magnetic media [Carley01]. The media plate is suspended by springs over an array of actuators which hold the read/write probe tips as shown in figure 1.1. Each probe tip needs to move towards the media in order to apply a magnetic field to write a bit. When a tip moves past a bit that has been written, the cantilever beam of the actuator is deflected vertically by the force of the magnetic field of the bit pattern on the media which opposes the magnetic field of the tip. The position of each probe tip with respect to the media can be determined by measuring the capacitance formed between the actuator plate and the media. This distance can then be sensed to read bits and controlled to set the position for writing.

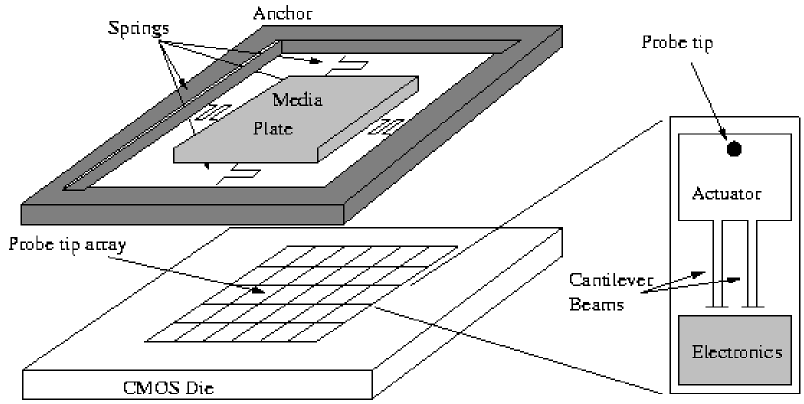


Figure 1.1 Conceptual diagram of data storage system using MEMS actuators.

This thesis presents a capacitive sense circuit for measuring the changing capacitance of an individual actuator in the MEMS probe based data storage system. The actuators' feedback control has been designed by others [Lu02, Wu02] and is not covered. Chapter 2 explains the design of the circuit and how it meets the constraints on noise, power consumption, and area. The results of simulations on the sensor are also explained in this chapter. The design of the chip that has been manufactured is detailed and the results from the testing of this chip are presented in chapter 3. Finally chapter 4 offers conclusions and suggestions for future work.

Chapter 2

Design

2.1 Capacitive Sense Circuit Overview

The basic structure of the circuitry surrounding the variable capacitor being sensed is shown below (figure 2.1). The capacitor formed by the media and the actuator plate (C_{sense}) needs to be electrically excited to produce a voltage signal that can be amplified, demodulated and processed.

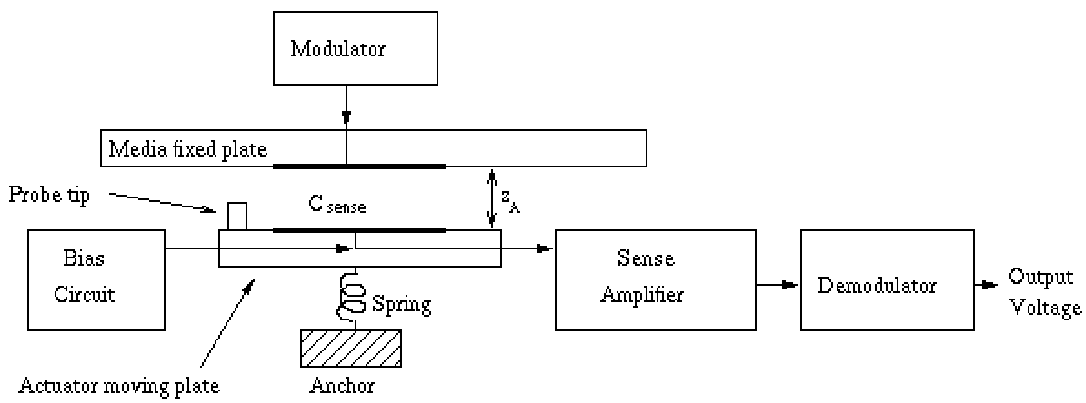


Figure 2.1 Capacitive position sensor architecture.

As the actuator is moved towards and away from the media C_{sense} changes inversely proportional to the distance between the media and the actuator plate. Measuring this changing capacitance provides a method for determining the distance between the two plates. This distance z_A varies between 300nm and 3μm in this design. This includes the height of the read/write probe tip and the space between it and the media.

The actuator, as shown in figure 2.2 (a) , is comprised of the plate which the read/write probe tip sits on that is suspended by two cantilever beams and is free to move in the z direction with a resonant frequency of approximately 10kHz. An SEM of such an actuator that has been designed by Dave Guillou and released in the poly-release process is also shown (figure 2.2 (a)) [Carley01]. From the SEM it is possible to see the comb drives used to electrostatically actuate the probe in the z direction. These are left off figure 2.2 (a) to simplify the schematic. The plate itself has a width (W_A) of 23.5μm and a length (L_A) of 27.5μm. When z_A is much less than the width and length of the plates, the capacitance can be between them can be defined as a simple parallel plate capacitor.

$$C_{sense} = \frac{\varepsilon_0 W_A L_A}{z_A} \tag{2.1}$$

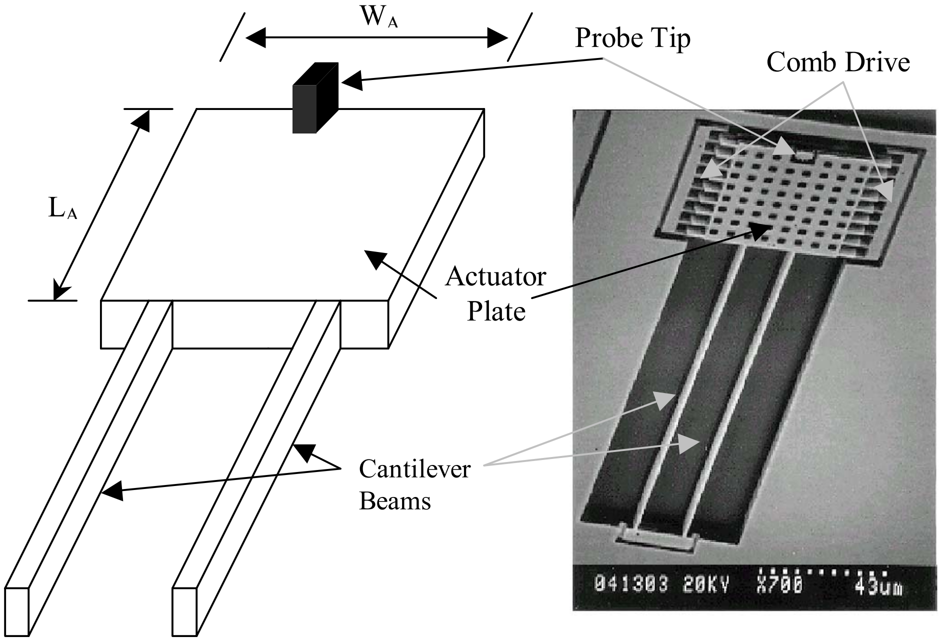


Figure 2.2 Probe (a) diagram of dimensions. (b) SEM of released actuator [Carley01].

There is an estimated parasitic capacitance of 10fF in parallel with the two plates which is extracted from simulation. Making the input node of the capacitance sensing amplifier close to the variable capacitor helps keep the parasitic contribution of routing capacitance as small as possible. Adding this parasitic capacitance to the variable capacitance implies the sensed capacitance can vary between 11.9fF to 29fF over the given range of z. Since the signal from this changing capacitance is very small, a low noise sensing scheme is necessary.

The bias circuit is needed to ensure the moving plate of C_{sense}, which is also the high impedance node of the sense amplifier, is biased to the proper DC voltage (shown in figure 2.1) [Guillou00].

The power budget for the entire data storage system is 1Watt. A data storage system comprised of 1000 probes operating simultaneously is considered in this research, which means each probe is allowed 1mW of power consumption. This power needs to be spread between sensing and control, so the power consumption for the sensor needs to be low, on the order of several hundred microwatts. An additional constraint laid on the sensor by the number of probes is the size of each cell, where a cell is comprised of a probe and its controlling circuitry. For a cell size of 100µm by 100µm where the probe takes up approximately 100µm by 50µm the circuitry must fit in the remaining 100µm by 50µm.

2.2 Noise Reduction Techniques

The dominating constraint on the sensor is the need to use small MOS devices for the sensing of the changes in capacitance to minimize the amount of parasitic capacitance in the circuit. Unfortunately, small MOS devices have a large level of $1/f$ noise. Therefore it is necessary to develop techniques to reduce low frequency noise. There are two main methods that have been explored for noise reduction in capacitance sensing systems [Enz96]: synchronous amplification, also known as chopper stabilization [Hsieh81, Loeb00], and correlated double sampling [White74, Lemkin99]. In this section both methods are presented and compared.

Chopper stabilization is a 3 step process wherein the signal being amplified is first modulated to a higher frequency range where $1/f$ noise is negligible. Next the modulated signal is amplified. Finally, the amplified signal is demodulated back into its original frequency range and high frequency artifacts introduced by the modulation are filtered out. The major advantage of this method is its operation in continuous time.

In correlated double sampling (CDS) two samples are taken and subtracted. The low frequency noise changes very little if at all between these two samples and is eliminated, leaving only the higher frequency signal being sensed and in the process acts as the demodulator for the signal.

While both methods successfully attenuate low frequency noise, CDS has several advantages over chopper stabilization including simplicity of implementing biasing, modulation, demodulation and the amplifier.

As mentioned in the previous section the input node of the capacitive sense amplifier is a high impedance node as it is connected to the sense capacitor and the gate of a MOS device. A DC path to ground needs to be implemented to control this node. It is nearly impossible to make large resistors on chip and smaller resistors add noise, so resistive biasing is not practical. Diodes are highly non-linear, so they can only be used at nodes with low signal swing.

Another possibility of biasing involves periodically resetting the high impedance node which unfortunately causes broadband noise to be under-sampled. The CDS approach is already a sampling system so it is easy to insert a reset phase during each sampling period. Additionally, this noise is correlated within a clock period and is largely cancelled by the subtraction phase. This is not the case in chopper stabilization and the addition of a reset phase interrupts the continuous time operation of the chopper stabilized system.

Another advantage of CDS over chopper stabilization is that the implementations of modulation and demodulation are less complex in CDS [Guillou00]. Demands on the amplifier and reconstructive filter for CDS are also less stringent. Fewer demands on the circuitry and less complexity in implementation typically imply fewer demands on number and size of devices, and power consumption, the two other constraints. For these reasons a capacitive sense amplifier has been developed that utilizes the correlated double sampling technique.

2.3 Correlated Double Sampling Circuit

There are many circuits that employ switched capacitor techniques to achieve correlated double sampling [Yoshizawa97, Huang96, Huang98]. A fairly common scheme is shown in figure 2.3. In this design the input is connected to the amplifier in the first phase and sampled at the output. The input is then grounded to sample the noise of the amplifier and the polarity of the feedback capacitor is inverted. The sample that was previously on the feedback capacitor is subtracted from the sample of the noise leaving only the desired signal. A major disadvantage of this system is the switching of the feedback capacitor. Due to the need for non-overlapping clocks, for a brief period of time there is no feedback on the amplifier. During this time it is possible for the output to spike creating undesirable glitches in the output signal. This is fixed by placing another capacitor C_{dg} across the amplifier as well. While this keeps the amplifier's output from spiking it introduces the problem of attenuation in the circuit.

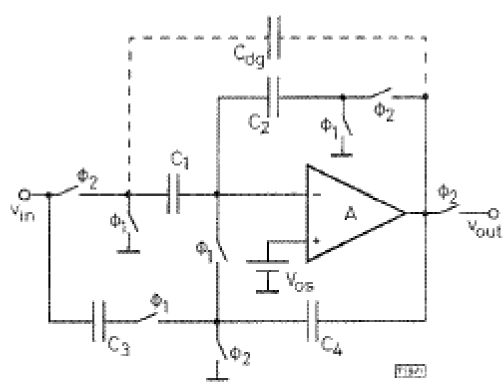


Figure 2.3 A correlated double sampling circuit utilizing switched capacitors [Yoshizawa97].

An alternate method of correlated double sampling utilizes two sample and hold circuits and a subtractor [Guillou00]. Rather than reversing the polarity of a single capacitor to perform subtraction, two individual samples taken from the sensing amplifier are applied to another amplifier in a subtractor configuration. Closely matching the positive and negative feedback loops of the subtractor helps reduce the amount of noise introduced by this stage of the system as described later in section 3.1. Additionally the feedback loops of both the initial sense amplifier and the subtractor are never opened limiting the adverse effect of output signal spiking. Although this method introduces a second amplifier that consumes more area and power, the subtraction stage can be shared amongst several probes as is discussed later in the thesis. The parasitic capacitance due to the c_{gs} of the input transistors and extracted interconnect capacitance can be ignored in the following analysis since their effect is reduced by the robust biasing technique.

There are four steps involved in the sampling process for this design (shown in figure 2.5). The clock signals Φ1 through Φ4 are non-overlapping clocks running at 4MHz as shown in figure 2.4. The modulation signals V_m- and V_m+ switch every two cycles of the clock (figure 2.4).

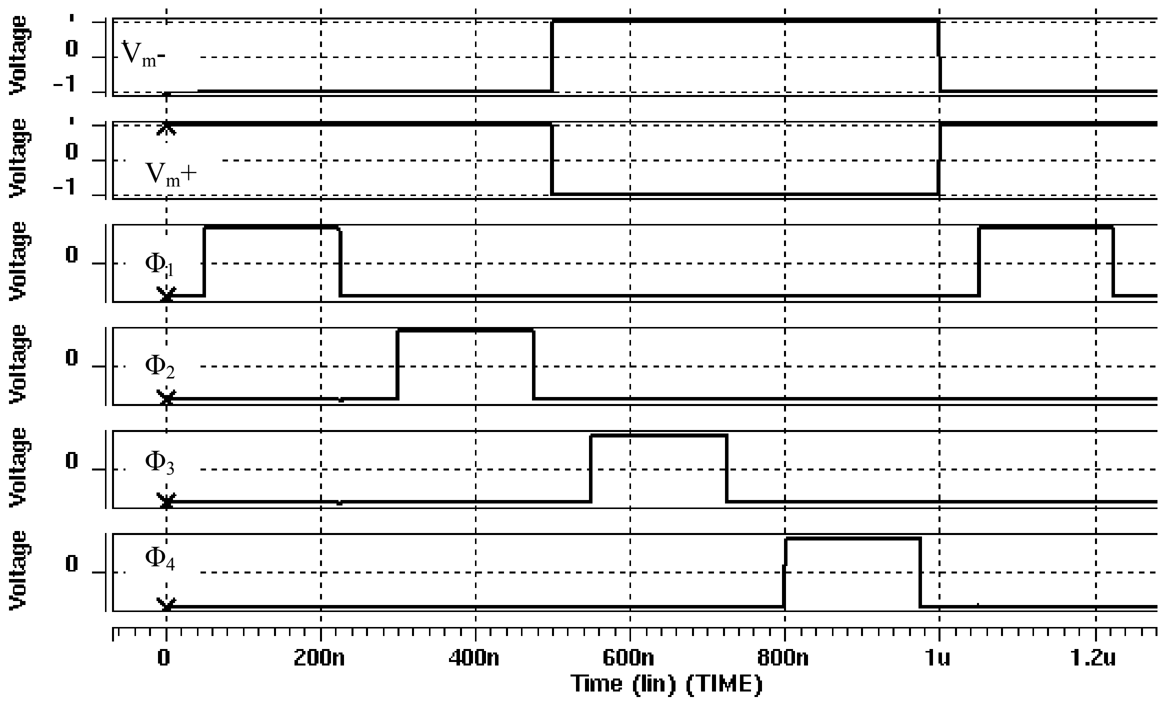


Figure 2.4 Non-overlapping clocks Φ_1- Φ_4 and modulation voltages.

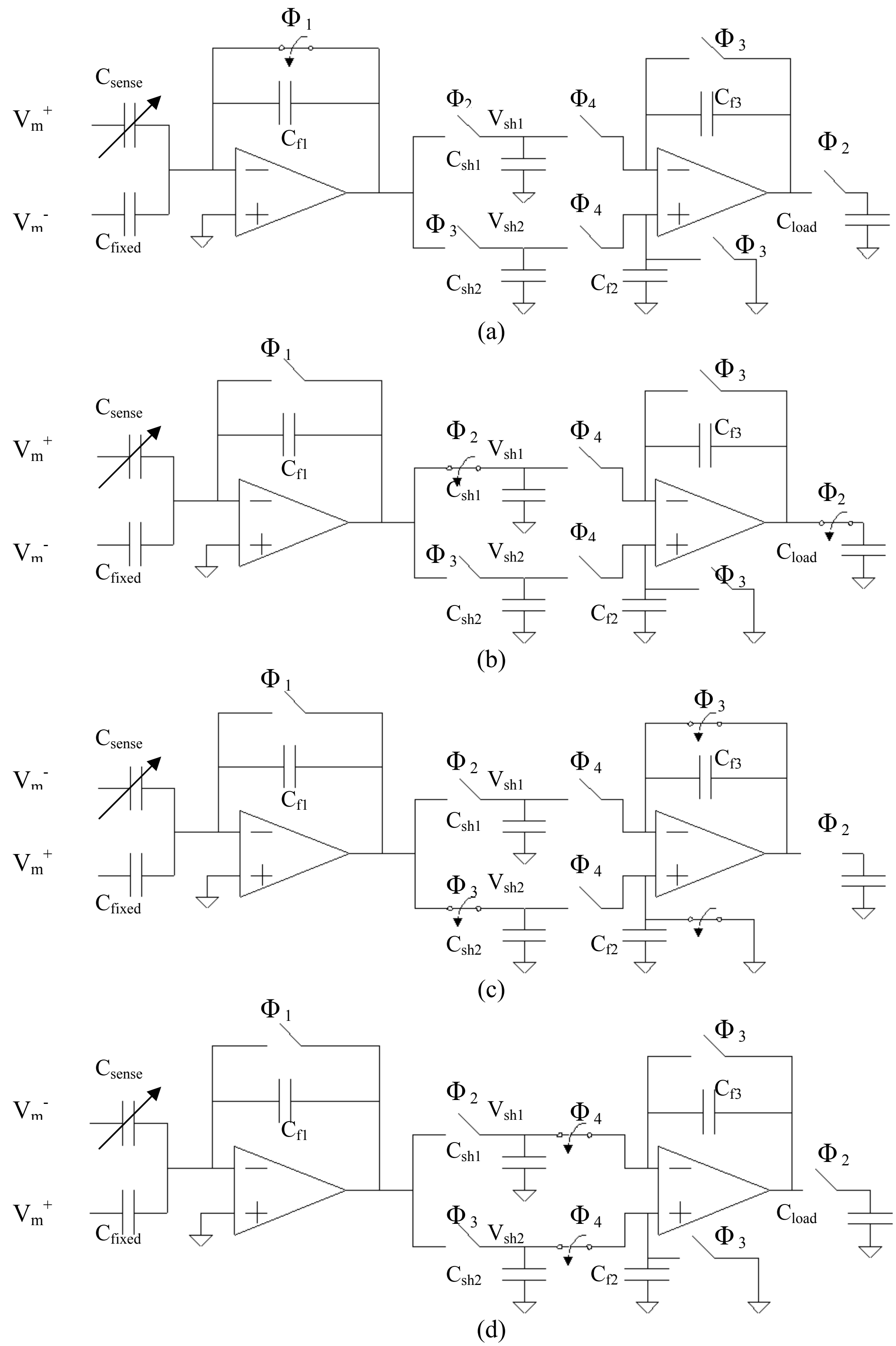


Figure 2.5 Four steps of sampling process. (a) initial reset. (b) positive sampling and output sampling. (c) negative sampling and subtractor reset. (d) subtraction.

During Φ_1 the initial sensing amplifier is reset forcing the output to zero. In Φ_2 a positive sample is taken and stored on C_{sh1}

$$V_{sh1} = -V_m \frac{\left(C_{sense}-C_{fixed}\right)}{C_{f1}} \tag{2.2}$$

where V_m is the voltage across the input capacitors or $V_m^+ - V_m^-$.

The modulation voltage across the input capacitors is reversed and the second sample is placed on to the second sampling capacitor, C_{sh2}.

$$V_{sh2} = -\left(-V_m\right)\frac{\left(C_{sense}-C_{fixed}\right)}{C_{f1}} \tag{2.3}$$

The negative feedback factor and negative modulation voltage cancel leaving

$$V_{sh2} = V_m \frac{\left(C_{sense}-C_{fixed}\right)}{C_{f1}} \tag{2.4}$$

Next these two sampled signals are subtracted and amplified to produce

$$V_{out} = -V_m \frac{\left(C_{sense}-C_{fixed}\right)}{C_{f1}}\left(\frac{C_{sh1}}{C_{f2}}\right) - V_m \frac{\left(C_{sense}-C_{fixed}\right)}{C_{f1}}\left(\frac{C_{sh2}}{C_{f3}}\right) \tag{2.5}$$

If C_{f2}, C_{f3}, C_{sh1}, and C_{sh2} are sized equally they cancel so in the final stage the sample taken is

$$V_{out} = -2V_m \frac{\left(C_{sense}-C_{fixed}\right)}{C_{f1}} \tag{2.6}$$

The factor of 2 produced in the polarity reversing of the modulation voltage provides a gain advantage. The output voltage with respect to z, the gap between the sense capacitor plate is

$$V_{out} = -2\frac{V_m}{C_{f1}}\left(\frac{\varepsilon_o W_A L_A}{z} - C_{fixed}\right) \tag{2.7}$$

By taking the first derivative of equation 2.7 with respect to z it is possible to find the sensitivity of the sensor at a gap of z_o,

$$\left.\frac{\Delta V_{out}}{\Delta z}\right|_{z=z_o} = 2V_m \frac{\varepsilon_o W_A L_A}{C_{f1} z_o^2} \tag{2.8}$$

Lastly, the output voltage is sampled once every 4 clock cycles producing a sampling rate of 1MHz, a 100 times over sampling rate.

The front end capacitors consist of the variable capacitor being sensed (C_{sense}) and a fixed capacitor (C_{fixed}). The voltage signal is proportional to difference between the two as shown in (2.6). In order to be able to sense the entire range of the variable capacitance the C_{fixed} is set to be in the middle of this range, or 20fF.

Because the largest difference in capacitance seen at the input is 10fF, the first feedback capacitor is chosen to be 15fF. While this is small enough to not completely attenuate the incoming signal it should also be large enough to not be overly effected by the charge injection noise of the reset switch in parallel with it. In order to additionally help reduce the amount of charge injection noise introduced in the circuit all the switches are made from matched transistor pass gates. Lastly, the two sampling capacitors (C_{sh1}, C_{sh2}) as well as the capacitors surrounding the subtractor (C_{f2}, C_{f3}) are chosen to be small enough to not significantly slow down the circuit but also large enough to minimize the amount of kT/C noise they accumulate.

2.4 Amplifier Design

The topology chosen for the amplifier is a single ended folded cascode amplifier as shown in figure 2.6. It consists of a differential input pair followed by a folded cascode high gain stage. The advantages of this topology include large gain and bandwidth with low power consumption and device area. Keeping the design single-ended eliminates the need for a common-mode feedback circuit, which would add area and complexity to the design. The amplifier is designed for the TSMC 0.35µm process. The power supplies V_{dd} and V_{ss} are 1.5V and -1.5V respectively.

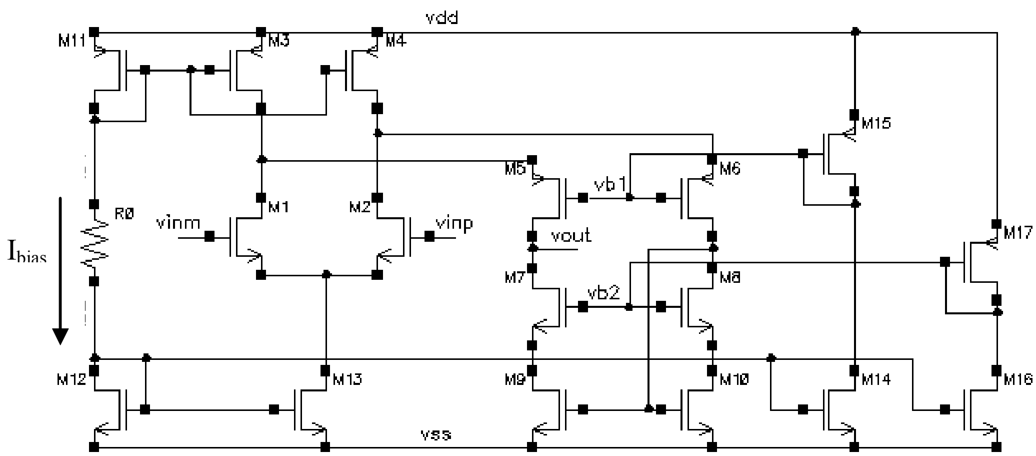


Figure 2.6 Transistor-level schematic of opamp.

Bias current I_{bias} is provided by transistors M11, M12 and the resistor R_0. Using KVL on this branch produces the equation,

$$V_{dd} + v_{gs11} - R_0 I_{bias} - v_{gs12} + V_{ss} = 0 \tag{2.9}$$

After plugging +/-1.5V in for V_{dd} and V_{ss} (2.9) can be solved for R_0,

$$R_0 = \frac{3\text{V} - v_{gs12} + v_{gs11}}{I_{bias}} \tag{2.10}$$

From this equation R_0 can be calculated for the desired bias current. Transistors M1 and M2 form the differential input pair. The current for this pair is mirrored from the bias current through M13. Cascode transistors M3 and M4 provide high output impedance along with the wide swing current mirror comprised by transistors M5 though M10. Transistor pairs M14, M15 and M16, M17 provide voltages for bias points vb1 and vb2. A simple bias circuit is used rather than a constant g_m circuit to reduce the amount of area consumed by the amplifier and to simplify the design.

The DC gain of this circuit can be found using small signal analysis to be

$$A_o = g_{m1} R_{out} \tag{2.11}$$

where the output impedance R_{out} is given by

$$R_{out} = \left(g_{m5} r_{ds5}\left(r_{ds1} \| r_{ds3}\right)\right) \| \left(g_{m7} r_{ds7} r_{ds9}\right) \tag{2.12}$$

As shown, the output impedance is on the order of $g_m r_{ds}^2$, a significant increase over the DC gain of a simple differential input pair which is on the order of $g_m r_{ds}$ only, improving the ability to drive subsequent stages.

The transfer function can be approximated as

$$A_v = g_{m1} Z_L(s) \tag{2.13}$$

Where $Z_L(s)$ consists of the output impedance of the amplifier in parallel with the output load capacitance, C_L, giving

$$A_v = \frac{g_{m1} R_{out}}{1 + s R_{out} C_L} \tag{2.14}$$

For mid-band and high frequencies the unity term in the denominator can be ignored and the gain becomes

$$A_v = \frac{g_{m1}}{s C_L} \tag{2.15}$$

which means the unity gain frequency of the amplifier is simply g_{m1}/C_L. For the initial sense amp, this load capacitance is 150fF, the capacitors the initial samples are stored on (C_{sh1}, C_{sh2}). For the subtractor, the load capacitance is the input of the control stage which consists of the gate of a transistor, estimated at 1.5pF. Since all of these capacitors are constrained by different aspects of the system the unity gain frequency of the amplifier is maximized by sizing the input pair for a large transconductance. The size of the input transistors still need to be limited to ensure each C_{gs} does not get so large it overwhelms the front-end capcitors.

Table 2.1 shows the sizing for all the transistors in the amplifier. The bias resistor is set at 350kΩ to provide the bias current of 5μA. The three volt power supply is split to +/- 1.5V.

Table 2.1 Transistor dimensions.

Transistor W/L	Transistor W/L	Transistor W/L
M1 8.4μm/.035μm	M7 1.0μm/0.7μm	M13 1.4μm/0.35μm
M2 8.4μm/0.35μm	M8 1.0μm/0.7μm	M14 3.5μm/0.7μm
M3 7.0μm/0.35μm	M9 1.0μm/0.7μm	M15 0.7μm/0.35μm
M4 7.0μm/0.35μm	M10 1.0μm/0.7μm	M16 7.0μm/0.7μm
M5 4.9μm/0.7μm	M11 3.5μm/0.35μm	M17 4.9μm/4.2μm
M6 4.9μm/0.7μm	M12 0.7μm/0.35μm	

2.4.1 Amplifier Characterization

All of the simulations in this section are produced with HSPICE. The power consumption for the amplifier and bias circuitry at DC is 167μW. The bias circuitry uses 81μW of that power, but can be shared amongst amplifiers and can be removed from consideration. The remaining power consumption is then 86μW. The output swing is +/- 1.37V giving a broad range of voltage for the sensed variable capacitance.

The open-loop response of the sense amplifier is shown below (figure 2.7). The open loop response has been loaded with the 150fF sampling capacitor.

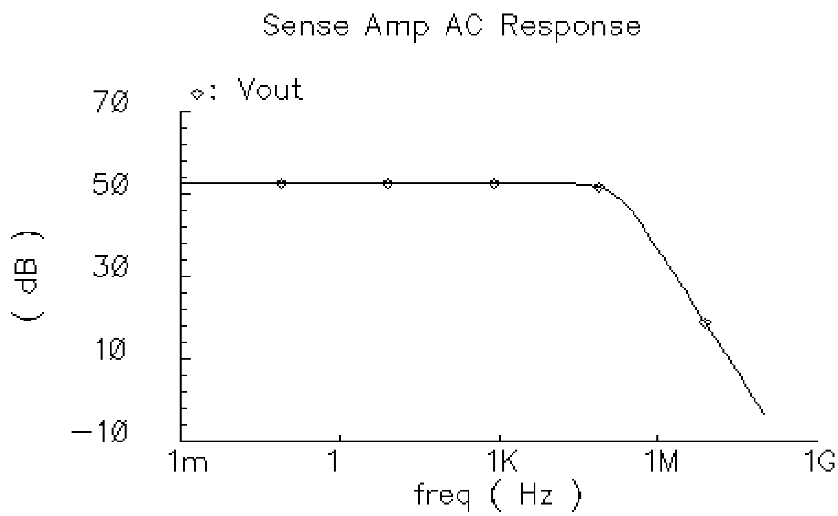


Figure 2.7 Sense amplifier open-loop gain response.

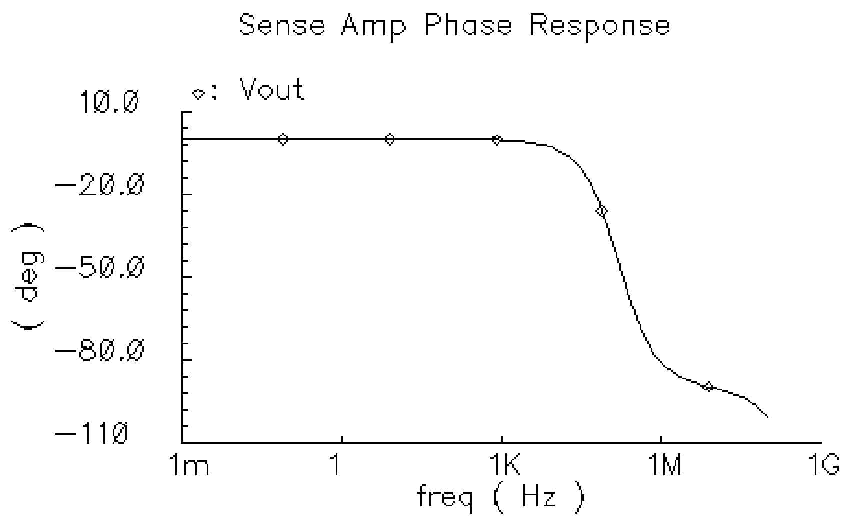


Figure 2.8 Sense amplifier open-loop phase response.

The amplifier has a DC gain of 52.6dB or 426.6V/V with a 3dB frequency of 162kHz. The unity gain frequency (UGF) is 69MHz. At this point the phase is –97.5˚ which provides a phase margin of 82.5˚. This implies that the amp is very stable at UGF.

The following graph (figure 2.9) shows the slewing response of the sense amplifier.

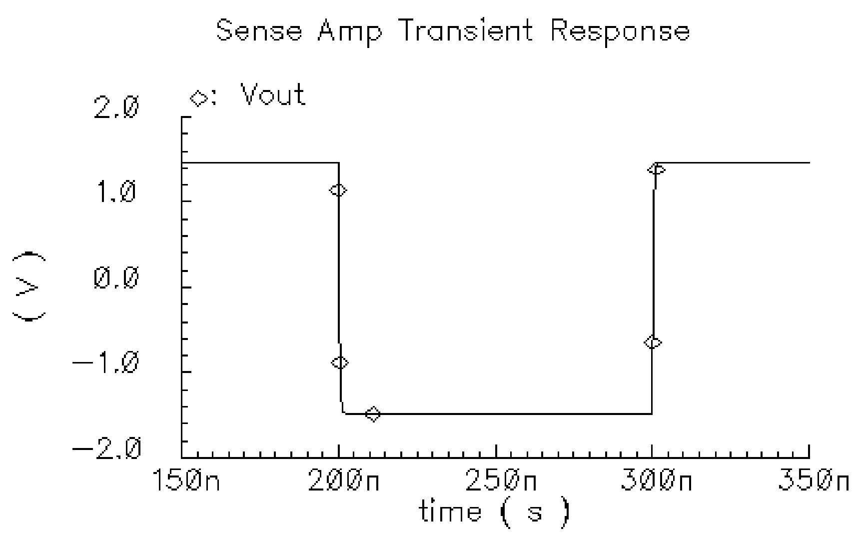


Figure 2.9 Sense amplifier output under slewing conditions.

The negative and positive slew rates of the sense amplifier are –/+2.5V/ns. It should be noted that the slew rate is helped by the fact that the load capacitance on the sense amplifier is only 150fF so the response is extremely fast.

The response of the amplifier in the subtractor configuration is not quite as fast and does not have as high a bandwidth as the initial amplifier due to the fact that the load capacitance is a factor of 10 larger. This implies that the 3dB and UGF frequencies are a factor of 10 smaller or 16.2kHz and 7MHz respectively. The phase margin increases slightly to 87˚. This is still enough bandwidth for the 1MHz modulation frequency and has stability at unity gain. Graphs for the subtractor amplifier are shown in figures 2.10-2.12.

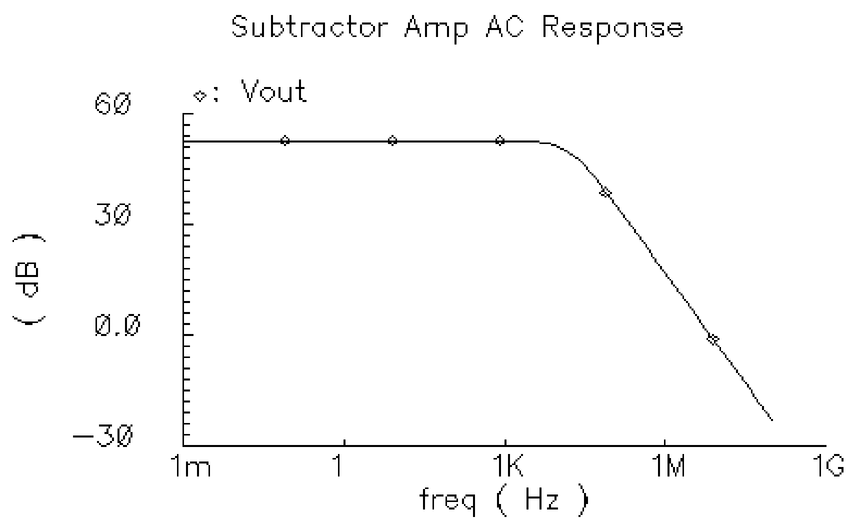


Figure 2.10 Subtractor amplifier open-loop gain response.

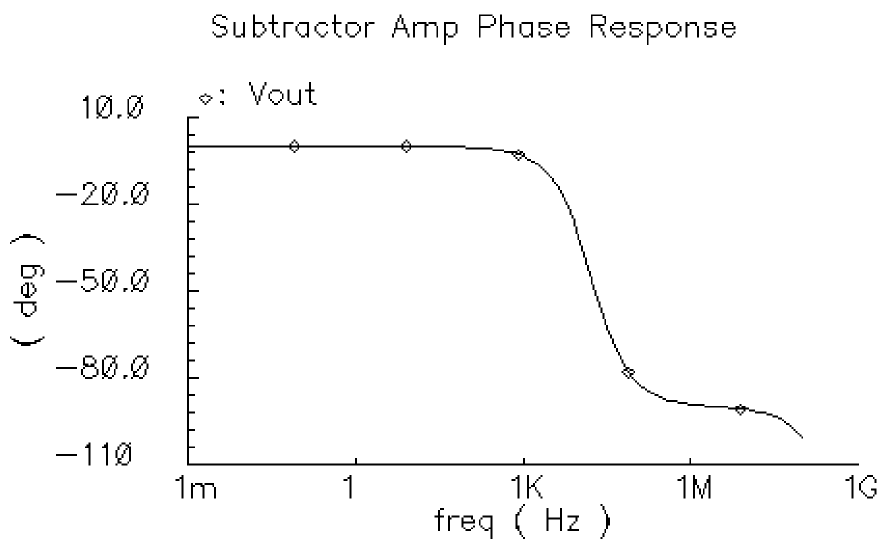


Figure 2.11 Subtractor amplifier open-loop phase response.

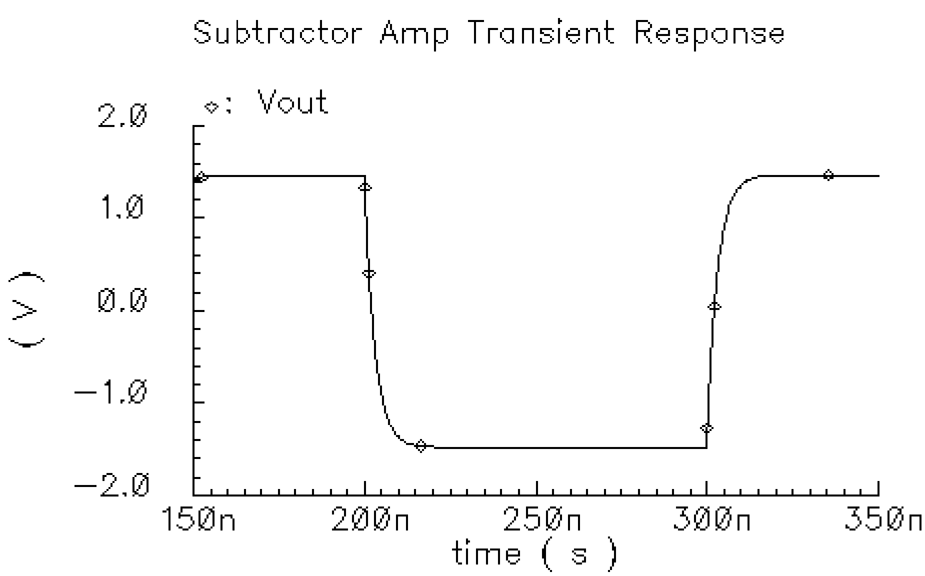


Figure 2.12 Subtractor amplifier under slewing conditions.

2.4.2 NOISE ANALYSIS

Although low frequency noise is attenuated by the CDS scheme mid and high frequency noise can also be a concern. There are three noise sources associated with the amplifiers as shown in the simplified schematic below (figure 2.13). For simplicity the voltage noise of the half circuit can be analyzed and added together in v_n. For the following analysis C_1 refers to $C_{sense}+C_{fixed}$ and C_2 refers to C_{f1} in the first stage of the sensor. The noise sources of the amplifier are the thermal noise due to the drain current and flicker noise of the input transistors.

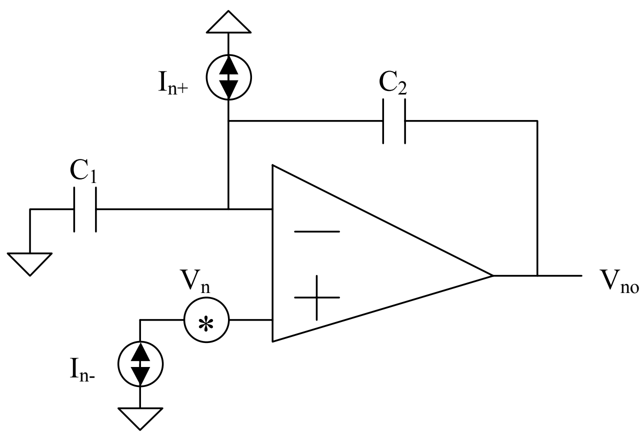


Figure 2.13 Simplified amplifier noise schematic.

The contribution of each noise source can be calculated separately and added together using the principle of superposition. When calculating noise contributions it is assumed that the amplifier in question is ideal. Current noise is considered first (figure 2.14).

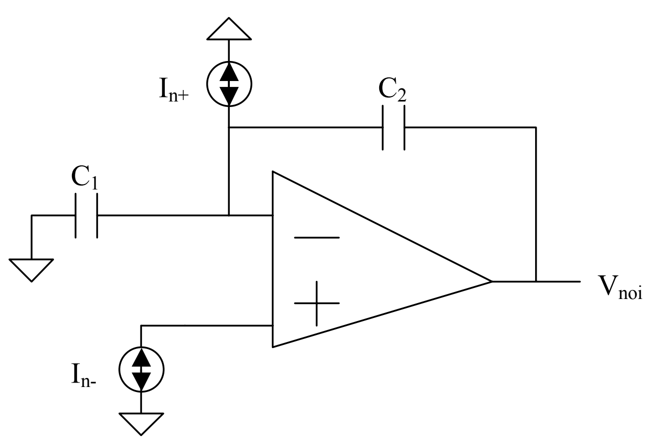


Figure 2.14 Current noise model.

In an ideal amplifier no current flows into the positive or negative terminals of the amplifier. This means i_{n-} has to be zero. If no current flows into the positive terminal that also means the positive and negative terminals are biased at zero. This makes the voltage across C_1 also zero, so all the current from i_{n+} flows through C_2. Using Ohm's law to find the output voltage produces

$$v_{noi} = \frac{i_{n+}}{sC_2} \tag{2.16}$$

i_{n+} can be converted into a voltage by dividing it by (sC_{gs}),

$$v_{noi} = v_n \frac{sC_{gs}}{sC_2} \tag{2.17}$$

where C_{gs} is the gate source capacitance of a transistor. Canceling like terms reduces the current noise contribution to

$$v_{noi} = v_n \frac{C_{gs}}{C_2} \tag{2.18}$$

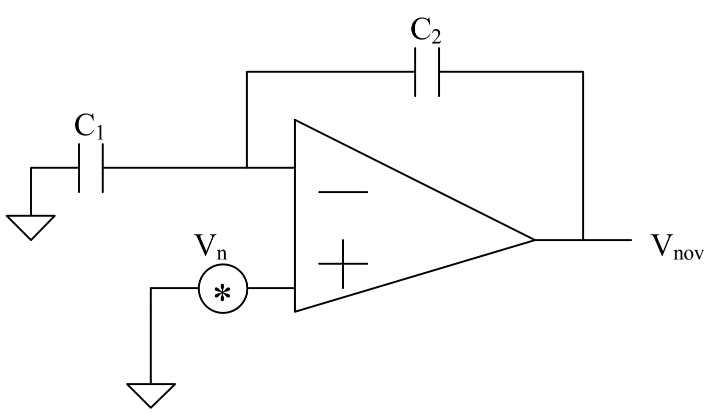


Figure 2.15 Voltage noise model.

Figure 2.15 shows the voltage noise contribution. Again assuming an ideal amplifier implies the voltage at the negative terminal is also v_n. No current flows into the positive terminal so

$$-v_n sC_1 = (v_n - v_{nov})sC_2 \tag{2.19}$$

This equation can be solved for v_{nov},

$$v_{nov} = v_n \frac{C_1 + C_2}{C_2} \tag{2.20}$$

Adding the voltage and current noise components together and squaring both size of the equation produces the total noise contribution at the output,

$$v_{no}^2 = v_n^2 \left(\frac{C_{gs} + C_1 + C_2}{C_2} \right)^2 \tag{2.21}$$

The major voltage noise devices in the amplifier are the transistor pairs M1-M2, M3-M4 and M9-M10 [Gray82]. Since these devices are all matched their noise contributions are equal and can be doubled to simplify calculations as mentioned above. The noise voltage of each can be calculated by applying a voltage source to each gate and determining the output voltage due to each. Using superposition the noise voltage for each transistor pair can be added together to produce the output voltage noise,

$$v_{nov}^2 = 2(g_{m1}R_{out})^2 v_{n1}^2 + 2(g_{m3}R_{out})^2 v_{n3}^2 + 2(g_{m9}R_{out})^2 v_{n9}^2 \tag{2.22}$$

In (2.22) v_{nx} refers to the noise voltage source applied to the gate of transistor x. In order to find the input-referred voltage noise v_{nov}^2 is divided by the voltage gain of the amplifier, (2.11)

$$v_n^2 = \frac{v_{nov}^2}{g_{m1}R_{out}} \tag{2.23}$$

which, by dividing and canceling like terms the resulting input-referred voltage noise becomes

$$v_n = 2v_{n1}^2 + 2\left(\frac{g_{m3}}{g_{m1}} \right)^2 v_{n3}^2 + 2\left(\frac{g_{m9}}{g_{m1}} \right)^2 v_{n9}^2 \tag{2.24}$$

The noise voltage of each transistor x is defined as

$$v_{nx} = 4k_B T \left(\frac{2}{3} \right) \left(\frac{1}{g_{mx}} \right) \tag{2.25}$$

where k_B is Boltzmann's constant (1.38x10-23J/K) and T is room temperature in Kelvin (300K). Flicker noise is ignored for this analysis given the modulation voltage is at a high frequency range

[Wu02]. Using the device parameters given in table 2.1 and results from simulation the total input-referred noise from the amplifier v_n is 42nV/√Hz.

It is possible to determine the input-referred noise displacement by dividing equation 2.21 by the sensitivity of the sensor, equation 2.8.

$$z = v_n \frac{(C_{gs} + C_{sense} + C_{fixed} + C_{f1})z_o^2}{2V_m \varepsilon_o W_A L_A} \tag{2.26}$$

Therefore it is important to keep capacitors as small as possible and use the largest possible v_m that will not saturate the amplifier. Figure 2.16 shows the noise displacement versus initial gap, z_o given the device sizes previously discussed. As the gap decreases there is an increase in sensor gain which decreases the amount of input-referred noise.

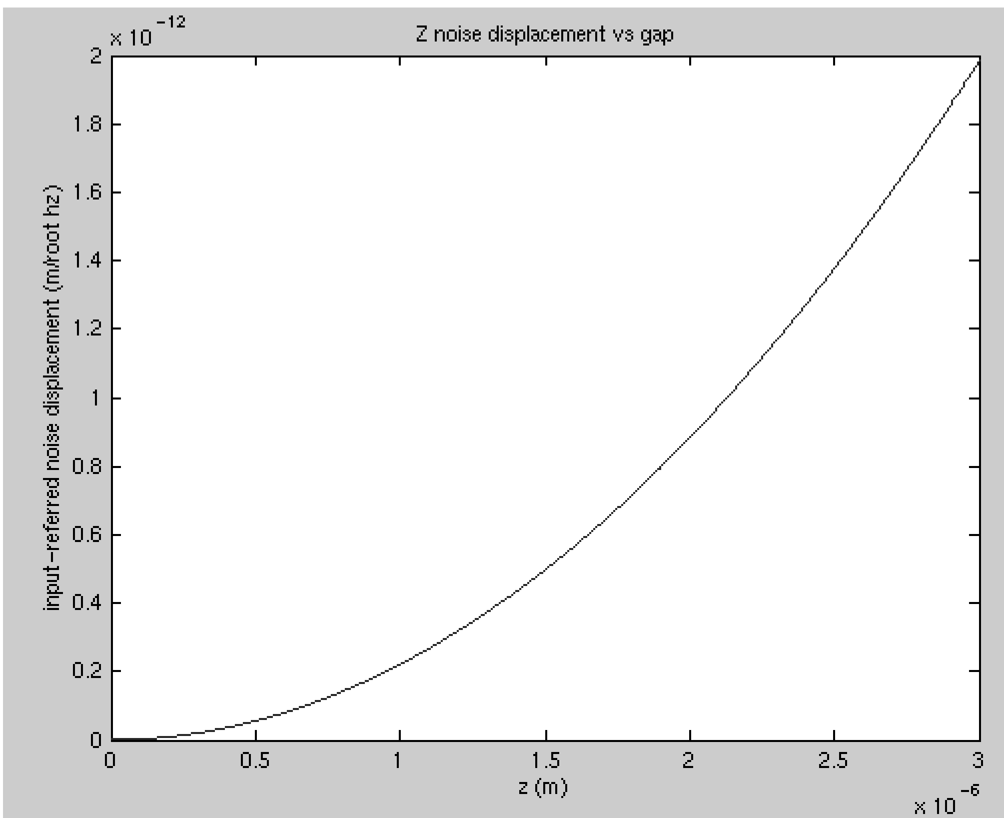


Figure 2.16 Minimum input-referred noise displacement versus initial gap.

Chapter 3

Chip Design

3.1 Chip Design and Layout

A chip was designed in the TSMC 0.35µm process and submitted for fabrication. The test chip consisted of clock generators, a simple discrete variable capacitance system to test circuit functionality and an array of sixteen actuators with logic and controlling circuitry. A simple block diagram is shown in figure 3.1 and the schematic and layout of each cell is shown below.

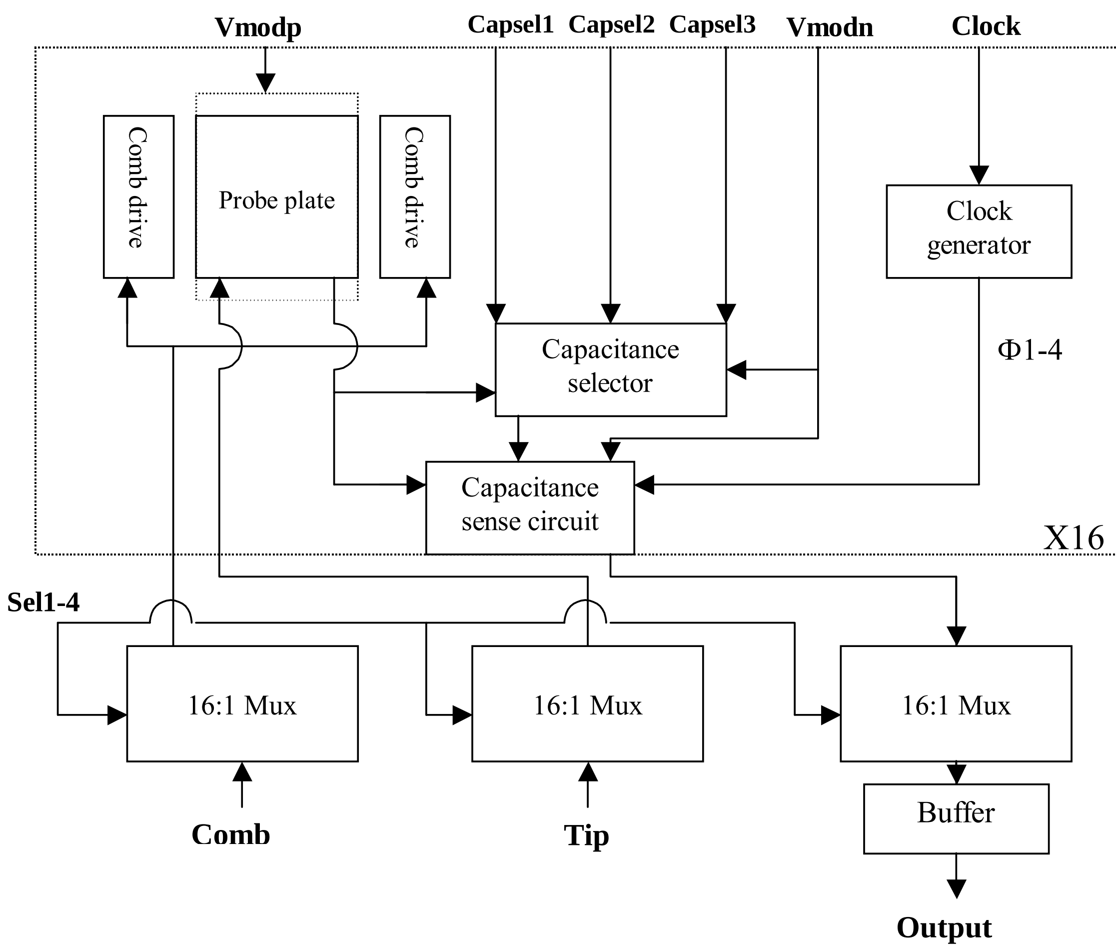


Figure 3.1 Block diagram of actuator array circuitry.

A rough layout of the amplifier was produced using Neocell [Neolinear]. This layout was then rearranged to reduce empty space and form a more compact cell. The input, active load and folded cascode transistors pairs were matched to reduce offset. The switches and capacitors for the sample and hold, and feedback and biasing for second amp were laid out to be as symmetric as possible to limit the amount of offset that might occur from mismatched devices in the subtractor. The layout of the capacitance sense circuit is shown in figure 3.2.

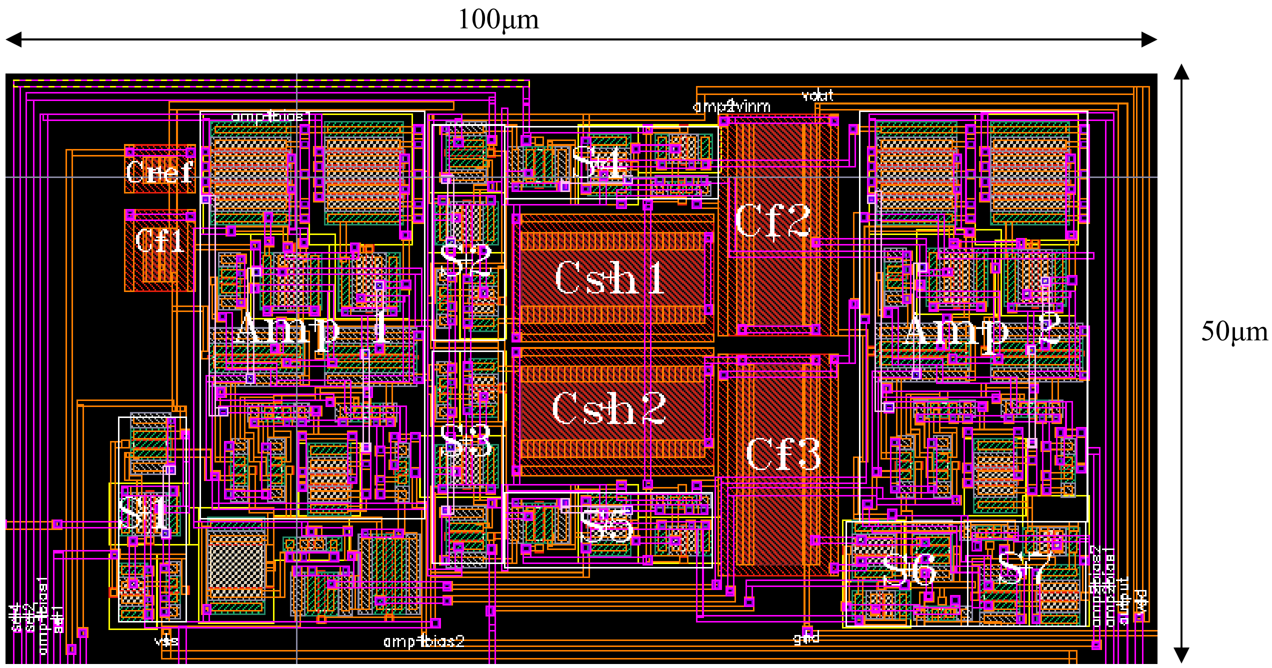


Figure 3.2 Layout of sensor.

Each capacitance sense circuit also has its own input capacitance selector shown in figure (3.3a schematic, 3.3b layout). It consists of seven 5fF capacitors which can be switched into a parallel configuration with the fixed reference capacitor of the sensor. Three inputs to a few logic gates provide the switches with signals that allow just one through all seven to be activated. This can be used to tune the reference capacitor to the value closest to the desired initial capacitance since it is difficult to determine what the actual capacitance will be in the data storage system from simulations. This layout was produced with Neocell.

Additionally, this functionality is used for the simple testing circuit. In the simple circuit two fixed capacitors are used at inputs. One of these capacitors is connected to the capacitor selector in order to provide eight discrete capacitance values. By varying this capacitor it is possible to produce 8 different DC voltages at the output.

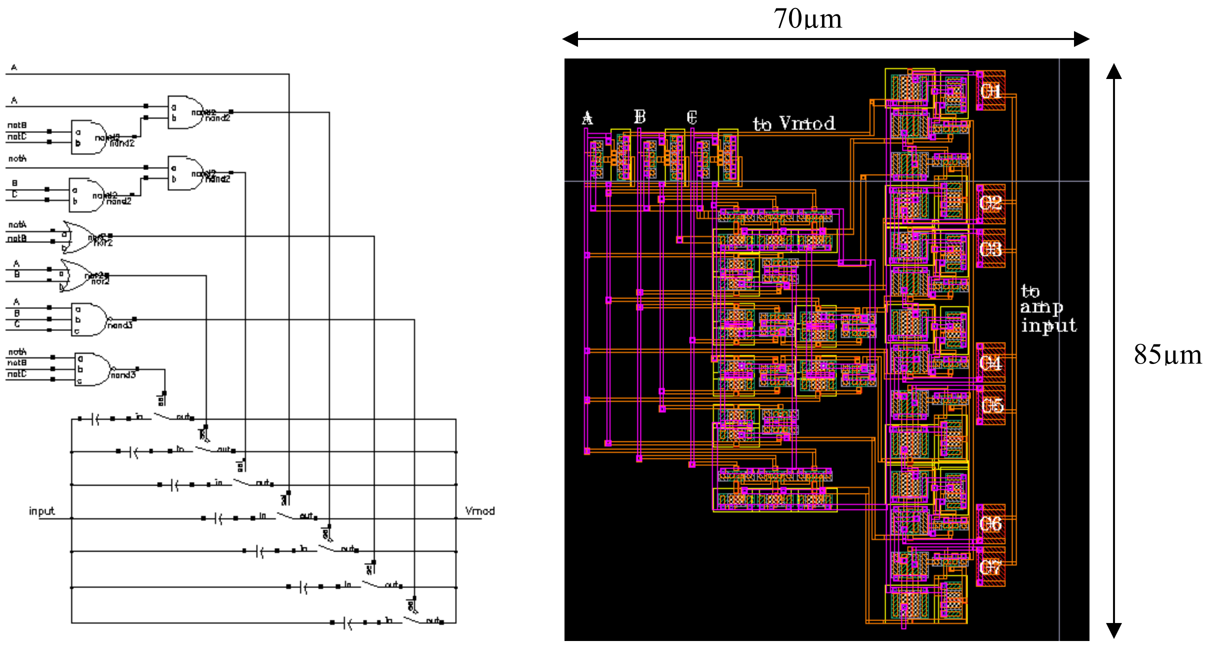
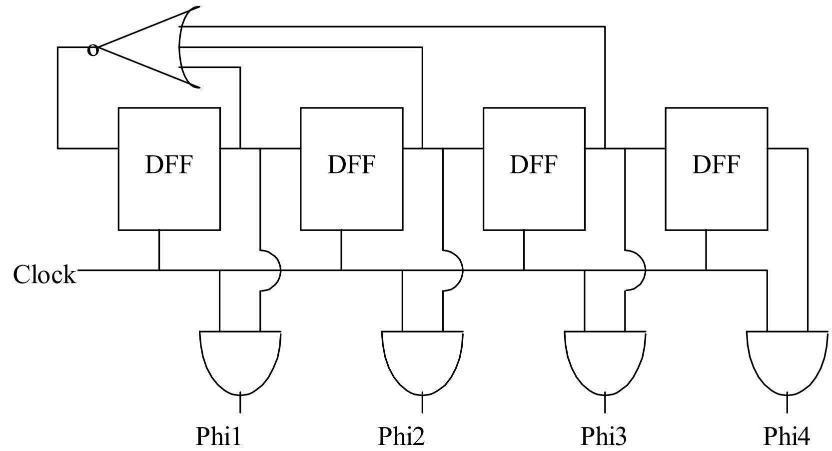
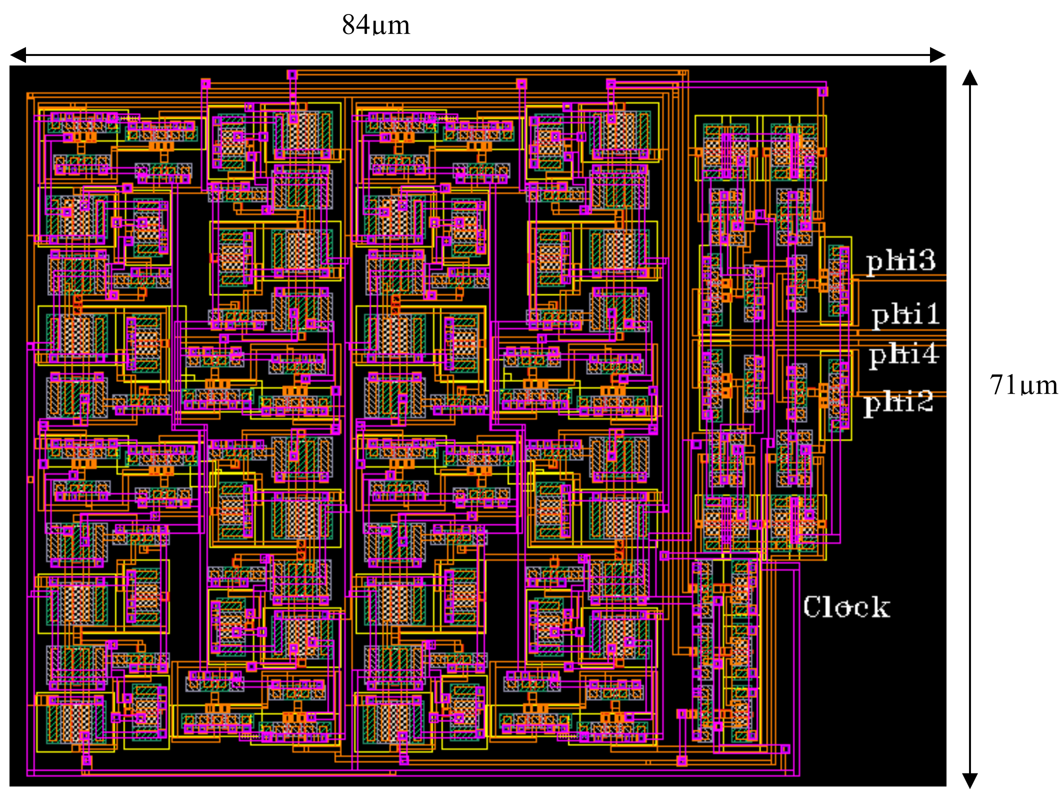


Figure 3.3 Capacitor selection circuit (a) schematic, (b) layout.

Clock generators are able to provide four non-overlapping clock pulses. A pulse is used to clock four D flip flops (dff). The positive outputs of the first three dffs are fed through a nor gate to the input of the first dff. This ensures the input for the dff remains low until the pulse has reached the final dff effectively creating a single pulse ring buffer. The output of each dff is passed through a nand gate along with the clock signal to shape each pulse to the correct duty cycle. Each of these outputs are passed through one final inverter to provide the four separate clock pulses which drive the sensors (3.4 (a) schematic, 3.4 (b) layout). The layout was also produced with Neocell.



(a)



(b)

Figure 3.4 Clock generator (a) schematic, (b) layout.

In order to test the functionality of an array of actuators, 16 independent actuators have been placed on the chip (figure 3.5). Each actuator has its own controlling and sensing circuitry. The outputs and controls are fed through 16:1 muxes so a single probe can be used at a time. The probes on the test chip were designed by Dave Guillou for the 3 metal layer Agilent 0.5µm process [Guillou95]. The actuators have been changed slightly to comply with design specifications for the 4 metal layer TSMC 0.35µm process.

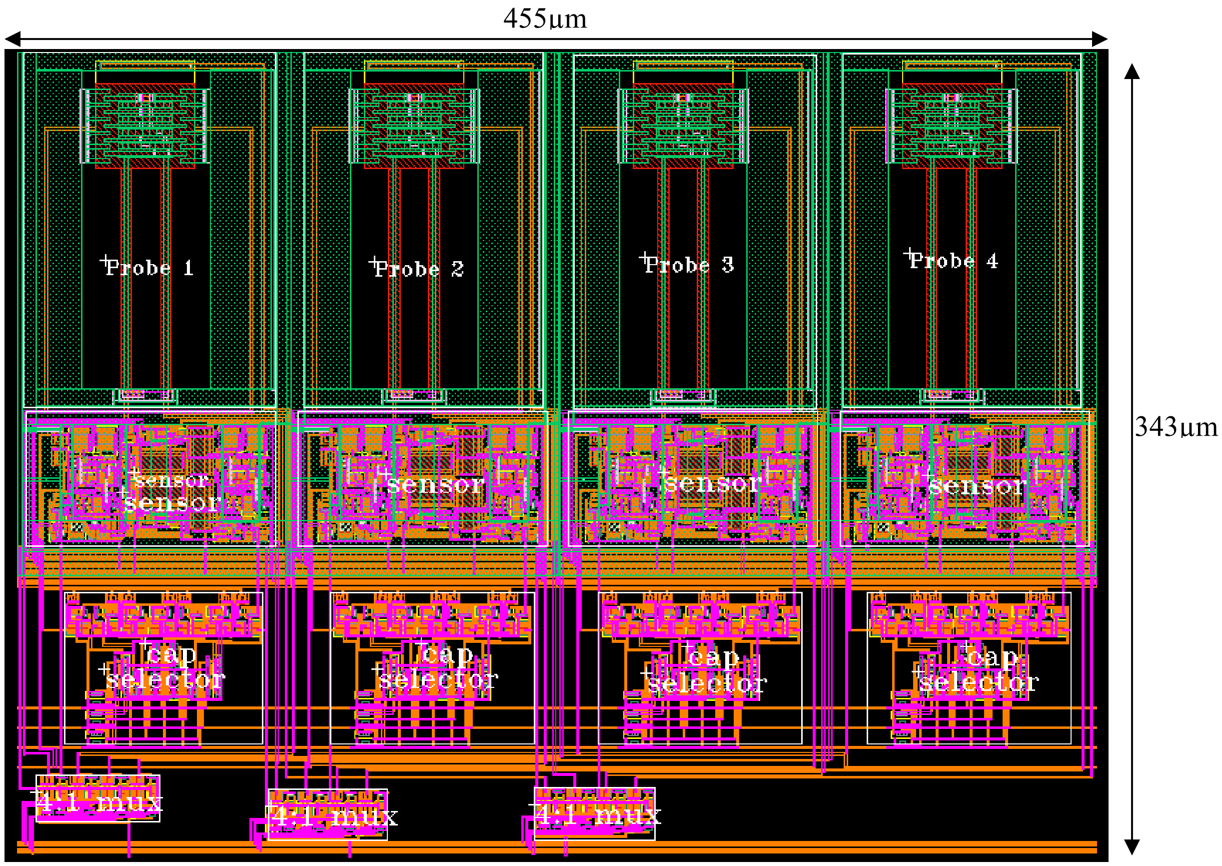
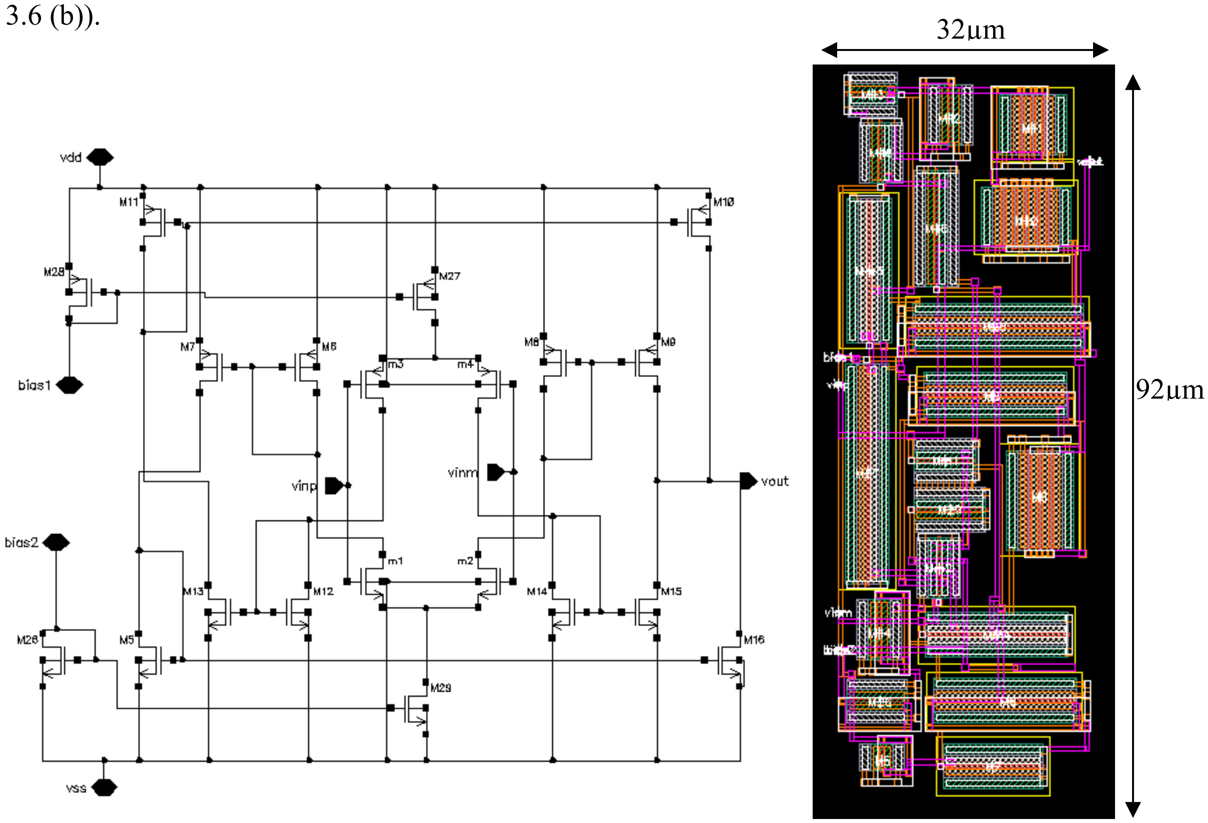


Figure 3.5 An array of 4 probes with sensing circuitry.

The output of the amplifier was designed to carry a load of 1.5pF, the estimated input capacitance of the feedback circuitry. For the testing of this chip all feedback controls were off chip, so the output needed to drive the much larger capacitance of the bond pad. In order to accomplish this the output of the muxes needed to be sent to a large swing high drive buffer amplifier. The design for the buffer shown in figure 3.6 (a) is a variation on a design that uses 2 pairs of complementary differential pairs as the input stage [Fisher87, Yazdi92]. When the input signal moves out of the dynamic range of one differential pair the other pair takes over amplification. Since this buffer is only needed for the off chip controls which will be on chip in the final data storage system, the power consumption and area are not considered in the calculations for meeting the specified constraints. The layout was generated using Neocell (figure 3.6 (b)).



(a) (b)

Figure 3.6 Buffer (a) schematic. (b) layout.

Although the sensor takes up all of the 50µm by 100µm area it is possible to decrease this amount by sharing certain parts of the circuitry. The initial sensing amplifier needs to remain as close to the probe as possible to limit the amount of noise and parasitic capacitance on the sensing node. If not all probes are being used at the same time it is possible for several probes to share their subtractor circuits. Since the sample and hold capacitors are already separated from the subtractor by a switch, it is straightforward to use these switches as though part of a mux. It is also possible to stagger the clock phases for several sense amplifiers so that while one is sampling the others are resetting or holding their values. They can then be running at the same time and still share a subtractor. For this to work a reset phase would have to be inserted after each subtraction. The frequencies of the modulation and clock signals would also have to be altered and care taken to ensure the bandwidths of the amplifiers are still adequate.

The following figure (3.7) shows the entire chip with various blocks and pins labeled. The final chart (3.1) lists the connections necessary for the chip to function.

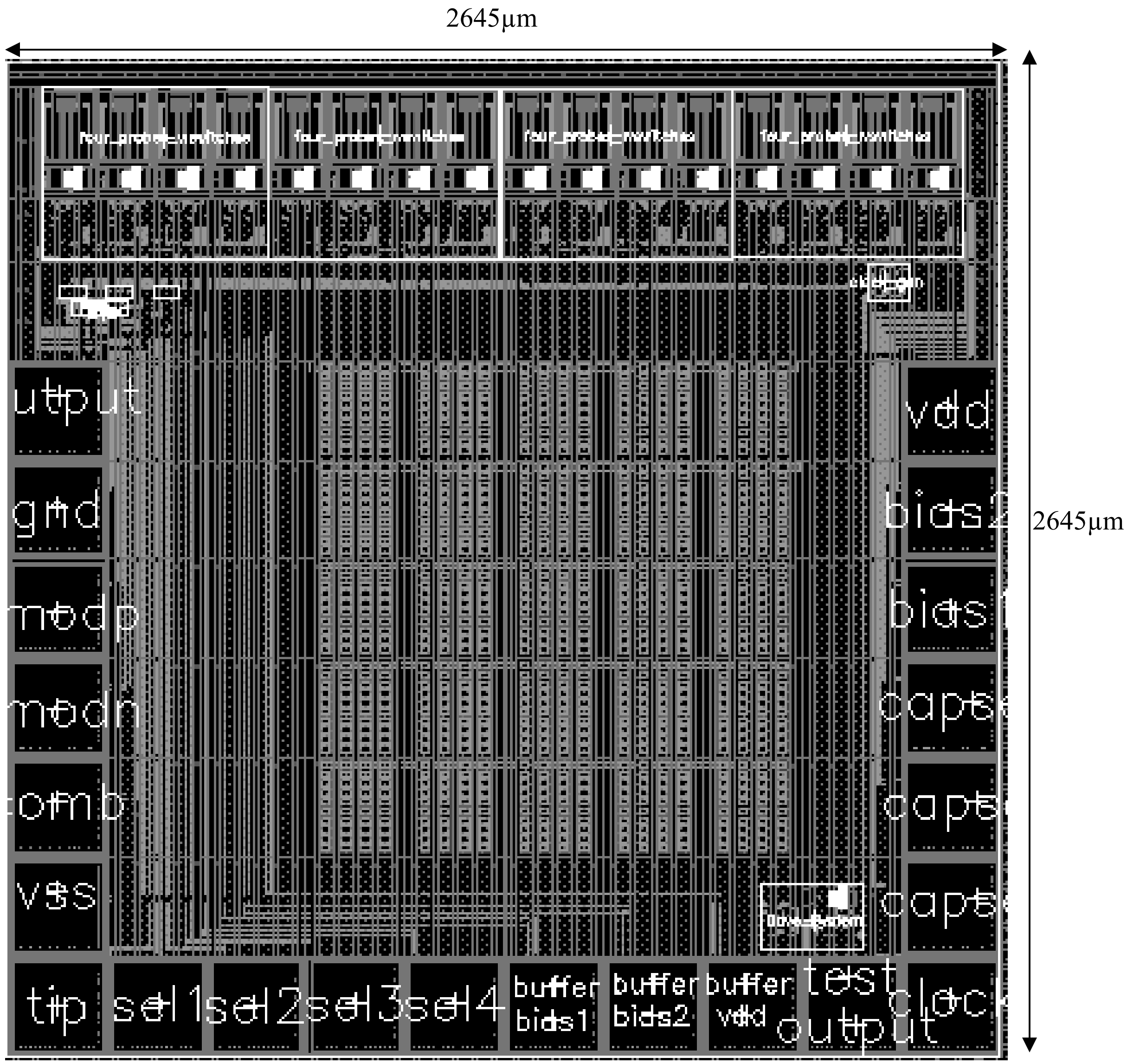


Figure 3.7 Layout of chip actuators86.

Table 3.1 Electrical connections for chip pins.

Pin	Connection
Output	Output of probe array
Gnd, Vdd, Vss	0, 1.5, -1.5 V
Vmodp, Vmodn	Alternating modulation signals @1MHz, +/-1V
Comb	Comb drive signal, ~10kHz sine wave, 10Vp-p
Tip	Connects to read/write head, only needed if a head is applied for testing purposes
sel1-4	Mux select lines for probe array +/-1.5V
Bufferbias1-bufferbias2	R=500kΩ
Buffervdd	1.5V
Test_output	Output of simple test circuit
Clock	Setup with Vmodn/Vmodp as shown in figure 2.4
Capsel1-3	Select lines for discrete capacitor selection +/-1.5V
Bias1-bias2	R=20kΩ

3.2 Experimental Results

The chip was submitted for fabrication in the TSMC 0.35μm process in late January, 2004 under the name actuators86 [CMU_MOSIS]. Upon return it was set up for testing of the simple test circuit. Voltage supplies were used to connect Vdd, Vss and Gnd to the proper pins. A bias resistor was placed across the bias pins and a LeCroy signal generator was used to provide Vmodn, Vmodp and the clock input. Cycling through the capacitance selection lines provided the following measured voltages at the output (figure 3.7).

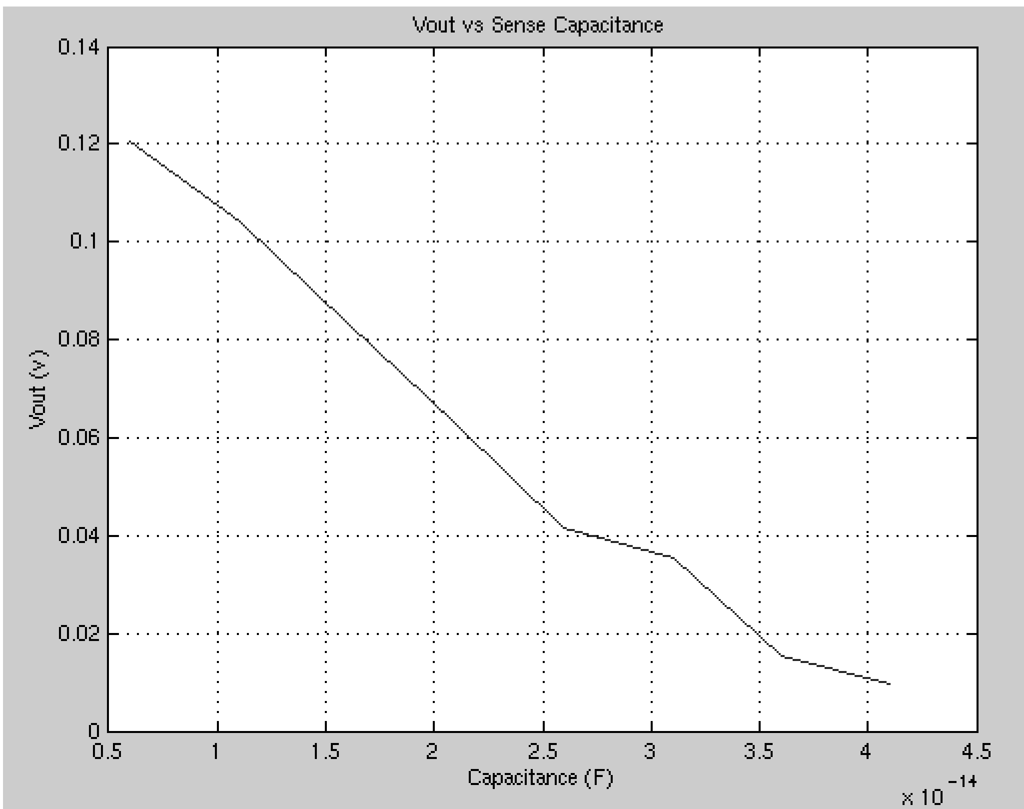


Figure 3.7 Output voltage for 8 steps of capacitance.

The increase in capacitance is estimated from parasitic extraction of each discrete capacitor in addition to the parasitic capacitances surrounding them. From this graph it is apparent that there is a steady decrease in voltage for each increase in capacitance. This graph also suggests that the fixed capacitor is closer to 45fF than the 20fF it was designed to be. This extra capacitance most likely is due to parasitic interconnect capacitors, illustrating the difficulty in estimating actual capacitance values from extracted simulations. In this case, all 7 discrete capacitors would need to be switched into the signal path to most closely match the variable capacitor and utilize the most range from the sensor.

Chapter 4

Conclusions

4.1 Summary

This thesis has presented the design of a variable capacitance sense amplifier intended for use in a MEMS probe-based data storage system. The basics of the probe storage design were presented along with the constraints the system lays upon the sensor. Methods of noise reduction were discussed and a sensor design utilizing one of these methods, correlated double sampling was explained. An amplifier design which meets the requirements of the sensor was presented and analyzed. Noise analysis was performed on the sensor. The design and layout of the blocks necessary to complete a test chip were shown and lastly experimental results were presented.

4.2 Directions for Future Work

Unfortunately at the time of this writing it has not been possible to test any released probes. Suresh Santhanam was able to release other probe designs using the CMOS-MEMS process developed at Carnegie Mellon. These probes have an nwell electrode connected to Vmodp beneath their moving plate. It is possible to use the comb drives to move the probe in and out of the z-plane and use the nwell electrode as the fixed plate of the variable capacitor for testing purposes, instead of a fixed plate media.

For testing with a fixed plate of media, the chip was laid out so that the plate could be brought in over the probes without interfering with any bond pad wiring. Mike Lu was able to produce closed-loop control of probes in experimental setups [Lu02].

Future versions of the chip should explore the feasibility of sharing subtractors amongst several probes and look for other options for reducing noise, area and power consumption.

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