Low Power Wide Tuning Range LC-VCO using RF MEMS passives

by

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A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical and Computer Engineering

August, 2004

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Abstract

The thesis describes the motivation, design, layout and test of a voltage controlled oscillator (VCO), targeted for use in a dual frequency-hopped receiver configuration to be used for portable applications. The key requirements of this architecture are integration, low power and wide tuning range. Micromachined passives enable low power operation through increased quality factors (Q) and wide tuning range through discrete reconfiguration. Integration is achieved by using foundry provided metal interconnect layers for building these passives. This is the first time both micromachined inductors and capacitors have been integrated on-chip using standard CMOS processing.

Micromachining leads to reduced substrate coupling capacitance causing an increase in inductor self-resonance, resulting in an increased Q at higher frequencies. This allows usage of bigger inductors and smaller capacitors, leading to low power operation. The degradation in phase noise due to usage of small capacitors is offset by the high Q achieved for the tank. The decreased power (2.75 mW from a 2.5 V supply), combined with higher operating frequency (2.8 GHz) and acceptable phase noise (-122 dBc/Hz at 1 MHz offset) results in an attractive figure of merit of 187. This is the best performance achieved till date for a VCO using MEMS passives as well as for integrated VCOs operating above 2 GHz, with the exception of VCOs using bondwire inductors and SOI technology.

Additionally, the VCO also achieves a wide tuning range through micromachined reconfigurable capacitors. The capacitors can be discretely tuned relaxing the requirements of the continuously tunable lossy non-linear varactor. The advantage of using the low parasitic linear MEMS capacitor in parallel with the tank is that it allows an extension of the tuning range without any degradation of phase noise or the requirement of any additional mixed-signal control. A tuning range of 700 MHz is obtained from 2.1 GHz to 2.8 GHz with the same phase noise (-122 dBc/Hz) at both these frequencies.

Acknowledgement

I would like to thank Dr. Tamal Mukherjee for his availability for discussions throughout the course of this work, which includes not only the time-frame when the designs and measurements were done but also during the writing of the thesis. His utmost pain in reading the thesis and prompt feedback led to a significant improvement in the thesis in a very short time. I also acknowledge Dr. Mukherjee and Prof. Gary K. Fedder for providing access to micromachining and fabrication facilities. Without the availability of top-notch foundry processes and excellent post-foundry in-house processing facilities, none of this work would have taken its present shape. I would like to thank Prof. Larry Pileggi for taking out time from his busy schedule to read my thesis. Prof. Rick Carley deserves a special mention for his insightful comments and observations during the course of this work.

I would like to thank all my CSSI and MEMS lab colleagues for their support. Altug Oz deserves a special thanks for doing post-foundry processing on my chips before I could make measurements. I acknowledge his prompt efforts in coming up with SEMs, as well as answers to questions related to his designs. I would also like to acknowledge Deepa Ramachandran for her support during the course of this work.

I am grateful to Mary Moore and Drew Danielson for all their efforts in ensuring smoothness in administrative related issues. In this context, I would also like to thank Elaine Lawrence and Lynn Philibin.

Finally, I would like to thank my parents, sisters and Shruti for their moral support throughout the course of this work.

This work was funded by the MARCO/DARPA Focus Center Research Program's Center for Circuits & Systems Solutions (C2S2) and the Industrial Taiwan Reseach Institute Lab at CMU.

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1 Introduction

1.1 Oscillator Needs and Requirements

Most radio frequency (RF) systems contain an oscillator which generates the periodic output signal used to modulate the transmitted or received signal. In order to span across the channels in a band, the oscillator would need to be tunable. The frequency is often tunable by voltage and hence the name voltage controlled oscillator (VCO). Thus, VCOs are found in systems which require a source of variable frequency used for frequency synthesis, clock and data recovery and other applications.

Oscillators must have some sort of self-sustaining mechanism to ensure that they continue to generate these periodic signals for an indefinite period of time. The basic operation of all oscillators involves positive feedback of the output to the input, thus allowing the signal to regenerate and sustain itself from one cycle to the next. The feedback system oscillates if the loop gain is equal to unity and total phase shift around the loop is equal to zero. This is known as the Barkhausen's criteria for oscillations.

While quartz crystals are popularly used to generate clean oscillations, their frequency limitations restrict their use at GHz radio frequencies. Similarly, noise due to higher active device count restrict the use of ring oscillators at RF. Thus oscillators employing a combination of lumped element energy storage elements like inductors (L) and capacitors (C) are commonly used in RF systems.

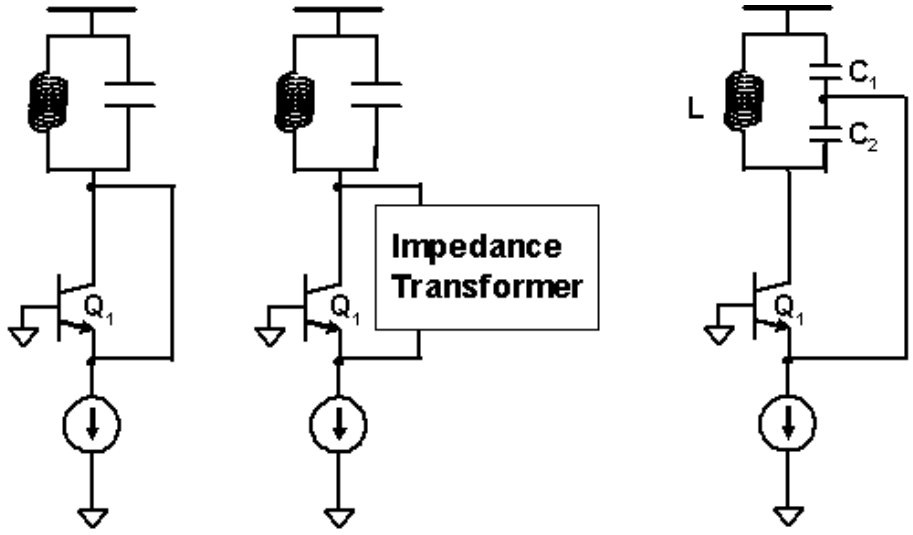
1.2 Common LC Oscillator Topologies

Connecting an inductor, L, to a charged capacitor, C, either in parallel or in series, results in energy sloshing between them This gives rise to oscillations at a frequency of $\frac{1}{2\pi\sqrt{LC}}$. The discussion following is based on a parallel LC tank. Practical Ls and Cs have losses associated with them. The tank losses can be represented as an equivalent parallel resistance, R_p. Some amount of the energy, being sloshed between L

and C gets dissipated across R_p. In the absence of any replenishing mechanism, all this energy would finally dissipate to zero. Hence an active device is needed to replenish lost energy.

Active device count is important as it relates to noise. Hence oscillators with just one active device are often used. This active device must be used in the feedback loop to ensure positive regenerative feedback at the frequency of interest. At resonance, the inductive and capacitive parts of the tank cancel each other. Hence the phase across a resonant tank is zero. For the total loop phase to be zero, it is imperative to provide zero phase across the feedback network too. Since the collector and emitter of a BJT are in phase, the signal can be fed back from the collector to the emitter of the transistor Q_1, as shown in Figure 1-1(a). Connecting it directly however would the load the tank by the impedance seen at the emitter ($1/g_{m1}$), dropping the loop gain to below unity, preventing oscillation. To isolate the tank, some form of an impedance transformation must be used to boost the emitter impedance to a much higher value before it appears parallel to the tank, as shown in Figure 1-1 (b). Figure 1-1 (c) shows one such method using passive impedance transformation. Here, the equivalent resistance appearing parallel to the tank is $(1+C_1/C_2)^2/g_{m1}$. This configuration is the well-known Colpitt's oscillator.

While the single-ended Colpitts'oscillator is a good candidate for a LC-tank VCO, adding one more active device to make the circuit differential is often preferred. Firstly, like any differential circuit, it has



(a) (b) (c)

Figure 1-1. Colpitt's Oscillator

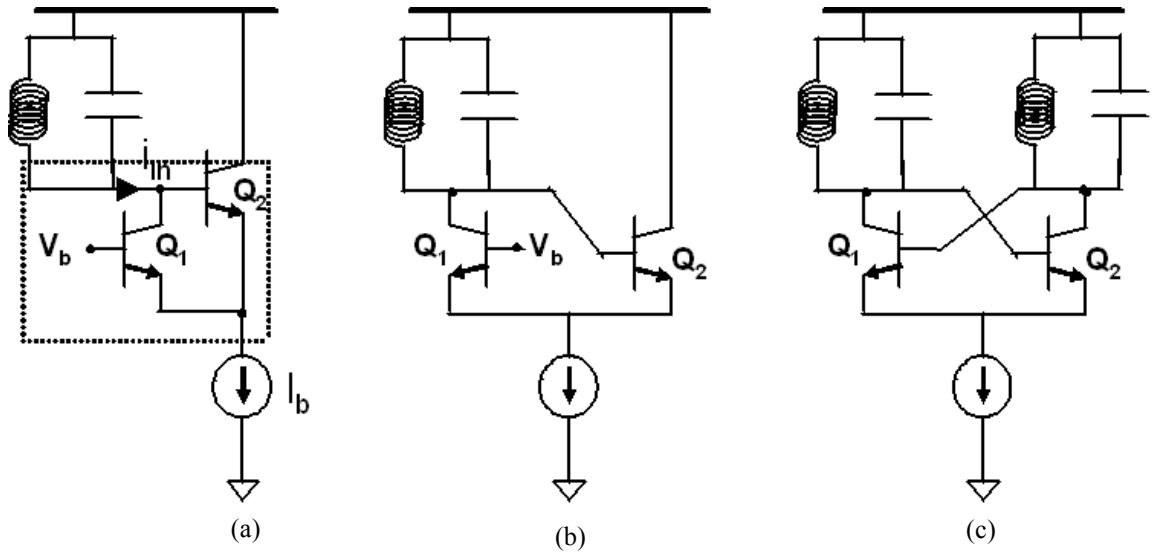


Figure 1-2. Cross-coupled Oscillator

better power supply noise immunity. Secondly, differential LO signals from the VCO are required to drive the single-balanced or double-balanced mixer in a typical transceiver architecture. Figure 1-2 (a) shows how the extra active device (Q_2) can be added. Q_2 feeds the signal from the collector of Q_1 back to the emitter of Q_1.

From the point of view of loss cancellation, this arrangement should be able to provide a 'negative resistance' to cancel the tank loss (R_p). In order to see how negative resistance is provided, if we apply increasing voltage at the base of Q_2 (Figure 1-2 (a)), the emitter follows that due to the presence of the constant current source, I_b. This decreases the V_{BE} across Q_1, decreasing its current, and hence decreasing the current, i_{in}, flowing in the active circuit network (denoted by dotted lines). This is equivalent to a 'negative resistance' since the current flowing in the network decreases even though voltage increases. This negative resistance, which is equal to $1/g_m$, must be less than or equal to R_p, to ensure sustained oscillations.

Figure 1-2 (b) is a redrawing of (a). If the collector current of Q_2 flows through another tank and the resulting voltage is applied to the base of Q_1, then we get to the topology of Figure 1-2 (c). This is the standard cross-coupled configuration in which differential outputs are obtained at the collectors of Q_1 and Q_2. The outputs are differential because when the voltage at the base of Q_1 rises, its collector falls, due to

the existence of the anti-phase relationship between the base and collector of a BJT. Since the collector and base of Q_1 and Q_2 are inter-connected to each other, and since we started off with the base of Q_1 rising, it means that the collector of Q_2 was also rising. Hence the two collectors are anti-phase with each other. Q_1 and Q_2 can be implemented as MOS transistors also.

1.3 Motivation

The VCOs discussed in this thesis [1] [2] are targeted for use in a dual frequency-hopped receiver configuration to be used for portable applications (Figure 1-3). The 100 MEMS mixer-filter array is used to hop between 100 kHz 'fine' bands. The VCO used in the wide-range synthesizer is used to define the 'coarse' hop of 10 MHz all the way from 100 MHz to 10 GHz.

There are 3 key requirements for the VCO to be used in this architecture:

(a) Wide tuning range: A wide tuning range micromachined reconfigurable capacitor [3] that mechanically switches between different capacitance configurations allows extension of tuning range.

(b) Low power: Micromachining [4] passives (inductor, L [5] and capacitor, C) enables low power operation through increased quality factors (Q). Low power consumption is highly desired in portable applications as it leads to longer battery life before recharge.

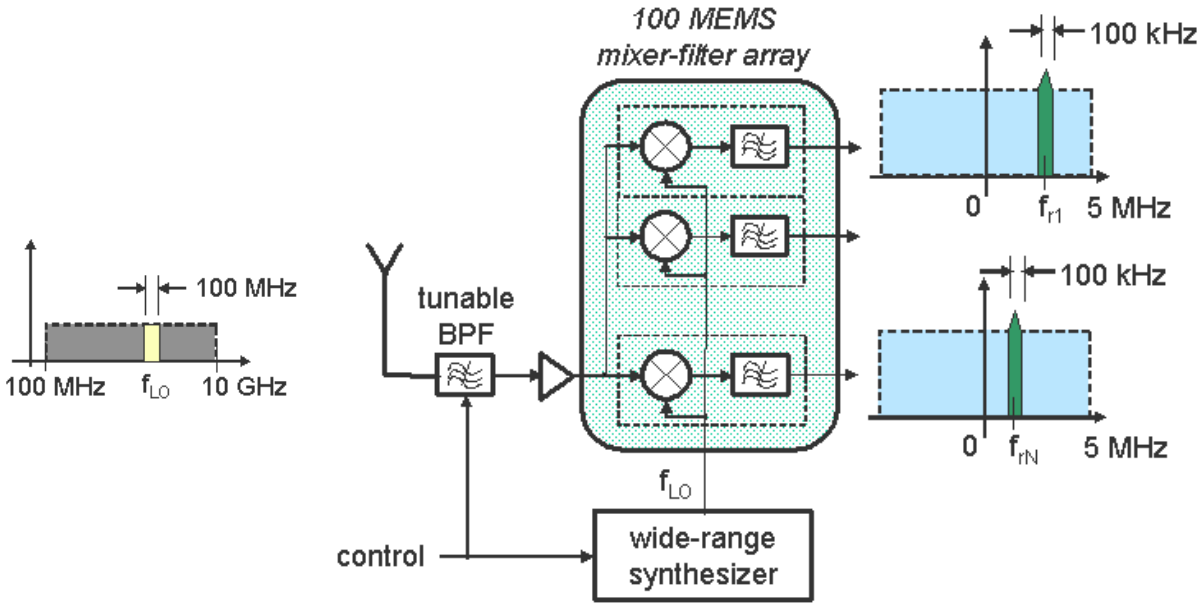


Figure 1-3. Dual frequency hopped receiver configuration

(c) Integration: Although MEMS inductors were integrated with electronics about 10 years ago [6], recent RF MEMS inductors [7] and capacitors [8] have used customized processing, preventing integration. The VCOs discussed in this work use a foundry fabricated interconnect stack for the RF passives, enabling monolithic integration with electronics, and eliminating losses arising from bonding custom fabricated RF MEMS passive chips to electronics ICs.

1.4 Micromachining background

The 3 key requirements will be met using a post-foundry micromachining process [4]. This process is used to sacrificially etch the dielectric stack and silicon, as shown in Figure 1-4. Interconnect layer patterns fabricated by the foundry define the regions where the back end of line (BEOL) dielectric will be removed for access to the silicon surface. This exposed silicon surface allows the sacrificial removal of the of the silicon around narrow metal dielectric patterns. The resulting micromachined geometry affects RF performance in the following ways:

A. C_1, the capacitance between X_1 and X_2 reduces due to the dielectric removal.

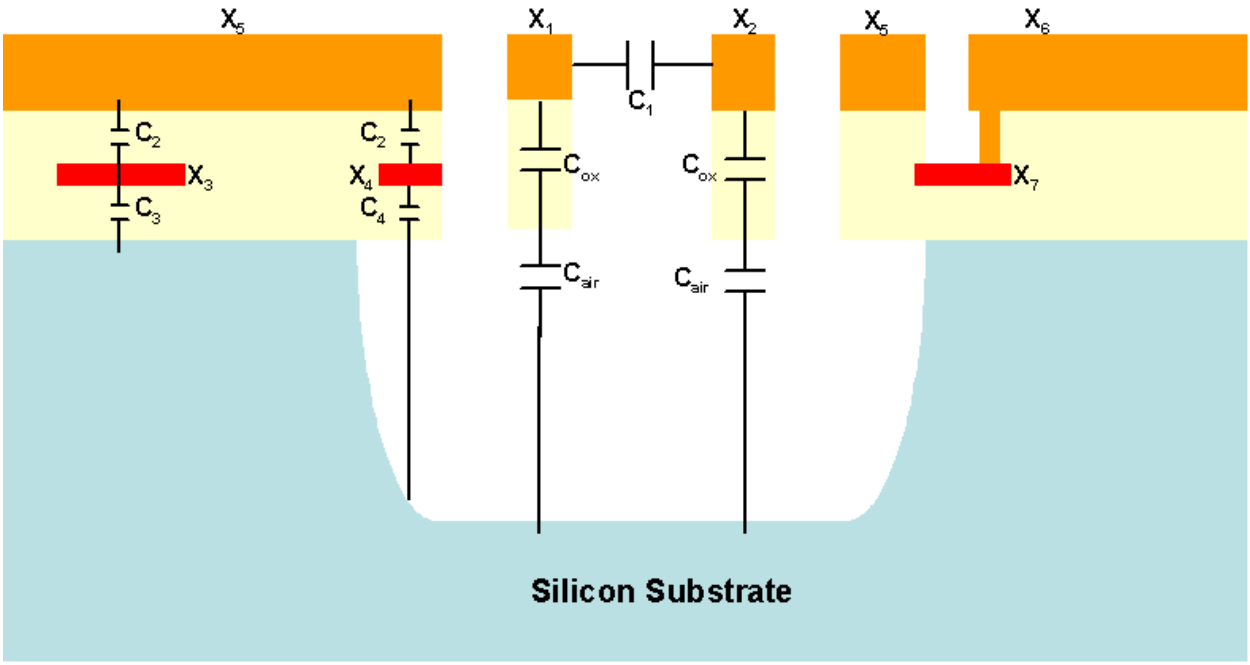


Figure 1-4. Manifestations of micromachining

B. C_{air} is now introduced in series with C_{ox}. As C_{air} is much less than C_{ox}, the effective value of capacitance from X_1 or X_2 to the substrate is reduced.

C. C_3 and C_4 denote the capacitances from X_3 and X_4 respectively to the substrate. The placement of an interconnect trace (X_4) above the undercut region reduces the effective capacitance to the lossy substrate (C_4) through the same mechanism as 'B'. On the other hand, the value of C_3 is the same as it would be without micromachining, and is hence higher than C_4.

D. There is an extra capacitance, C_2, which is introduced due to the top metal layer mask, X_5. This is shown only in the left side of Figure 1-4. The top mask is used to protect the circuits region in the post-foundry micromachining process. This mask is usually grounded, causing a direct capacitance to ground. However, the losses are less compared to coupling to the lossy silicon substrate.

These aspects of micromachining impact the VCO design in the following ways:

1. X_1 and X_2 can move. This is the priniciple of reconfigurable capacitors [3].

2. Inductors also use X_1 and X_2, but are mechanically fixed by choice of layout topology [5].

3. X_6 and X_7 show how the top thick metal layer can be used for routing, without hindering the micromachining process. Using X_6 instead of X_7 reduces interconnect loss. Here, X_6 serves the dual purpose of a mask as well as a routing wire.

1.5 Thesis Outline

Chapter 2 describes the mechanisms that cause phase noise and presents mathemetical expressions for phase noise. Chapter 3 describes the VCO design comprising of the LC tank and the active circuitry. Chapter 4 discusses the implemented designs and the measured results. Chapter 5 concludes the thesis with comparisons to previously published work.

2 LC Oscillator Phase Noise Mechanisms

Oscillator performance is measured by phase noise in addition to tuning range and power. This chapter begins by motivating the discussion of phase noise by showing the impact of phase noise on RF systems. It then describes the noise sources in IC implementations of oscillators. Mathematical expressions for phase noise are then introduced to allow quantification of trade-offs with the tuning range and power specifications.

2.1 Phase Noise in RF Systems

Oscillators' noise performance is affected by the thermal, shot and flicker noise of the active and passive devices found in integrated circuits. When this noise is superimposed on the output periodic signal of the oscillator, it leads to a random variation in the output's frequency and amplitude. These random variations in the frequency can also be regarded as random changes in the position of the zero crossings or phase of the output signal. In this regard, this noise is usually referred to as 'phase noise'. From the equipartition theorem of thermodyanimcs, half of this noise takes the form of amplitude noise and the other half as phase noise [9]. All oscillators have an amplitude control mechanism that prevents amplitude increase without bounds. Also, the negative resistance does not let the amplitude decrease beyond a certain limit. Hence, amplitude noise is not significant. On the other hand phase noise is a concern as it cannot be removed by the oscillator.

Figure 2-1 (a) shows the single spike of energy at the center or carrier frequency, ω_o for an ideal oscillator, while Figure 2-1 (b) shows the "skirts" around ω_o due to phase noise. Phase noise is usually

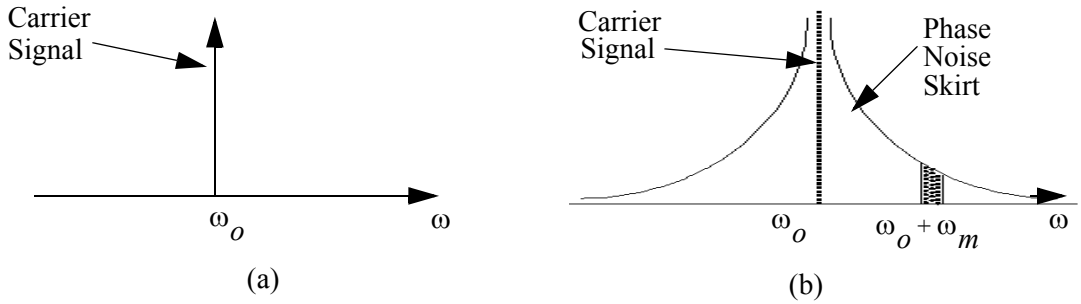


Figure 2-1. Output spectra of (a) ideal oscillator (b) practical noisy oscillator

expressed as the power at a particular offset, ω_m from ω_o, with respect to the power at ω_o. The oscillation signal power is measured in a 1 Hz measurement bandwidth at ω_m. The unit of phase noise is dBc/Hz, read as 'decibels below the carrier per hertz'.

Phase noise is important in RF systems because it degrades system performance by reducing the signal integrity of the outputs of a transceiver [10]. In the receive path, the incoming signal has to be demodulated by convolving with a local oscillator (LO) signal which has phase noise. An interfering signal close to the desired signal is also convolved due to the oscillator 'skirts', producing 'skirts' in the demodulated interferer. These 'skirts' fall on the desired signal, degrading signal integrity. Similarly in the transmit path, the 'skirts' of the transmitted signal will degrade the signal of another receiver which is operating at a frequency near to that of the transmitted signal.

Section 2.2 discusses an intuitive understanding of noise sources and spectrum folding. Section 2.3 describes an analytical expression for phase noise, which is based on a classical model. Section 2.4 develops a mathematical model for phase noise based on an analogy with a Brownian particle and concludes by showing agreement with the classical model of Section 2.3.

2.2 Phase Noise Sources and Noise Spectrum Folding

To understand phase noise around the carrier, we need to look at the noise sources of an oscillator as well as the transformations they undergo due to the circuit. The switching action of the cross-coupled pair [11] can be used to understand the frequency translations of noise. There are two consequences of the switching action. First, noise components across the spectrum are 'upconverted' or 'downconverted' to the

carrier frequency, just as in a mixer. This is a non-linear phenomenon. The second is that noise (which rides on the switching voltage), changes the instant when the currents are switched across the cross-coupled pair. This event happens twice in each oscillation cycle, since there are two transistors in the cross-coupled pair. Hence, noise is sampled at $2\omega_o$. When a signal is sampled at a frequency of $2\omega_o$, the signal spectrum repeats at every multiple of $2\omega_o$. Aliasing takes place if the signal has a bandwidth greater than ω_o. Noise is not constrained within a bandwidth and has components throughout the frequency spectrum. Hence due to aliasing, noise at frequencies greater than ω_o fold back to ω_o. This is a linear phenomenon in contrast to the first method, since this is frequency translation due to aliasing, rather than translation due to upconversion or downconversion.

A conceptual schematic of the cross-coupled oscillator used in this work is shown in Figure 2-2, where R_p models the resonator loss. There are three broad categories of noise sources which contribute to phase noise around the carrier [12].

2.2.1 Resonator Noise

Thermal noise of R_p is shaped by the resonator bandwidth. Thus only noise component around ω_o is significant. Assuming that the switching time is zero, this noise will be samped by impulses repeating at $2\omega_o$. Hence it will repeat every $2\omega_o$, appearing at ω_o, $3\omega_o$ etc. However, again due to the band-pass fil-

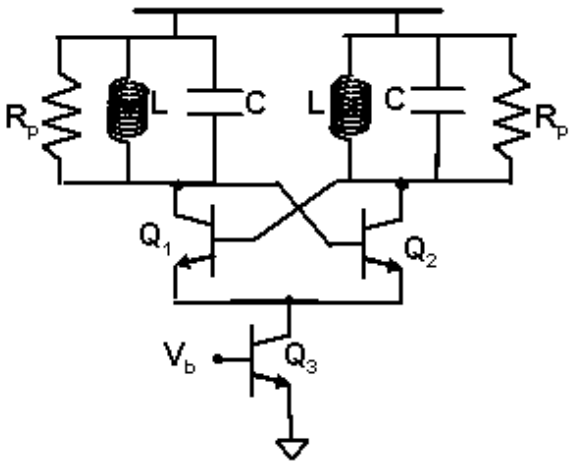


Figure 2-2. Conceptual schematic of cross-coupled LC-VCO

tering of the resonator, components at $3\omega_o$ and higher are attenuated, leaving the component at ω_o to dominate.

2.2.2 Tail Current Noise

The tail current noise can be represented as a equivalent noise voltage source at the base of Q_3. It is transformed due to the non-linear switching action of the cross-coupled pair. This non-linearity manifests itself by mixing the base voltage with the cross-coupled switching voltage (whose frequency is the oscillator free running frequency, ω_o). This is then equivalent to a single-balanced mixer [10], whose tail current source is now driven by a broadband noise signal. Since this mixer shows the largest conversion gain around the fundamental frequency, only mixing by fundamental at ω_o is important. Also, a mixer both upconverts and downconverts around the switching frequency. However, we are only concerned about the components that appear around the carrier at ω_o. Hence, flicker noise, which dominates at ω_m, is upconverted to $\omega_o \pm \omega_m$. Thermal noise, which dominates at $2\omega_o \pm \omega_m$, is downconverted to $\omega_o \pm \omega_m$. The process of upconversion leads to amplitude modulation (AM) sidebands only, which in the presence of a non-linear varactor will convert in frequency modulation (FM) sidebands. This is because AM changes the reverse bias randomly, thereby changing the capacitance, which in turn changes the frequency, resulting in FM. Noise around $2\omega_o$, though, results in direct phase noise. A noise filter [13] can be used to reduce that effect by capacitively shorting the $2\ \omega_o$ noise to ground.

2.2.3 Differential Pair Noise

To understand how white noise in the differential pair, Q_1 and Q_2, is sampled at $2\omega_o$, one would have to consider the finite switching time of the differential pair. This is because, unlike resonator noise, differential pair noise has significant components across the entire spectrum (as there is no filtering). Hence sampling by an impulse train would lead the noise around the carrier to increase without bound. The aliased noise also depends on the width of the sampling period. The smaller the period, more is the sampling bandwidth. The input referred noise of a differential pair is inversely proportional to its transconductance. A

larger transconductance translates to a higher bandwidth. Hence, to lower the effect of this noise, it is desirable to keep the sampling period as low as possible. Stated in other words, the transistor should switch as quickly as possible.

Flicker noise, which can be modeled as a random voltage source at the gate of the differential pair, causes unbalance in the differential pair. This again modulates the $2\omega_o$ voltage waveform at the tail, as mentioned above. This results in a noise current in the tail capacitor, proportional to the value of the tail capacitor. This current then mixes down to the oscillation frequency by the same mechanism as described for the $2\omega_o$ thermal noise of the tail current source. Techniques for reducing this noise include decoupling the sources of the differential pair transistors by an optimally chosen capacitor to avoid noise modulation of the $2\omega_o$ voltage waveform at the tail [14].

Figure 2-3 shows how noise from the three sources undergoes frequency translation to appear as phase noise around the carrier.

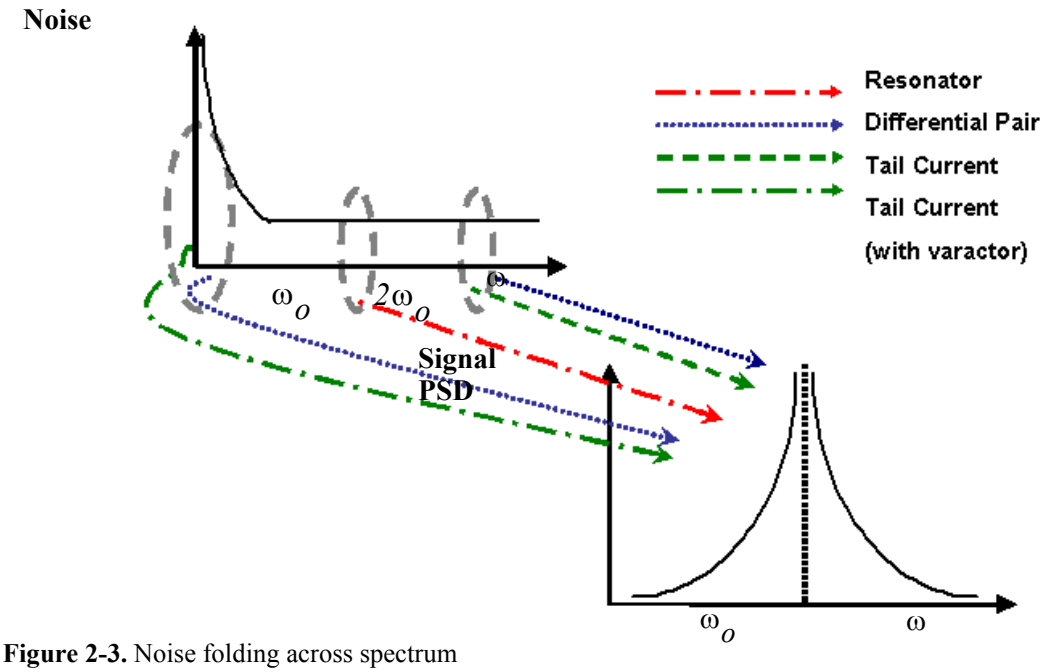


Figure 2-3. Noise folding across spectrum
$2\omega_o$ noise from the differential pair and the tail current source are down-converted to around the carrier. Resonator noise at ω_o directly appears as phase noise. Flicker noise from the differential pair is upconverted to the carrier. Also flicker noise from the tail current source is up-converted in the presence of a non-linear varactor.

2.3 Leeson's model for estimating Phase Noise in a LC-VCO

Since phase noise is an important performance measure for an oscillator, it is convenient to have a simple linear time invariant model to estimate it before design. For this purpose, the classical Leeson's model [15] extended by Scherer [16], to account for flicker noise, can be used. The expression for phase noise calculation at an offset ω_m from the carrier frequency ω_o is

$$L(\omega_m) = \frac{2k_B TFR_p}{r_o^2}\left(\frac{\omega_o}{2Q\omega_m}\right)^2\left(1+\frac{\omega_{m_{1/\omega^3}}}{\omega_m}\right) \tag{2.1}$$

where k_B is Boltzmann's constant, T is the absolute temperature, r_o is the amplitude of oscillation, Q is the resonator loaded quality factor, R_p is the parallel resistance used to model the losses in the resonator, $\omega_{m_{1/(\omega^3)}}$ is the $1/\omega^3$ corner frequency in the phase noise spectrum and F is the excess noise factor. It can be seen from (2.1) that phase noise drops by the square of r_o and tank Q. The reason for the quadratic improvement with Q is that a high Q offers more filtering due to decreased bandwidth, $\Delta\omega = \frac{\omega_o}{Q}$. With a higher Q, more noise is filtered both before aliasing and after aliasing (Section 2.2.1). The reason for the quadratic improvement with r_o is that phase noise is noise normalized to the carrier power, which is $r_o^2/2$.

2.4 Understanding Phase Noise from a Mathematical Perspective

LC oscillator dynamics can be understood by plotting the voltage V across the capacitor and the current I of the inductor in the V-I state space. Due to periodicity, the limit cycle is a closed curve [17]. Regardless of the initial transient in the radial (amplitude) direction, the state would return to the limit cycle, due to the restoring force of the negative resistance from the cross-coupled pair. However any fluctuations along the limit cycle do not experience any restoring force. Thus, in the presence of noise, the state point walks "randomly" across the limit cycle, or the phase undergoes a "diffusion" process.

Phase noise of an oscillator is analogous to the random walk of a Brownian particle [18]. Any Brownian particle when immersed in a fluid walks randomly, as it is continuously bombarded by thermally agitated fluid molecules. This is known as diffusion. When the random force exerted by the fluid molecules has a white spectrum, the variance of the displacement x of the Brownian particle increases proportionally with time i.e., $\langle x^2 \rangle = 2Dt$, where D is the diffusion constant [19].

To derive at a more formal expression for phase noise through this process, one can start by taking N samples of the same oscillator which are taken at the same time (say t_0) after starting them up N different times (T_0, T_1, $T_{2...}T_{N-1)}$. For any stochastic process, average of such N samples is called the ensemble average at any given time (in this case, t_0). An expression of the output voltage, whose phase is modulated by noise expressed as $\phi(t)$, can be represented as $v(t) = r_o cos[\omega_o t + \phi(t)]$. The ensemble average, at any given time, t, is

$$\begin{aligned} \langle v(t) \rangle &= \frac{1}{N} \bullet \sum_{i=1}^{N} r_o [cos(\omega_o t + \phi_i t)] \\ &= \frac{r_o}{N} \bullet cos[\omega_o t] \sum_{i=1}^{N} cos[\phi_i(t)] - \frac{r_o}{N} \bullet sin[\omega_o t] \sum_{i=1}^{N} sin[\phi_i(t)] \end{aligned} \tag{2.2}$$

This can be re-written, in terms of ensemble averages, as

$$\langle v(t) \rangle = r_o [cos(\omega_o t) \langle cos\phi(t) \rangle - sin(\omega_o t) \langle sin\phi(t) \rangle] \tag{2.3}$$

To find $\langle cos\phi(t) \rangle$ and $\langle sin\phi(t) \rangle$, we use the statistical theory for transformation of variables:

$$\langle cos\phi(t) \rangle = \int_{-\pi}^{\pi} (cos\phi(t)) P(\phi, t) d\phi \tag{2.4}$$

A similar formulation can be written for $\langle sin\phi(t) \rangle$. As shown in [20], the motion of an ensemble of Brownian particles, which at t=0 are at X=0, can be characterized by a Weiner Process, $X(t)$. Due to the

analogy of phase with position, $\phi(t)$ can also be considered as a Weiner process, the pdf of which is gaussian, and is described at any given time, *t,* as:

$$P(\phi, t) = \frac{1}{\sqrt{2\pi\sigma^2(t)}} e^{\left[-\frac{\phi^2}{2\sigma^2(t)}\right]} \tag{2.5}$$

where $\sigma^2(t) = \langle \phi^2(t) \rangle = 2Dt$

Substituting (2.5) in (2.4) yields $\langle cos\,\phi(t) \rangle = e^{(-\langle \phi(t)^2 \rangle / 2)}$ and $\langle sin\,\phi(t) \rangle = 0$. This can also be deduced intuitively since, the pdf, being gaussian, is symmetric about the origin, hence multiplying and integrating with an odd function (*sin*(-*x*)=-*sin*(*x*)), will result in zero, while the same operation with an even function (*cos*(-*x*)=*cos*(*x*)), will result in non-zero values. Substituting the values of $\langle sin\,\phi(t) \rangle$ and $\langle cos\,\phi(t) \rangle$ in (2.3) yields

$$\langle v(t) \rangle = r_o e^{(-Dt)} cos(\omega_o t) \tag{2.6}$$

If there was no phase noise, the ensemble average would remain constant and never decay. The decay rate, which is exponential, as derived in (2.6) clearly depends on the diffusion constant, *D*. The bigger the value of *D*, the faster would be the decay rate, implying more phase noise.

Phase noise is expressed in terms of power spectral density, and power spectral density is the fourier transform of the autocorrelation function. The autocorrelation function is defined by $R_v(\tau) = \langle v(t) \rangle \langle v(t+\tau) \rangle$. Hence,

$$R_v(\tau) = \frac{r_o^2}{2} \langle cos[\omega_o(2t+\tau) + \phi(t) + \phi(t+\tau)] + cos[\omega_o(\tau) + \phi(t) - \phi(t+\tau)] \rangle \tag{2.7}$$

Using the same procedure as used above to find $\langle v(t) \rangle$, we obtain an expression similar to (2.6) for $R_v(\tau)$,

$$R_v(\tau) = \frac{r_o^2}{2} e^{(-D|\tau|)} cos(\omega_o t) \tag{2.8}$$

The power spectral density (PSD), $S_v(\omega)$, is then found by using the following Fourier transform

$$e^{(-D|\tau|)} cos(\omega_o t) \leftrightarrow \frac{2D}{D^2 + (\omega_m)^2} \tag{2.9}$$

where $\omega_m = \omega - \omega_o$.

Phase noise at any given offset ω_m is given by the ratio of the power spectral density at $\omega_o + \omega_m$ to the total oscillation energy $r_o^2/2$, which is given by

$$L(\omega_m) \equiv \frac{S_v(\omega)}{\left(r_o^2\right)/2} = \frac{2D}{D^2 + (\omega_m)^2} \tag{2.10}$$

For large $\omega_m >> D$, the spectrum has the familiar $1/f^2$ dependence. But if D is large, then for frequencies less than D, the spectrum will be almost independent of frequency. D tends to be large for small C (which is required for low power operation), as will be explained in Section 3.1, and is hence relevant for the designs discussed in this work. A plot of the phase noise spectrum for some values of D are shown in Figure 2-4.

The expression of D for a Brownian particle undergoing diffusion is given by Einstein's relation [19] - [21],

$$D = \frac{k_B T}{M} \bullet \frac{1}{\gamma} \tag{2.11}$$

where γ is the frictional coefficient, M is the mass and $k_B T/M$ is the sensitivity factor, which arises from the equipartition theorem stating that each independent degree of freedom in a system in equilibrium has a mean energy of $k_B T/2$, that is $<MV^2/2> = k_B T/2$, where V is the velocity of the particle, or $<V^2> = k_B T/M$.

Similarly to derive the expression of D for phase noise in an oscillator, one can start by taking a parallel LC tank and lumping all the losses by an equivalent parallel resistance R_p. Though the $\langle v^2 \rangle$ across the capacitor, and the $\langle i^2 \rangle$ across the inductor in the LC tank are correlated to each other, the equipartition theorem can be used as a first order approximation [22] and hence each would then constitute a degree of freedom and will have $k_B T/2$ of thermal energy. Hence $\langle v^2 \rangle = k_B T/C$ and $\langle i^2 \rangle = k_B T/L$, analogous to the $k_B T/M$ sensitivity factor derived above. To derive sensitivity of a brownian particle, one describes it in terms of velocity, V, (time derivative of diffusion displacement). Similarly to find sensitivity for the oscillator, one can take the time derivative of voltage, $\dot{v}$; or current, $\dot{i}$, either one giving the same result. Considering, $\dot{v}$

$$\langle \dot{v}^2 \rangle = \frac{1}{C^2}\langle i^2 \rangle = \frac{k_B T}{LC^2} = \frac{k_B T}{C}\omega_o^2 \tag{2.12}$$

To complete the analogy to the motion of a brownian particle in (2.11), γ remains to be formulated. That simply represents the energy loss (friction) associated with the oscillator, to find which one can either

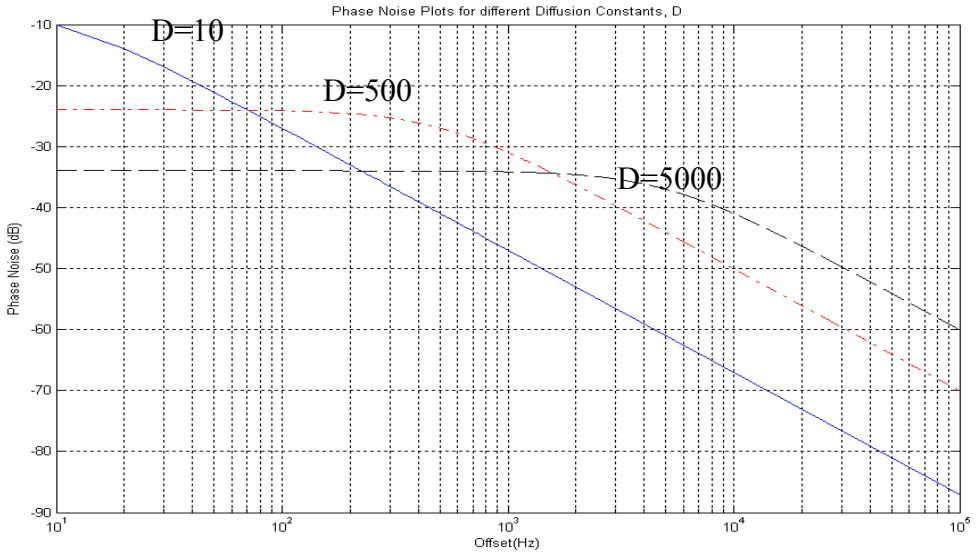


Figure 2-4. Phase Noise Plots for various diffusion constants
An oscillator with very good low frequency phase noise performance will typically have a $D < 10$. Hence the 'flattening' of the spectrum would hardly be observed on the spectrum analyzer. However, as it will be shown soon, low power oscillations obtained by choosing a small C, lead to values of D in hundreds or thousands, the phase noise performance of which are observed by the other 2 plots.

consider the *LR* part of the resonator or the *RC* part, both ultimately yielding the same result. Considering the *LR* part, the current in the circuit satisfies $i = -\left(\frac{L}{R_p}\right)\dot{i}$. Comparing this with the equation of motion $\dot{V} = -\gamma V$, one can find the expression for γ

$$\frac{1}{\gamma} = \frac{L}{R_p} = \frac{1}{\omega_o Q} \tag{2.13}$$

Combining (2.12) & (2.13), D can be written as

$$D = \frac{1}{r_o^2}\langle \dot{v}^2 \rangle \frac{1}{\gamma} = \frac{1}{r_o^2}\frac{k_B T \omega_o}{C}\frac{}{Q} \tag{2.14}$$

where r_0 is the oscillation amplitude (same as r_0 in (2.1) - (2.10)) and $1/r_0^2$ converts the voltage diffusion to phase diffusion.

Also, as seen from (2.14), in order to keep *D* small, to get better phase noise, one would need to increase either r_o, or *C* or the tank *Q*. In contrast, the purpose of low power is best served by increasing *Q*, but decreasing *C* (as will be explained in Section 3.1) and r_o. During design, one would take the best *Q* achievable given the center frequency and tuning range constraints. r_o would be constrained to operate the oscillator in the current limited regime [22]. The only other parameter left in the control of the designer is *C*. As seen from Figure 2-5, one would try to keep *C* greater than 0.5 pF, due to the sharp increase in *D* observed for values of *C* less than that. In practice, power and tuning range constraints place a limit on how big *C* can be, as will be seen in the next chapter.

The Q of a tank is defined by $Q = \omega_o \frac{E_{stored}}{P_{sig}}$, where E_{stored} is the energy stored and P_{sig} is the power dissipated in the resonator. The energy stored in the capacitor is $Cr_o^2/2$. Substituting this in (2.14) yields the following relationship for *D*

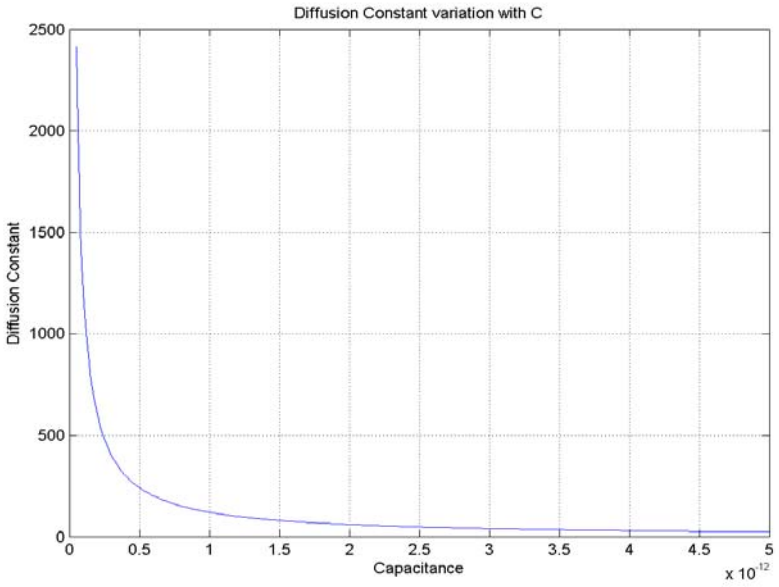


Figure 2-5. Variation of diffusion constant, D with tank capacitance, *C*
This is plotted for approximate values of one of the designs. The center frequency is 3 GHz, tank *Q* is 10 and the amplitude of oscillations (p-p) is 0.5 V. There is a sharp increase in *D* for values of *C* less than 0.5 pF. Hence, from the phase noise perspective, one would choose C > 0.5 pF. However, both tuning range and low power purposes may be served with *C* < 0.5 pF.

$$D = \frac{k_B T}{2P_{sig}}\left(\frac{\omega_o}{Q}\right)^2 \tag{2.15}$$

For $\omega_m >> D$, and for the value of D as found in (2.15), (2.10) can be re-written as

$$L(\omega_m) = \frac{2D}{(\omega_m)^2} = \frac{k_B T}{P_{sig}}\left(\frac{\omega_o}{\omega_m Q}\right)^2 \tag{2.16}$$

Re-writing (2.1) in terms of P_{sig}, we obtain

$$L(\omega_m) = \frac{2k_B TF}{P_{sig}}\left(\frac{\omega_o}{2Q\omega_m}\right)^2\left(1 + \frac{\omega_m 1/\omega^3}{\omega_m}\right) \tag{2.17}$$

Neglecting the *1/f* noise effect and ignoring the empirical fitting parameter *F*/2, (2.17) is the same as (2.16). Hence the diffusion theory is consistent with the Leeson's model.

3 VCO Design

In this chapter, we discuss how phase noise trades-off with the essential requirements of the architecture, namely, low power, wide tuning range. We start off by discussing the phase noise - power trade-off in the chosen topology. This trade-off is discussed with respect to each of the parameters that controls phase noise, namely, voltage swing (r_o) and Q. Low power and wide tuning range motivate use of micromachining, which is introduced in Section 3.2. The remainder of design considerations for a complete IC implementation are covered in Section 3.3

3.1 VCO Topology

It was seen in Chapter 1 that the cross-coupled configuration was the preferred configuration for integrated LC-VCOs. Either two cross-coupled pairs (one n-MOS, one p-MOS) can be connected in parallel in a 'CMOS VCO' or a single BJT cross-coupled pair can be used in a 'bipolar VCO'. CMOS is preferred for cost reasons in mixed-signal applications. However, BJT outperforms MOS in terms of f_T, g_m/I and flicker noise considerations. These effects are further enhanced with Silicon Germanium (SiGe) Heterojunction Bipolar Transistors (HBTs) [23] [24], since the higher β can be traded off for smaller base resistance by increasing base doping, thereby reducing noise. The reduction of bandgap by adding Ge in the base, aids in further increasing f_T.

The drawback of a high g_m/I ratio is that the noise current is proportional to g_m, and hence a higher ratio means more noise for the same bias current. However, the bias current consumed to cancel the tank losses is itself less due to the higher g_m of the HBTs. This is one of the ways in which phase noise trades-off with power. Since low power was the driving force for the targeted application, the higher g_m/I ratio of the bipolar led to its use for the designs in this work.

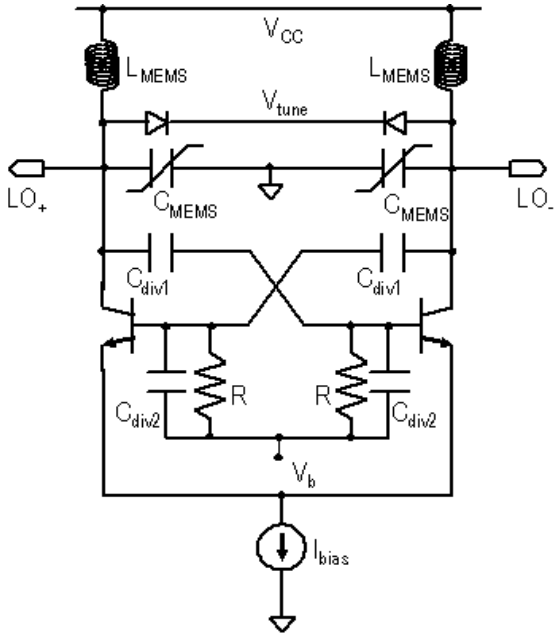


Figure 3-1. LC-Tank VCO schematic
Schematic showing the cross-coupled pair with the micromachined LC-tank. I_{bias} is implemented as an on-chip current mirror of an off-chip current source.

Figure 3-1 shows the bipolar cross-coupled configuration used in this work. DC-decoupling the base and collector of the cross-coupled pair with a capacitive divider (C_{div1} and C_{div2}) prevents forward bias of the C-B junction, thereby allowing more swing at the collectors. Also since the inductors are connected directly to V_{CC}, swing higher than V_{CC} is possible. This is because the two ends of an inductor have to swing equally in opposite directions around V_{CC} to ensure that the inductor does not see a large DC drop. While increasing the current to increase the swing, r_o, improves phase noise (2.1), it does so at the cost of increased power consumption. On the other hand, as seen in Section 2.3, phase noise improves quadratically with tank Q, and it does so without any increased power consumption. Additionally, a high Q implies that less power is needed to cancel the tank loss, to initiate and sustain oscillations. Hence, low power implementation is best served by increasing the Q of the tank.

3.2 Micromachined LC Tank Design

The LC tank comprises of a micromachined inductor and reconfigurable capacitor for discrete tuning. A small varactor diode is also included in the tank for analog tuning. The losses associated with the

inductor and capacitor are usually represented as a series resistance *(R_{sL}* and R_{sC} respectively). A simple first order expression for the *Q* of these passives is given by

$$Q_L = \frac{\omega L}{R_{sl}} \; ; \; Q_C = \frac{1}{\omega R_{sC} C} \tag{3.1}$$

However, it is not the individual *Q*s, but the tank *Q* which affects VCO performance. Since a parallel LC tank is implemented, the series losses associated with *L* and *C* are first converted to equivalent parallel resistance, by the relation $R_p \approx Q^2 R_s$. The tank *Q* is then derived in the following way:

The characteristic impedance of the tank is

$$Z_o = \frac{1}{\omega C} = \omega L = \sqrt{\frac{L}{C}} \tag{3.2}$$

The total equivalent parallel loss resistance is then $R_p = R_{pC} // R_{pL}$. Since $Q_T = \frac{R_p}{Z_o}$;

$$\frac{1}{Q_T} = \frac{Z_o}{R_p} = Z_o\left(\frac{1}{R_{pL}} + \frac{1}{R_{pC}}\right) \tag{3.3}$$

Substituting (3.2) in (3.3), we obtain

$$\frac{1}{Q_T} = \left(\frac{\omega L}{R_{pL}} + \frac{1}{\omega C R_{pC}}\right) \tag{3.4}$$

Substituting (3.1) in (3.4), we get

$$\frac{1}{Q_T} = \left(\frac{1}{Q_L} + \frac{1}{Q_C}\right) \tag{3.5}$$

From (3.5), it can be seen that the tank quality factor will be dominated by the *Q* of the passive, whose *Q* is lower. From (3.1), it can be deduced that Q_L will dominate at low frequencies and Q_C at higher frequencies. In practice, as it will be seen in Section 3.2.1, Q_L does not keep on increasing with frequency,

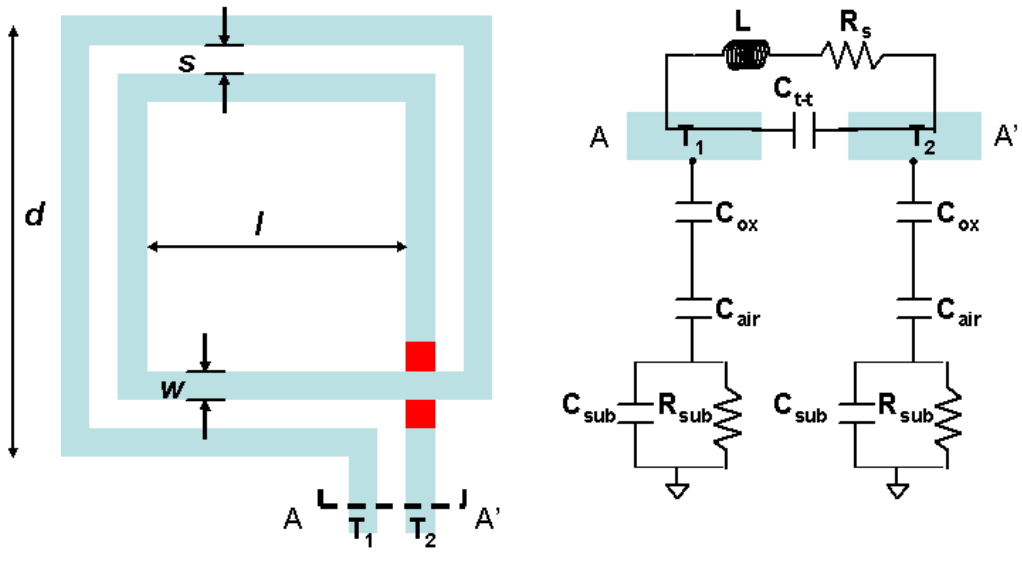
as suggested by (3.1), but drops down due to high frequency effects. Hence, at high frequencies, both Q_L and Q_C are important.

From a low power perspective, it is desirable to use a bigger inductor to achieve the same carrier frequency with a smaller capacitor. This is because current consumption increases with the capacitance in the tank, because a bigger capacitance implies a smaller impedance, and hence more current for the same voltage swing ($I = j\omega CV$). From Section 2.14, it is known that a smaller capacitance is not good from the phase noise perspective, since it leads to a higher value of *D*. However, the phase noise degradation is checked by the improvement in Q_L (and hence Q_T, assuming Q_L dominates), which is achieved due to micromachining, as will be seen in the following section.

3.2.1 Micromachined Inductor Design

3.2.1.1 Model and Loss Mechanisms

Figure 3-2 (a) shows a typical on-chip spiral inductor with n = 2 turns. The underpass (shown in red) allows the inner end of the spiral to be connected to the terminal T_2. The width of the turns is '*w*', spacing between the turns is '*s*', 'd' is the outer diameter of the spiral and '*l*' is the inner diameter or the distance



(a) (b)

Figure 3-2. Top view of spiral inductor (a). Cross-section showing lumped parasitics (b)

between the inner-most turns. Designing an inductor involves choosing n, s, w and d. Figure 3-2 (b) shows a simplified lumped parameter model of the essential parasitics in a spiral inductor. This model is based on [25], and incorporates the effect of micromachining.

R_s models the sheet resistance of the spiral at low frequencies. At high frequencies, 'skin effect' reduces the effective area of cross-section of a wire, increasing the DC resistance with frequency. In addition it also includes the eddy current losses due to two mechanisms. The first is the due to eddy current loops formed in a spiral turn due to field lines of neighboring turns ('proximity effects' or 'current crowding'). The second is due to the eddy current losses induced in the substrate. $C_{t\text{-}t}$ models the capacitance of the spiral with the underpass and the turn-to-turn fringing capacitance. The turn-to-turn capacitance is usually neglected since the adjacent turns are almost equipotential. Besides, in a lumped parameter model, these capacitances add in series before they appear at the ports. C_{ox} is the oxide capacitance coupling the signal from the inductor to the substrate (turn-to-substrate). C_{air} is the contribution of micromachining (effect 'B' in Section 1.4), and represents the capacitance of the substrate area beneath the inductor that has been etched. C_{sub} and R_{sub} are the substrate capacitance and loss respectively.

Figure 3-3 shows the Q plot of an inductor as a function of frequency. Contrary to the expectation from (3.1), the Q of an inductor does not keep on rising with frequency. This implies that there must be losses which increase with frequency and exceed the energy stored in the inductor at some frequency after which Q begins to drop-off with frequency. These losses have magnetic origins (skin effect, proximity effects, substrate eddy currents) and electrical origins (substrate loss due to capacitive substrate coupling).

Skin depth is given by

$$\delta = \sqrt{\frac{2}{\omega \mu_o \sigma}} \tag{3.6}$$

where σ is the conductivity of the material and μ_o is the permeability of air. This is equal to 4 μm at 0.5 GHz. The thickness of the top metal layer (in which the inductor is usually laid out) of modern processes typically does not exceed 4 μm. Hence, skin effect starts to manifest itself after 0.5 GHz.

For bigger inductors (which are required for low power), both *n* and *d* tend to be larger. Hence, losses produced due to eddy currents flowing in the substrate and due to the proximity effect dominate. The eddy current loss in the substrate has been shown to be proportional to $(n\omega)^2 d^3_{avg}$ [26], where d_{avg} is the average of the inner (*l*) and outer diameters (*d*), showing that these effects increase with size, number of turns and frequency. Similarly, with increasing *n*, current crowding (proximity) effects start to dominate [27]. This constricts the current flow to the inside edge of the spiral (nearest the center of the spiral), again increasing the effective series resistance with frequency. It has been shown [28], that these effects are again either quadratically or linearly proportional to frequency. Hence, eddy current losses dominate over the skin effect, which increases only by the square root of frequency. For micromachined inductors, substrate loss due to coupling through C_{ox} does not dominate due to the existence of C_{air} in series with $C_{ox.}$ Hence, signal power loss in R_{sub} is highly reduced as a result of micromachining.

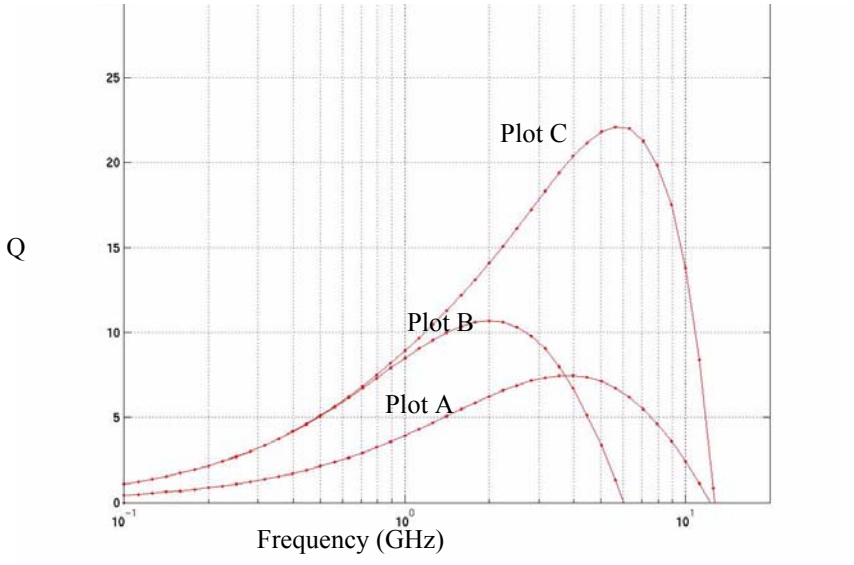


Figure 3-3. *Q* plots of differentially excited simple spiral and symmetrical inductors
Plot A: Two 4 nH simple spiral inductors in series. Plot B: 8 nH symmetrical inductor before micromachining. Plot C: 8 nH symmetrical inductor after micromachining.

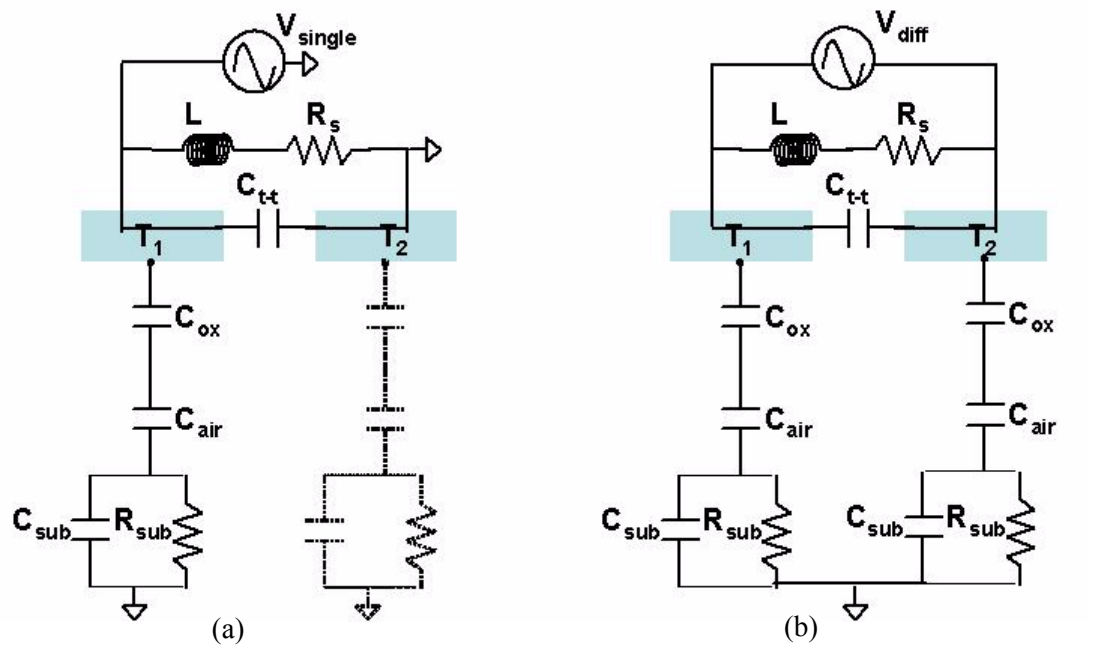
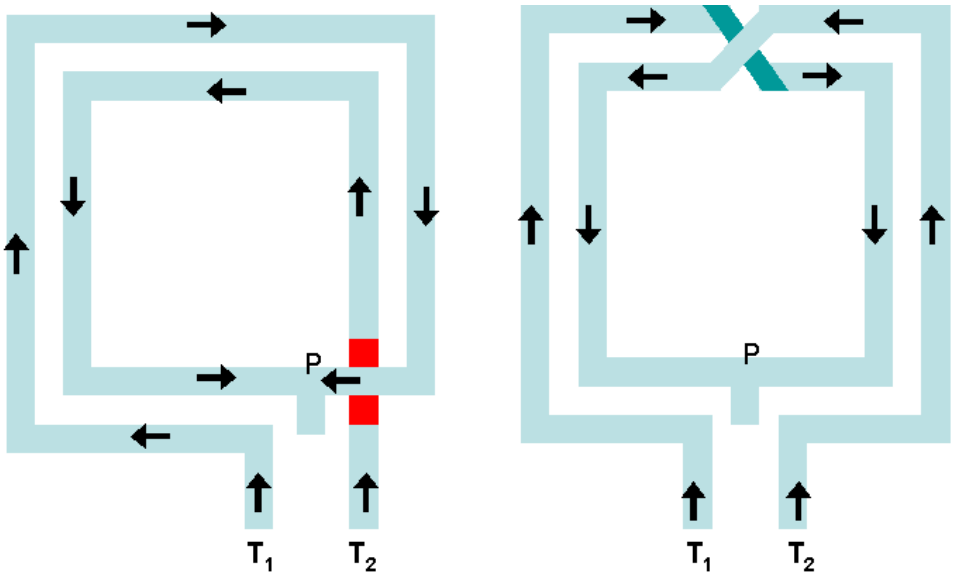


Figure 3-4. Single-ended (a) and Differential (b) excitation of an inductor
Due to the differential excitation, the effective R_{sub} is $2*R_{sub}$ and the effective capacitances (C_{ox}, C_{air}, C_{sub}) are reduced by a factor of 2.

Increasing R_{sub} by using a fully depleted Silicon-On-Insulator (SOI) or Silicon-on-Sapphire (SOS), reduces substrate losses, leaving the proximity effect to dominate [29]. Other than by micromachining, C_{ox} effects can also be reduced by using a Patterned Ground Shield (PGS) [30], but at the expense of self-resonance frequency (frequency at which Q of an inductor becomes zero). This is because PGS is implemented in a conductive IC fabrication layer that is closer to the inductor than the silicon substrate. This increases C_{ox}, but at the same time drastically reducing R_{sub}, with the result that though substrate losses are reduced, self-resonance frequency is also reduced. Since bigger inductors are desired for this low power application, a sacrifice in self-resonance cannot be afforded as it would severely restrict the frequency range for which the inductor can be used.

Beyond decreasing losses by micromachining, Q can be further enhanced by differential excitation. This is compatible with the differential topology of the VCO. Differential excitation leads to increased Q at higher frequencies due to the fact that the parasitics have a higher impedance when excited differentially [31], reducing the real part and increasing the reactive part of the input impedance (Figure 3-4).



(a) (b)

Figure 3-5. Differential excitation of simple spiral (a) and symmetrical (b) spiral inductors
The cross-overs are denoted in different colors from the spiral turns. *C* denotes the center tap, which can be used to define the DC voltages at T1 and T2.

Figure 3-5 (a) shows the simple spiral being excited differentially. The arrows inside the turns show the flow of DC current. For this topology to work as expected, the inductance, and losses from T_1 to P and T_2 to P should be the same. As can be seen from the figure, it would not be possible to redraw the simple spiral in any way to ensure that. Two separate spirals can also be used between T_1 and T_2, the Q plot of which is shown as Plot A in Figure 3-3. The third option is to layout the inductor symmetrically as shown in Figure 3-5 (b). It can be seen that now the path from T_1 to P and T_2 to P is identically the same. In addition, there is no need to use two separate spirals. Since the occupied area is now almost halved, symmetrical layout also leads to better Q as can be seen from Plot B in Figure 3-3. It can also be seen from this plot that the self-resonance frequency is reduced compared to Plot A. The turn-to-turn fringing capacitance, which had been ignored till now for reasons mentioned before, now becomes significant. This is because adjacent turns are now anti-phase. This also causes the capacitances to appear in parallel and add before appearing at the terminals. Additionally, there is a significant cross-over capacitance, as seen in Figure 3-5 (b).

Plot C shows how Effects A and B (Section 1.4) of micromachining result in a higher resonance frequency in addition to improved Q. It should be noted that these effects are visible only if the proximity effect does not dominate.

Hence, a symmetrical layout micromachined inductor has been used for most of the differential VCO designs discussed in this work. The following sub-section gives some insights on designing the inductor.

3.2.1.2 Design trade-offs

A given value of inductance can be achieved by increasing d, n [32] or by decreasing s (decreasing s leads to larger n for same d). Increasing d leads to more eddy current losses in the substrate. Increasing n leads to more eddy current losses in the substrate and proximity effect losses.

The following presents the directions in which the parameters can be changed, their consequences, and the limits:

1. d: Increase d until limited by application-specific area constraints and eddy current losses in substrate.

2. w: Increase w for reduced DC R_s till the point that eddy current losses dominate.

3. s: Decrease s for a higher inductance/area ratio due to tighter magnetic coupling, the limit being set by turn-to-turn capacitance and the fact that MEMS Design Rule Checks (DRCs) [33] make its imperative to leave a certain amount of space, to ensure complete release of the inductor.

4. n: Increase n for higher inductance/area ratio, the limit being set by proximity effects and substrate eddy currents.

5. l: As a rule of the thumb [34], $l \geq 5w$, to decrease the negative mutual coupling between opposite sides of the inductor.

6. As a rule of the thumb [34], at least $5w$ space should be maintained between the outer turn of the spiral and any surrounding metal features to decrease any parasitic magnetic and electrical coupling.

3.2.2 Micromachined Capacitor design for discrete tuning

As discussed in the Section 3.1, low power favors the choice of a small capacitance in the tank. However, some capacitance would still be needed to get the desired center frequency. Also a minimum capacitance would be needed to achieve an acceptable phase noise due to the fact that phase noise is the $\frac{kT}{C}$ noise, due to sampling, shaped by the bandpass tank filter. Additionally, if this capacitor can be made to be discretely tunable, then a wide tuning range can be divided into much smaller discrete ranges, within which, fine tuning can be further achieved. The smaller fine tuning needed relaxes the requirements of the lossy non-linear varactor diode (to be discussed in Section 3.2.3). This relaxation is crucial in the tuning range - phase noise trade-off, since achieving a wide tuning range with an analog tuning varactor comes at the expense of non-linearity, hence phase noise (Section 3.2.3.1). To achieve a wider tuning range and higher *Q*, it is also essential to reduce the fixed parasitic capacitances to the lossy substrate. This is the motivation behind using a reconfigurable micromachined capacitor.

The capacitor is formed by interdigitated beams fabricated using interconnect layers in the BiCMOS process [3]. Micromachining the chip after foundry fabrication allows sets of beams to move with respect to each other. This change in the gap between the beams leads to a change in capacitance. A wider tuning range can be achieved by adding fingers to the beams [35]. For operation with zero-standby power, a lateral mechanical latch composed of a "peg" in a slot is used. This latch defines the discrete values of the gaps between the beams or the overlap area between the fingers. In this thesis, we focus on the simplest case of reconfigurable capacitor: one that has only two states. Hence, the frequency range is only divided into two discrete frequencies.

From the VCO design perspective, to get an insight into the parameters of the capacitor affecting tuning range (*R*), the following equations are considered:

$$R = \left(\frac{f_{max} - f_{min}}{f_{center}} \right) \tag{3.7}$$

where f_{max}, f_{min} and f_{center} are the maximum, minimum and center frequencies respectively.

Replacing each frequency by $\frac{1}{2\pi\sqrt{LC}}$, and pulling out the $\frac{1}{2\pi\sqrt{L}}$ term, (3.7) can be written as

$$R = 2\left(\frac{\frac{1}{\sqrt{C_{min}}} - \frac{1}{\sqrt{C_{max}}}}{\frac{1}{\sqrt{C_{max}}} + \frac{1}{\sqrt{C_{min}}}}\right) \tag{3.8}$$

This can be re-written in a ratio form as

$$R = 2\frac{\left[\sqrt{\frac{C_{max}}{C_{min}}} - 1\right]}{\left[\sqrt{\frac{C_{max}}{C_{min}}} + 1\right]} \tag{3.9}$$

C_{max} and C_{min} in these equations include the fixed parasitics of the MEMS capacitors, routing wire parasitics in the tank connecting the inductor and capacitor (which tend to be significant due to the large sizes of the micromachined capacitors), varactors, coupling capacitors and swing enhancing MIM capacitors (as will be discussed later). Tuning range can be increased by either decreasing C_{min} or increasing C_{max}. C_{max} is limited by the area and power constraints. Once C_{max} is chosen, C_{min} is typically set by the fixed capacitances. The value of C_{min} is not only important for the highest frequency that can be achieved, but also from the phase noise perspective, since the worst phase noise is achieved in this configuration.

Due to the discrete reconfiguration of the MEMS capacitor, non-linearity is not an issue. This avoids linearization techniques that can be achieved by connecting a fixed capacitor in series [36] or parallel [37] with the varactor. The former is at the expense of tuning range while the latter requires additional mixed-signal control. The zero-power micromechanical latch used for gap control eliminates the need of any additional mixed-signal control for the MEMS capacitor. In addition, a wider tuning range is achieved

because of lower parasitics (as compared to that of semiconductor varactors) in the areas internal to the micromachined capacitor, which are released.

3.2.3 Varactor Diode design for analog tuning

After the frequency range that needs to be spanned by the VCO has been divided into smaller discrete ranges (through the micromachined reconfigurable capacitor), varactors are needed for tuning in these smaller ranges. This will enable coverage of the entire frequency range. The varactor used in the designs were *P*+/*N*- diode varactors. Varactor operation is linked to the junction capacitance appearing due to the formation of the depletion region between the *P*+ and *N* implants. The value of the capacitance depends upon the width of the depletion region, which in turn is controlled by the reverse bias across the junction. The *P*+/*N*- forms the emitter-base junction of a bipolar transistor in which the *N-/P-sub* junction forms the base-collector junction.

3.2.3.1 Direct phase noise trade-off with tuning range

The wider the difference between C_{max} and C_{min}, the higher is the value of the sensitivity of the varactor to amplitude fluctuations [38], which cause the AM-FM conversion of phase noise (Chapter 2). This is because, due to the non-linearity of the *C-V* curve, the time-average capacitance is not equal to the small-signal value at the bias voltage [39]. In order to get the highest tuning range, varactors in oscillators are usually biased in the region of the steepest slope of the C-V curve. However, this is the most non-linear region of the C-V curve. This is the main motivation behind using the micromachined capacitors for discrete reconfiguration, as it breaks up the entire frequency range into smaller ranges. Thus the varactor is only needed to tune a small range, reducing AM-FM conversion, hence reducing phase noise.

3.2.3.2 Indirect Phase Noise trade-off though *Q* with tuning range

Tuning range and *Q* trade-off with each other due to the fact that a higher C_{max} is achievable near forward bias. This motivates biasing the varactor such that it is not strongly reverse biased in the C_{max} configuration. However, such an action can easily cause the varactor to be forward biased during some period

of the oscillation swing. When the junction is forward biased, due to the appearance of the diffusion capacitance and the losses associated with it, Q is largely degraded [40]. This in turn degrades phase noise. This is the trade-off between Q and tuning range and hence between phase noise and tuning range.

3.2.3.3 Design Issues

One end of the varactor needs to be AC grounded as it is connected to the DC tuning voltage, while the other end is connected to the tank. The resistance seen at the anode due to the emitter metal resistance ($\sim 0.3\Omega$) is much lesser than the resistance seen at the cathode due to the base series resistance ($\sim 4\Omega$). Hence the cathode is grounded so that the high series resistance does not degrade the tank Q. However, to reverse bias the junction, the tuning voltage would then need to go above V_{CC}. This is what has been implemented in the designs so far, as they are stand-alone designs, with a pad to an off-chip tuning voltage.

However, when used as a cell in a RF system, the tuning voltage has to be kept within achievable bounds. One way to keep the tuning voltage less than V_{CC} is shown in Figure 3-6. Here C_{c1} and C_{c2} represent the capacitors DC-decoupling the anode from the tank. The floating node can then be set by large resis-

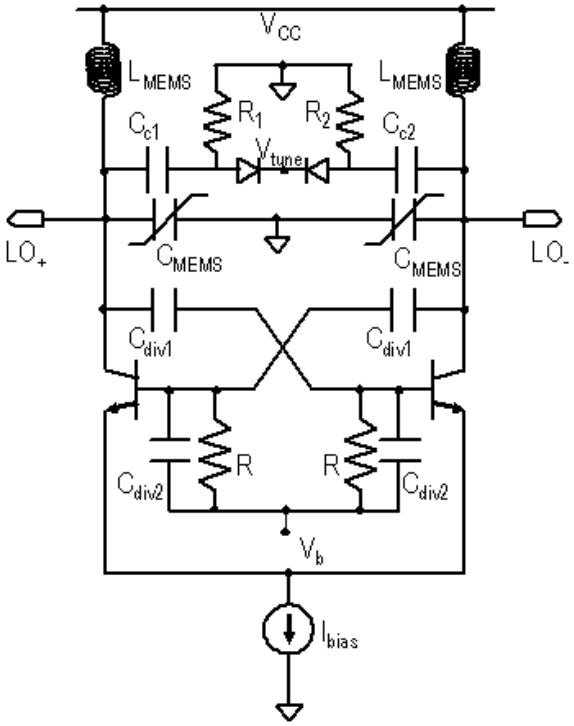


Figure 3-6. Modified VCO schematic with coupling capacitors
Typically $C_{c1}=C_{c2}$ and $R_1=R_2$. The additional circuitry offsets the range of V_{tune}, so that it is now less than V_{cc}

tors R_1 and R_2, which in turn connect those nodes to ground. In order to not limit the tuning range, C_{c1} and C_{c2} should be taken to be much greater than the maximum value of C_{var}, the varactor capacitance. For example is $C_{c1} = 5\ C_{var,max}$, then the equivalent series capacitance only reaches $5C^2_{var,max} / 6C_{var,max} = 0.83C_{var,max}$, resulting in 17% reduction in tuning range. However if they are chosen to be small, they can significantly improve the tank Q (if it is degraded by the varactor Q) as will be seen by the following equations:

$$Q_{var,\,eff} = \frac{(C_c + C_{var})}{\omega C_c C_{var} R_s} \tag{3.10}$$

where $Q_{var,eff}$ is the effective Q of the series combination of C_c and C_{var}. It is assumed that C_c is lossless, R_s is the series losses of C_{var}, $C_{var,eff} = (C_c C_{var})/C_c + C_{var}$ is the effective series combination of the capacitors.

Now, $Q_{var} = \frac{1}{\omega R_s C_{var}}$, where Q_{var} is the varactor Q. Hence (3.10) can be re-written as

$$Q_{var,\,eff} = Q_{var} + \frac{C_{var}}{C_c} Q_{var} = Q_{var} \frac{(C_c + C_{var})}{C_c} \tag{3.11}$$

Hence, smaller the C_c is, more is the improvement in Q_{var}.

By representing the losses as a parallel equivalent, R_p, it can be derived that the effective Q, $Q_{c,eff}$, of $C_{var,eff}$ (with Q as $Q_{var,eff}$) parallel with the MEMS capacitor, C_{MEMS} (with Q as Q_{MEMS}) is given by

$$\frac{1}{Q_{c,\,eff}} = \frac{C_{MEMS}}{Q_{MEMS}(C_{MEMS} + C_{var,\,eff})} + \frac{C_{var,\,eff}}{Q_{var,\,eff}(C_{MEMS} + C_{var,\,eff})} \tag{3.12}$$

This implies that if $Q_{var,eff} < Q_{MEMS}$ then its domination on $Q_{c,eff}$ can be reduced by taking $C_{var,eff} < C_{MEMS}$.

3.2.4 Design Recipe for micromachined LC tanks

The following sub-section presents a design recipe to summarize the previous three sub-sections.

1. Tuning range determines ratio of C_{max} to C_{min} (3.9). This ratio is mainly set by post foundry fabrication constraints and capacitor design topology.

2. C_{max} is the configuration in which maximum power is burnt. For a given tuning ratio, choose the smallest C_{max}. However, C_{min} is the configuration where the worst phase noise is obtained. That sets the lowest limit of C_{min}. The lowest limit of C_{min} is also set by the fixed capacitance associated with C_{max}. Once the values of C_{max} and C_{min} are chosen, the value of inductance is obtained from the desired center frequency.

3. For deciding the dimensions of the inductor, start with the biggest possible area (set by application requirements), smallest width (set by foundry DRCs) and smallest possible spacing (set by foundry and MEMS DRCs). The number of turns is then the only variable left. This is set by the value of inductance required.

3. Estimate the area of the MEMS capacitor for C_{max} and hence estimate the parasitics associated with the routing between the inductor, capacitor and active circuitry. Parasitics play an important role in determining C_{min}, due to the presence of the top-metal ground above the interconnects (Effect D in Section 1.4). This presence can be reduced by partial overlap or by routing through lower metal layers. If the former procedure is adopted, one has to maintain sufficient overlap to ensure that there is no micromachining effect in that region [33]. The latter procedure adds series resistance (due to higher resistivity of lower metal layers) and degrades Q.

4. If multiple hops are implemented and analog tuning is designed to cover the entire hop range, then additional design constraints for the varactor will have to be considered.

5. After choosing the L, C and varactors, the combined Q at the frequency of operation is calculated using (3.5) and (3.12). If the varactor Q dominates, then tuning range would need to be compromised or a

higher C_{max} to C_{min} ratio would have to be designed for. If the MEMS capacitor Q dominates, then multiple banks of capacitors can be combined in parallel to improve Q (since the resistance from the actuators combine in parallel). This however leads to more fixed interconnect capacitance, hence to lower tuning range. If the inductor Q dominates, which should be the case in a typical design space, then directions in which improvement can be attempted are increasing the inductor dimensions and changing turn width to get the optimum trade-off between eddy current losses and DC resistance losses. In this context, it must be noted that if Q_C is less than being 10 times more than Q_L, then one enters the domain of diminishing returns, in which there is not much benefit obtained by increasing Q_L further.

6. Repeat steps 1-5 for different values of C_{min},C_{max} *and* L if the required Q for power and phase noise constraints is not obtained.

3.3 Active Circuit Design

Active circuitry in an oscillator has to compensate for the losses in the LC tank to sustain stable oscillations. The negative resistance provided by a cross-coupled pair is -2 / g_m. If all the losses in the tank can be represented as a parallel resistance, R_p, then for oscillations to begin, the negative resistance should be equal to the positive resistance. In practice, the value of negative resistance is chosen to be 2-3 times less than the value calculated for R_p, because of the large signal degradation of g_m. The value of g_m should not be large, because then the transistors spend most of the time in 'voltage-limited' regime [22]. Too large a g_m results not only in a waste of power but also causes further degradation of phase noise, as the voltage remains constant, but the noise increases proportionally to the bias current [12]. Since, the current is controlled by an off-chip current source, the value of g_m can be adjusted such that the oscillator is biased just before the onset of the voltage-limited regime.

3.3.1 Cross-coupled pair design considerations

During an oscillation cycle, when one of the transistors of the cross-coupled pair is off, the second transistor is on, due to their collectors being anti-phase. If the tail current source is assumed to be ideal then

this off transistor would not load the tank since there is no path for the signal current to flow. However, when both the transistors are on, then even with an ideal current source, there will be a path for the signal through the emitters of the two transistors, and the g_o of the transistors will then load the tank. Hence, effort must be made to minimize the time when both transistors are simultaneously on.

To ensure the transistors are switched off quickly, emitter area of the BJT's in the cross-coupled pair is increased, so that the transistor is biased at a low V_{BE}, and hence a smaller swing at the output would be needed to switch it off during transient. However with increasing area, not only do parasitic capacitances increase, which load the tank and reduce tuning range, but linearity is also compromised due to reduced V_{BE}. To improve linearity, emitter degeneration can be used with the argument that gain is not compromised due to the high β of the SiGe BJT's [41]. However, this is a burden on voltage headroom. With the 2.5 V supply in which the designs were done, this did not turn out to be viable option. The cross-coupled pair sizes were chosen after simultaneous simulations of phase noise, tuning range and linearity to optimize this trade-off.

3.3.2 Capacitive Divider design considerations

The capacitive divider, C_{div1} and C_{div2} (Figure 3-7) is required to enhance the oscillation swing, without causing the transistor C-B junctions to get forward biased. The capacitive divider ratio is chosen to ensure the swing at the base is small, but large enough to cause the transistor to switch off quickly. The C_π of the BJT is big enough to act as C_{div2}, eliminating the need of an external capacitor. The ratio then determines the value of C_{div1}. The series combination of C_{div1} and C_{div2} loads the tank and should be kept as small as possible to improve tuning range, as it presents a fixed capacitance to the tank.

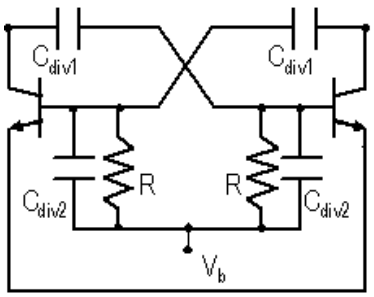


Figure 3-7. Capacitive dividers with cross-coupled transistors.

Due to the decoupling of the base and collectors of the transistors, the base has to be biased separately, which is done by R in Figure 3-7. R should be large enough, so that its thermal noise does not contribute to the phase noise, the limit being set by the voltage drop across it due to the current flowing in the base. V_b is derived from a 'beta helper' current mirror configuration [42] and should be chosen to ensure that the C-B junction of the cross-coupled pair does not become forward biased during the negative swing of the cycle.

3.3.3 Tail current source design considerations

Till now the bias current source was considered ideal. In practice, it is implemented as a current mirror, with finite impedance. The lower the impedance, the more the loading, even when only one transistor is on. SiGe BJT's with increased Early Voltage, V_A, [23] aided in boosting the impedance. Cascodes are not feasible due to voltage headroom and noise due to an added active device. Emitter degeneration of the BJT further enhances the output impedance by a factor of $(1+g_m R_E)$ [42], where R_E is the emitter degeneration resistance. However increasing R_E also tightens voltage headroom. Hence, an optimum value of R_E was chosen (as shown at the emitter of Q_7 in Figure 3-8), that would enhance the output impedance, while consuming less than 100 mV of voltage headroom.

Additionally, as discussed in Chapter 2, flicker noise from the tail current source is upconverted to the carrier frequency in the presence of a non-linear varactor. Hence, in the absence of a varactor, a long MOS transistor (for high output impedance) can be considered as a candidate but with caution, as the dimensions of this transistor tend to get big for smaller overdrives (to ensure more headroom for output swing) and larger bias currents. This increases the drain-bulk capacitance of this transistor, which can be referred to as the 'tail capacitor'.

Though a tail capacitor does reduce the duty cycle of the current waveform (and hence reducing the time when both transistors are on), as well as smoothens the variations at the tail node [43], it also reduces high-frequency output impedance, not only increasing sensitivity to supply voltage variations, but also

increasing the loading on the tank as described earlier. Also, the bigger the capacitor, the more the noise current from the tail node [14]. Hence, the length of the tail transistor was increased till the point the tail capacitor effects started to dominate.

3.3.4 Output Buffer design considerations

A buffer is required between the 50 Ω impedance of the measuring spectrum analyzer and the output of the VCO, without which the analyzer would load the tank, completely ruining the quality factor. A simple Class A topology (emitter follower configuration) is chosen and the bias current is set by the lowest voltage swing level, e.g. for a peak to peak swing of 0.36 V, the minimum current that would need to be set as bias would be 178mV / 50 Ω = 3.5 mA, which will also correspond to -5 dBm of power (rms voltage = 250mV).

The output from the main core can be connected to the buffer through the collector or the base of the cross-coupled transistors. The base connection is the better choice, since it decouples the buffer from the tank to some extent, and also allows the tank to swing much more than what is to be required to be delivered to the load, and hence improves phase noise. If emitter degeneration is used on the cross-coupled pair, then the buffer can also be connected to the emitters of the cross-coupled pair [41]. This connection offers the best isolation from the tank but requires voltage headroom. The base connection has been opted for as is shown in Figure 3-8. The complete schematic of the implemented design is shown in this figure. The thermal noise of the buffer transistors determines the noise floor, and is observed as the high offset frequency flattening of the phase noise spectrum.

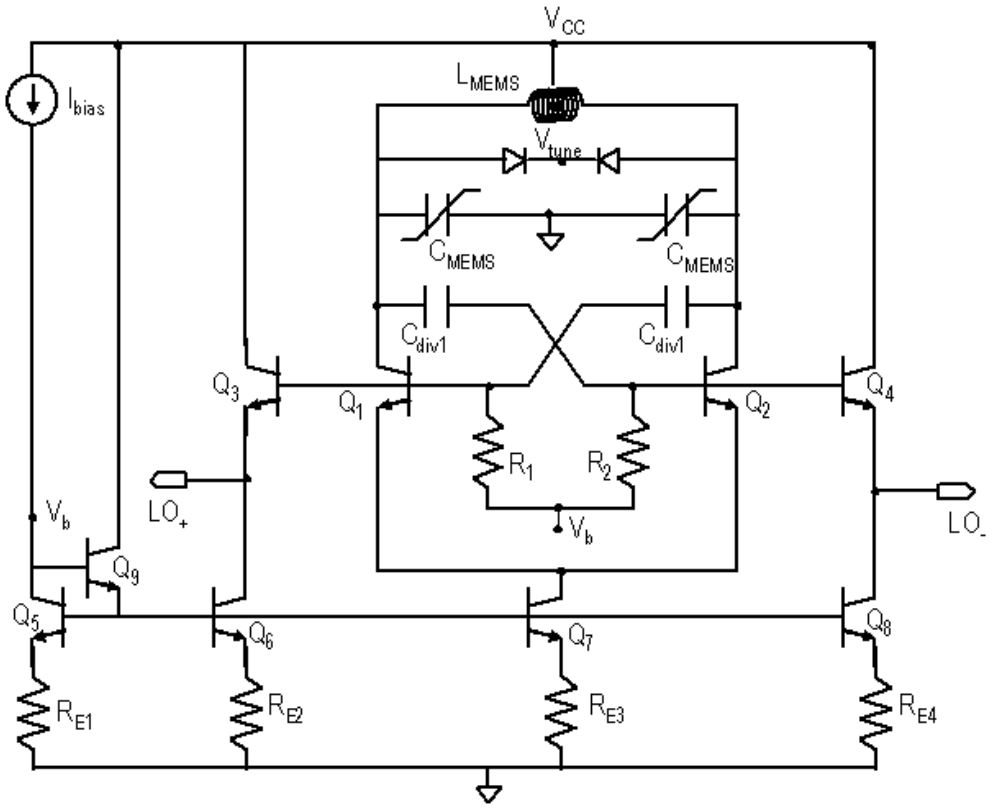


Figure 3-8. Complete VCO schematic.

Q_7 is the tail current source. Q_6 and Q_8 are the currents sources for the buffer transistors, Q_3 and Q_4. R_E denotes the emitter degeneration resistor. LO_+ and LO_- are connected to on-chip signal pads through AC coupling capacitors. AC decoupling capacitors are also added on-chip in most designs from V_{cc}, V_{tune} and V_b to on-chip ground.

4 Fabricated Designs and Measured Results

All designs were implemented in SiGe processes, which had a thick top-metal for the inductor. The chips were micromachined in-house [35] [44] following foundry fabrication. Measurements were made on a Cascade RF Probe Station, using an Agilent Precision Spectrum Analyzer (PSA E4440A), with phase noise personality. The personality enabled a 1-button measurement of phase noise.

Figure 4-1 shows the schematic of the measurement setup. The measurements were made single-endedly, with the other end of the differential output terminated with a 50 Ω load. The signals were either measured with GSG or GSGSG RF probes. The off-chip current source was implemented as a variable resistor. The current across it was measured by a multimeter, and the resistor was varied until the current in the multimeter matched the value needed.

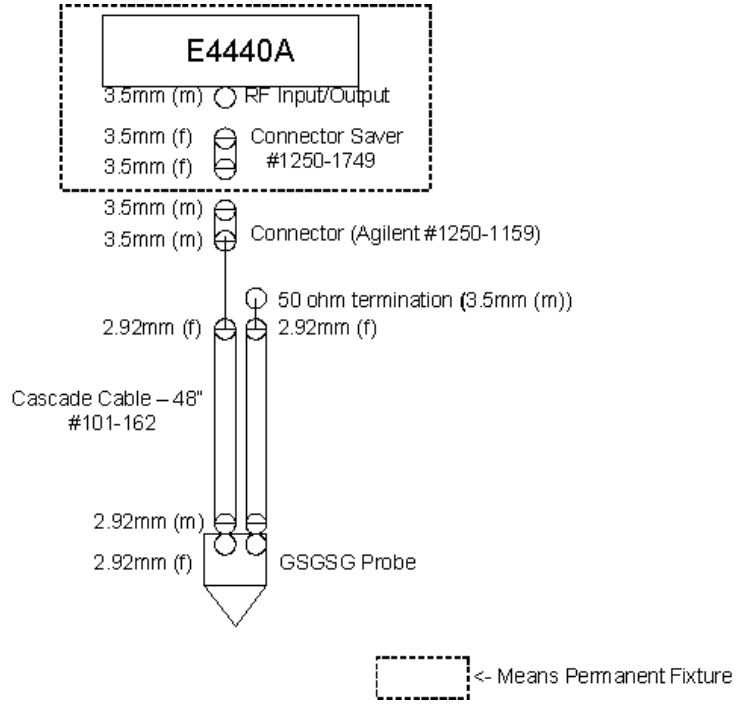


Figure 4-1. Test setup for measuring oscillator performance

AC decoupling capacitors were included to ground any AC signals on the DC lines like V_{cc}, I_{bias} (the connection node for the off-chip current source) and V_{tune} (the connection node for the off-chip tuning voltage for the fine tuning varactor). These decoupling capacitors were added on-chip depending on unused area. AC coupling capacitors are needed to DC decouple the load from the output of the buffer. For the first generation designs, these AC coupling capacitors were implemented off-chip. For the designs thereafter, these capacitors were added on-chip between the output of the buffer and the GSGSG pad.]

There were two generation of designs implemented. The first was that of a reconfigurable oscillator and the second was that of a reconfigurable VCO. Table 4-1 summarizes the differences in implementation between the first generation design and the generations thereafter.

4.1 First Generation Design

This was designed as a reconfigurable oscillator (no fine tuning by varactor, so there is no voltage control). The design goal was to illustrate the benefits of micromachining in reducing power and providing discrete reconfiguration [45]. A Scanning Electron Micrograph (SEM) of the design is shown in Figure 4-2. Due to the absence of a symmetrical inductor in the 6HP PDK, two octagonal 8-turn 14 nH spiral inductors were used. The MEMS capacitor consisted of three parallel banks of interdigitated beams and was designed such that the oscillator would discretely hop between 1.2 and 2.1 GHz. Since this was a fixed oscil-

Table 4-1. Differences in implementation of designs across generations

Generation	Process	Implementation	Inductor	Probes / DC Connections
First	IBM's BiCMOS6HP 0.25 μm	Reconfigurable oscillator (only reconfiguration via MEMS capacitor; no analog tuning)	Single-ended, octagonal shaped spiral	GSG Probes for signal / Bondwires for DC connections
Second, Third	Jazz 0.35 μm SiGe60	Reconfigurable VCO (reconfiguration via MEMS capacitor and tuning via varactor)	Symmetric square shaped inductor, differentially excited	GSGSG Probes for signal / Eyepass probes for DC connections

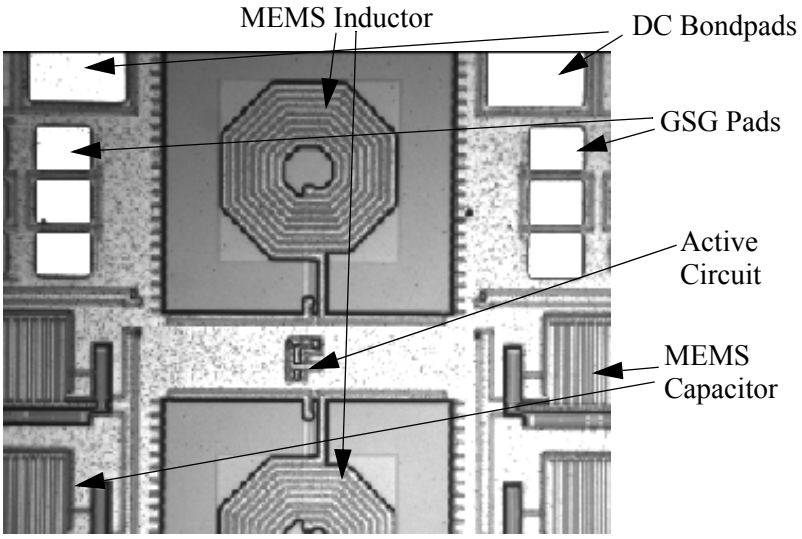
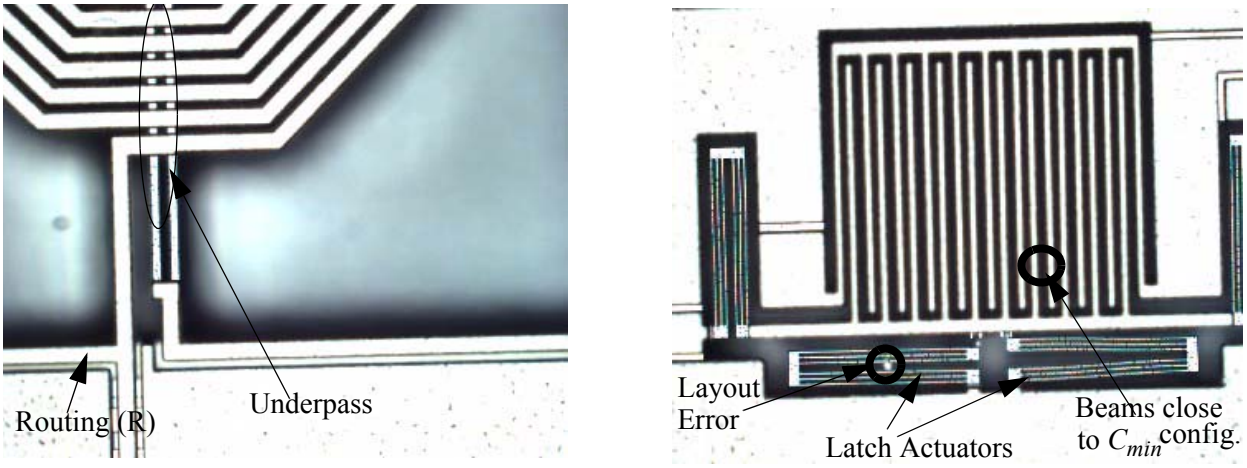


Figure 4-2. SEM of fixed oscillator

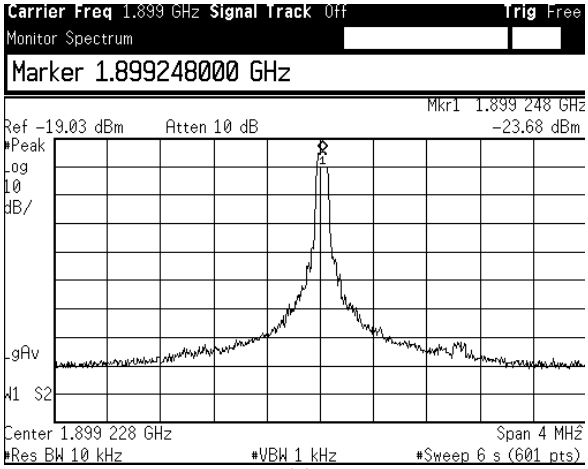
lator with no varactors, a long MOS tail current source was used, without worrying about AM-FM noise conversion, discussed in Chapter 2.

Some of the inductor layout issues can be pointed out from Figure 4-3 (a) The underpass was implemented as a stack of all metal layers except the topmost one, to reduce its resistance. It was divided into two, due to micromachining constraints, as there were concerns that the substrate below the 15 μm wide line would not be etched. Also, the routing, *R*, leading to the capacitor to the left was implemented at the edge, so that it would be micromachined (Effect C in Section 1.4). The active circuitry was placed 50 μm from the edge, to prevent damage from micromachining.

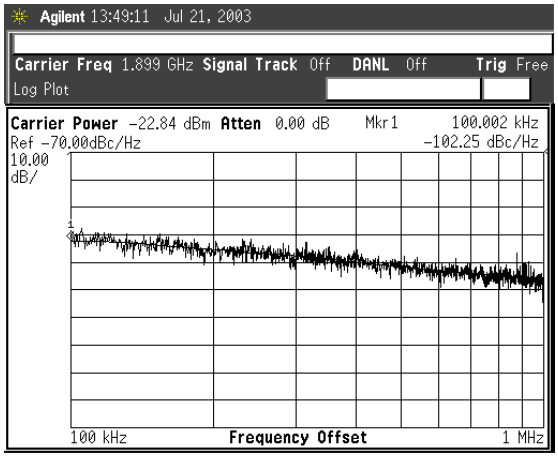


(a) (b)

Figure 4-3. Magnified SEMs of the MEMS inductor (a) and MEMS capacitor (b)



(a)



(b)

Figure 4-4. Oscillator Spectrum (a) and Phase Noise Plot (b)

As seen in Figure 4-3 (b), due to a layout error, one of the latch actuators did not work. Also due to processing issues, one of the three banks in each capacitor did not release. Due to this, there was not much change in the capacitance value from one configuration to another and hence discrete reconfiguration was not observed. The center frequency obtained was 1.9 GHz, close to the maximum design frequency of 2.1 GHz. This is due to the fact that the beams are close to being in the minimum capacitance configuration, as seen from Figure 4-3 (b), The observed spectrum and phase noise plots are shown in Figure 4-4 (a) and (b) respectively. The phase noise at 1 MHz offset from the carrier was -116 dBc/Hz, with a core power consumption of 1.35mW.

The value of the capacitance needed for 1.9 GHz with a 14 nH inductor is 0.5 pF. As pointed out in Chapter 2, this causes a 'flattening' of the close-in phase noise spectrum as can be observed in Figure 4-5. The flattening is observed till a frequency of 10 kHz, after which the plot begins to approach the expected -20 dB/decade roll off. The value of phase noise considered for comparison purposes is more than a decade after the flattening region to ensure that there is no 'seemingly improved' phase noise performance due to the flattened region.

4.2 Second Generation Designs

All designs hereafter were fabricated in the Jazz 0.35 μm 4-metal layer SiGe process. This process also has a top-most thick metal layer for inductors. In addition, since this PDK provides a symmetrically laid out square-shaped inductor, symmetrical inductors have been used in all the designs in contrast to the pair of single-ended spiral inductors used in the first generation design. As mentioned in Table 4-1, varactor diodes have been used for fine tuning across the discrete hops. Since the goal of these designs was to demonstrate digital reconfiguration rather than analog tuning, the smallest varactor available in the PDK was chosen. This provided a variable capacitance between 80 fF and 120 fF. The active circuitry included a SiGe BJT tail current source due to the presence of the non-linear varactor. Two second generation VCOs were designed.

4.2.1 Beam-based MEMS Capacitor VCO Design

The first of the two second generation VCOs uses beam-based reconfigurable MEMS capacitors [35] (Figure 4-6). The two targeted frequencies of operation in this design were 1.8 GHz and 3.2 GHz. Fixed capacitance parasitics were estimated to be 225 fF. The MEMS capacitor was designed to have a C_{min} of 0.18 pF and C_{max} of 1 pF. The varactor diodes lead to a 200 MHz fine tuning range at f_{max} and 100 MHz at f_{min}.

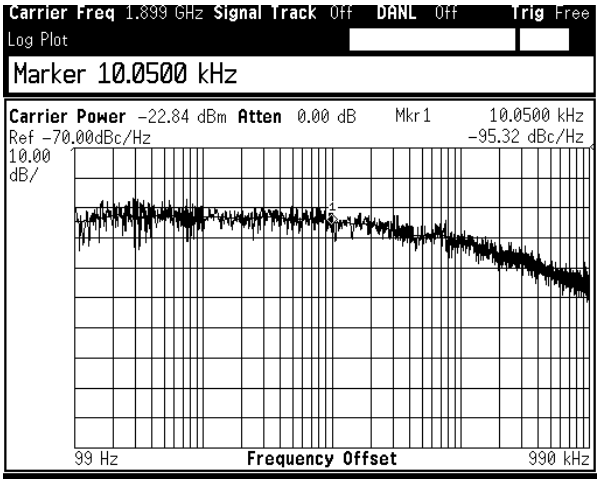


Figure 4-5. Flattening of the close-in phase noise spectrum

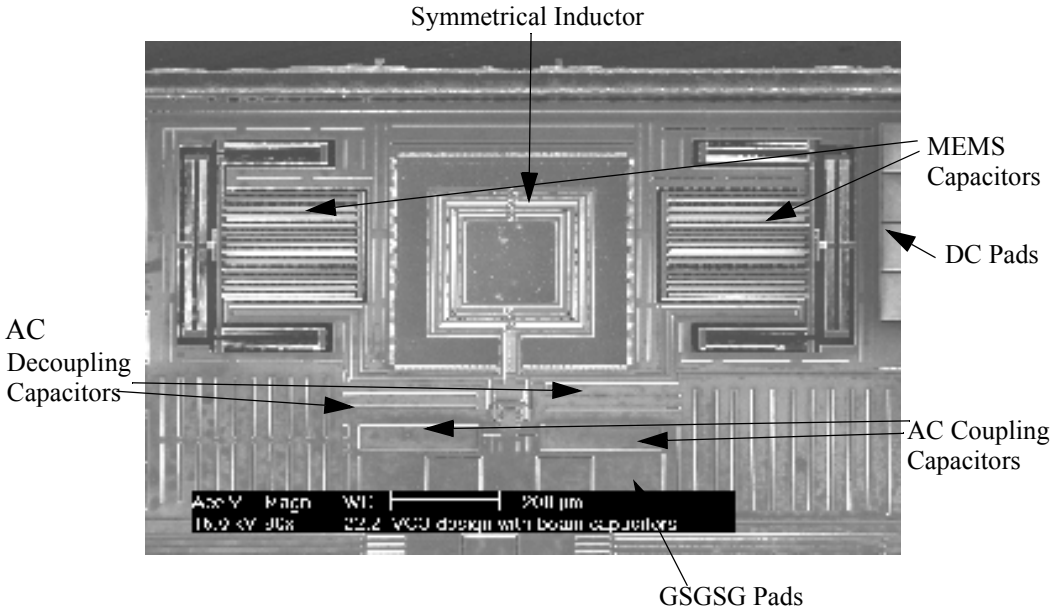
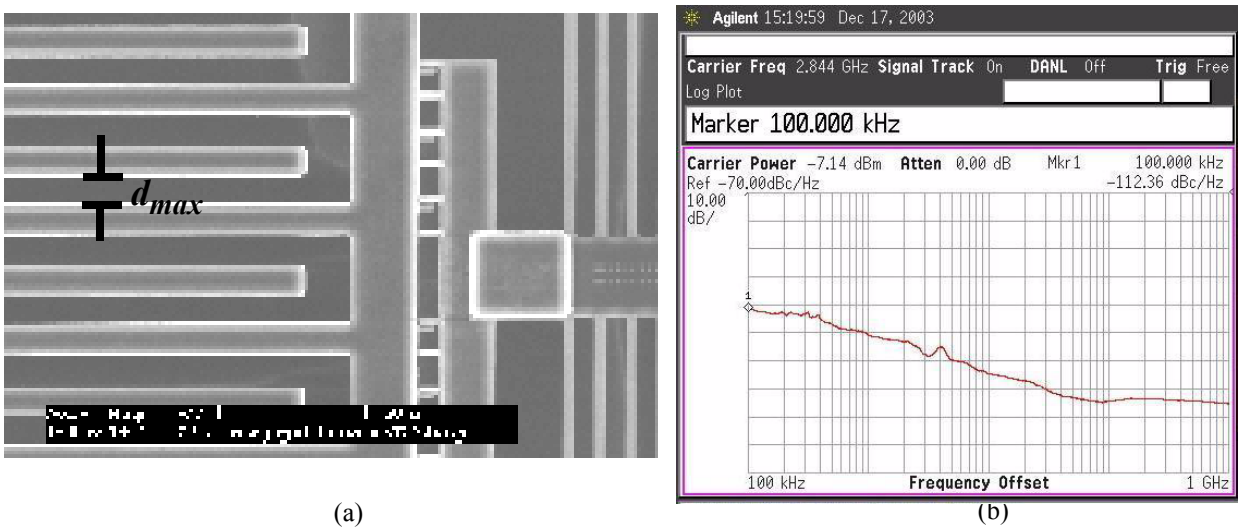


Figure 4-6. SEM of Beam Design VCO
The DC connections for the capacitor are shown to the right. The DC connections for the VCO (not shown in the figure) are to the left. The GSGSG pads are right below the active circuitry. The AC coupling capacitors are integrated on-chip, to fill in the space, right next to the output buffers, and right above the GSGSG pads.

The measured carrier frequencies obtained as a result of discrete reconfiguration were 2.75 GHz (C_{min} configuration) and 2.15 GHz (C_{max} configuration) which are in-between the designed frequencies of 3.2 GHz and 1.8 GHz. Along with analog tuning, the minimum and maximum frequencies obtained were 2.1 GHz and 2.8 GHz respectively, resulting in a tuning range of 30 % for a center frequency of 2.45 GHz. To maintain the same carrier power (-4 dBm) and phase noise (-122 dBc/Hz @ 1MHz), core power consumption is higher for the C_{max} configuration, because of the increased tank capacitance. For the same voltage swing, more current would be needed since $I = (j\omega C)V$ .It should be noted that though ω does decrease, it is only proportional to the square root of C, while I has a linear relationship with C.

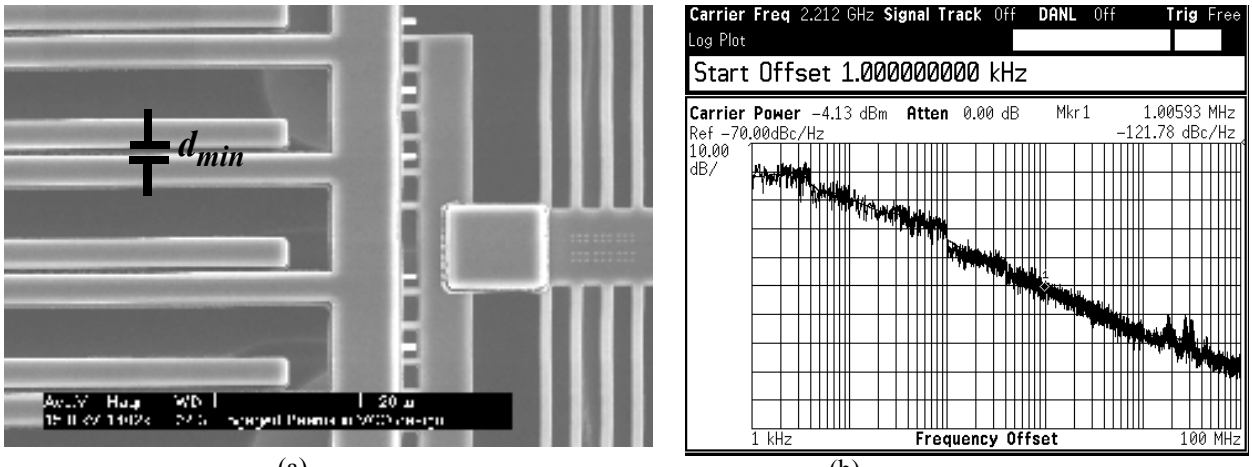
Figure 4-7 (a) shows the MEMS capacitor in the C_{max} configuration. The distance between the beams, d_{min} is minimum achievable with this design. Figure 4-7 (b) shows the phase noise plot. It can be seen that the phase noise spectrum flattens out at 3 kHz. Compared to the first generation design, this is 3 times lower, the difference largely contributed by the doubling of the capacitance in this design configuration



(a) (b)

Figure 4-8. SEMs of MEMS capacitor in C_{min} configuration (a) Phase Noise Plot (b)

Figure 4-8 (a) shows the MEMS capacitor in the C_{min} configuration, with maximum distance, d_{max}, possible between the beams. Figure 4-8 (b) shows the phase noise plot. The phase noise spectrum flattening is now observed to be at a frequency slightly less than 100 kHz, more than an order of magnitude higher than that for the C_{max} configuration. There are two reasons contributing this large degradation. First is the fact that $C_{min} = C_{max} / 2 = 0.5$ pF (measured capacitances in the tank), and hence the diffusion constant, D is higher. The second reason is that D is also proportional to the center frequency (2.14), which is higher in this case.



(a) (b)

Figure 4-7. SEMs of MEMS capacitor in C_{max} configuration (a) Phase Noise Plot (b)

Table 4-2. Benefit of micromachining in increasing tank Q

	Carrier Frequency (GHz)	PN @ 1 MHz offset (dBc/Hz)	Power dissipated (mW)
Before Release	1.6	-106	2.75
After Release	2.8	-122	2.75

There are two ways to show the benefit of micromachining in increasing the tank *Q*. The improvement of *Q* due to micromachining can be demonstrated from the minimum bias current required to start oscillations. Only 125 μA was needed for the oscillator after release, compared to 520 μA for the same oscillator before micromachining. The improvement of tank *Q* can also be demonstrated by comparing measured phase noise for the same bias current. Table 4-2 shows that micromachining improves the phase noise by 16 dBc/Hz for the same power dissipated.

4.2.2 Finger-based MEMS Capacitor VCO Design

The finger-based designs of the MEMS capacitor are implemented to further extend the tuning range [35]. A SEM of the VCO is shown in Figure 4-9. The inductor used is a 2 nH symmetrical one. The

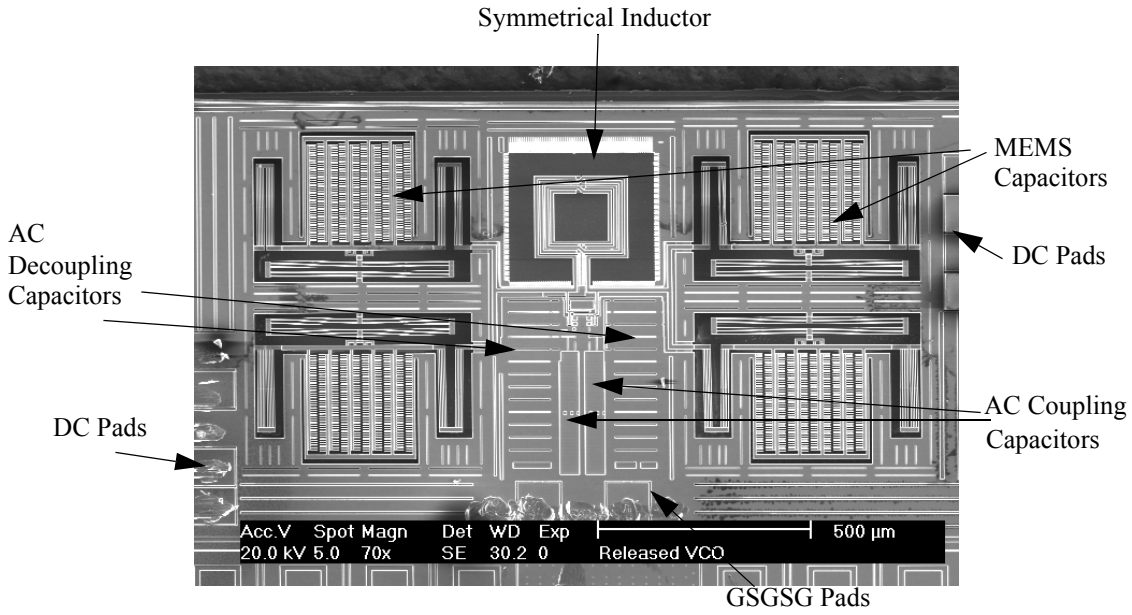


Figure 4-9. SEM of Finger-based Capacitor Design VCO
The DC connections for the capacitor are to the right and the VCO are to the left. The GSGSG pads are some distance below the active circuitry interfaced by the AC coupling capacitors. Due to a large amount of fill-in space available on this chip, large AC decoupling capacitors were included to provide a low impedance path for any RF signal on the DC lines to ground.

reason why a smaller inductor was chosen in this design was because of the targeted frequency hop from 2.4 - 5.2 GHz (IEEE 802.11 a & b standards). This ambitious hop would need a tuning range of almost 8:1 for the capacitors with a 2 nH inductor. This tuning range is achievable using CMOS-MEMS reconfigurable capacitors [35]. A bigger inductor, however, would have demanded more tuning range from the MEMS capacitors. A smaller inductor, on the other hand, would have forced C_{max} to be higher than what was possible to obtain from just 2 parallel banks of capacitances, the limit being set by post-foundry fabrication constraints. Adding an extra bank adds some fixed parasitic capacitances, thereby dropping tuning range. The capacitors were designed to be 0.24 pF in the C_{min} configuration and 2 pF in the C_{max} configuration. The small varactor was designed to provide a 300 MHz tuning range at f_{max} and 100 MHz at f_{min}.

Due to post-processing issues [35], the gaps between the fingers were covered with 300 nm of polymer, preventing the fingers from engaging. Hence, the hopping operation did not work as expected, and the two frequencies obtained were only 4 GHz and 3.56 GHz. This is because the tuning was obtained only from the truss beams, rather than the fingers, as designed.

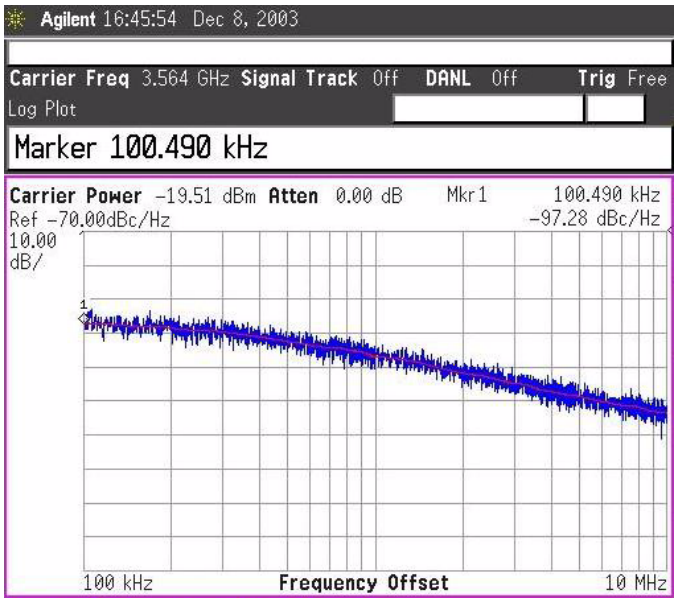


Figure 4-10. Phase noise plot of 3.56 GHz carrier

Figure 4-10 shows the phase noise plot at 3.56 GHz. The low *Q* of the capacitor [35] leads to a degraded phase noise performance of -105 dBc/Hz at @ 1 MHz offset from the 3.56 GHz carrier and -102 dBc/Hz @ 1MHz offset from the 4 GHz carrier. Besides, the power consumed in the two configurations was 5.75 mW. For a 2 nH inductor, for the frequencies obtained, the capacitances in the tank can be estimated as 1 pF and 0.8 pF respectively. Even though this capacitances in this design were not as low as the previous designs, the highly degraded *Q* and the higher frequencies led to an increased 'flattening frequency', as can be seen from Figure 4-10, where this frequency can be seen to be at 100 kHz, and the plot starts falling at the -20 dB/decade slope only after around 600 kHz.

4.3 Third Generation Designs

Due to smaller gaps in the second generation designs, the tuning range fell short to what was desired. Hence a VCO design was done, which incorporated larger gaps for the beams and the fingers. Also, although we did get low power operation, it was desired to achieve even lower power and higher frequency operation. For this purpose, a VCO was designed, which would only have fine tuning by varactor diode,

thereby consuming much less area due to the absence of the large micromachined reconfigurable capacitors. These two designs are yet to be tested and are described next.

4.3.1 Larger gap MEMS Capacitor VCO Design

To counter the formation of the polymer layer on the side-walls, as mentioned in Section 4.2.2, the gaps between the fingers as well as the beams were increased. This would now allow the gaps to engage. The gaps between the beams in the beam design VCO (Section 4.2.1) were increased from $3\mu m$ and $7\mu m$ to $5\mu m$ and $9\mu m$. The gaps between the fingers in the finger design VCO (Section 4.2.2) were increased from $3.8\mu m$ to $5.6\mu m$. This design is expected to have a higher tuning range than the previous design.

4.3.2 Non-reconfigurable VCO Design

This design was made with the goal of demonstrating low power operation at a high frequency, to get a good Figure of Merit (to be discussed in the next chapter). For high FoM, phase noise, hence tank Q is paramount. We eliminated the MEMS capacitor in favour of a fixed MIM capacitor and the same small varactor as used in the second generation designs. Additionally, this design has the advantage of reduced area (0.75 mm X 0.65 mm).

Figure 4-11 shows the layout of the design. Since the goal of this design was to get the best performance at the highest frequency possible, the design approach was to first plot the *Q*'s of different value of inductors across frequency. The values of *Q* in the region in which *Q* is proportional to frequency ($\left(Q = \frac{\omega L}{R_s}\right)$, were seen to be higher for increasing *L* till *L* = 5 nH. Since, high frequency was targeted, effort was made to reduce *C* in the tank for the chosen value of *L*. This meant that the varactor now formed a significant portion of the *C* in the tank, and its *Q* would dominate the *Q* of the capacitive part of the tank significantly (3.12). Hence, the frequency of operation was chosen at the point where the tank *Q*, as given by (3.5) was maximum.

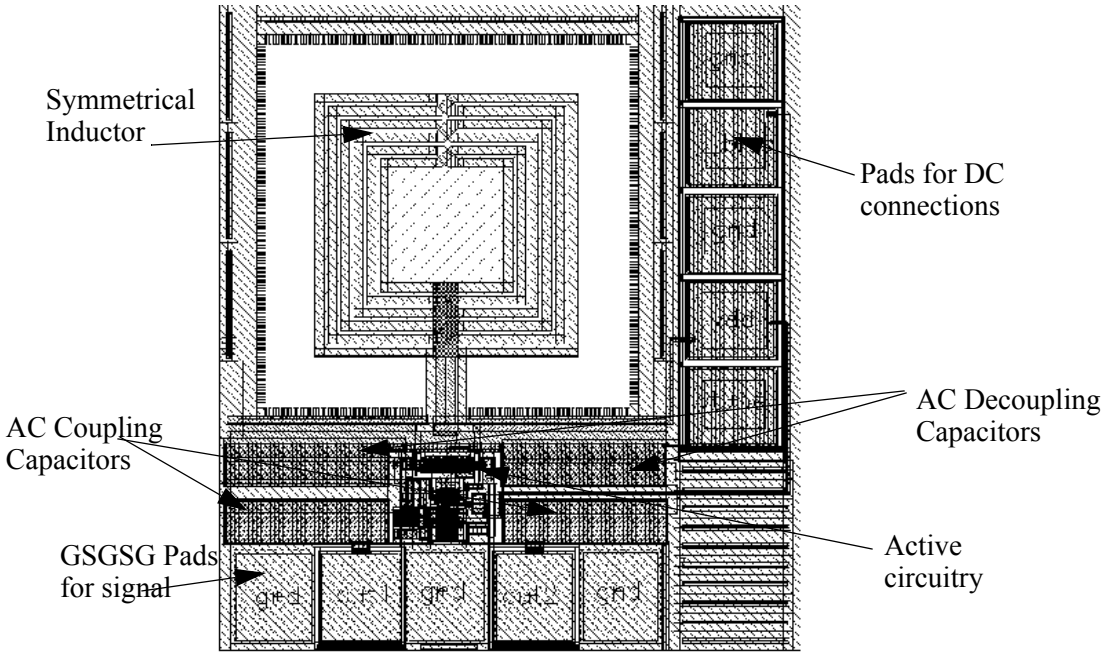


Figure 4-11. Layout of the non-reconfigurable VCO

Since the simulated tank Q (15) was high, R_p was high. Hence the voltage swing across the tank was high, since $V_{swing}=I_{bias}*R_p$. To prevent forward biasing of the C-B junction of the cross-coupled pair, a small C_{div1} (25 fF) was chosen, so that the base would swing much less than the collector. To get the desired frequency, some fixed capacitance had to be added in parallel to the varactor. This was realized in the form of a Metal-Insulator-Metal (MIM) capacitor of 0.16 pF. Combined with routing parasitic capacitances, the total C in the tank was 0.3 pF, which resulted in a frequency of 4.1 GHz.

5 Discussion and Conclusions

5.1 Comparisons with previously published work

The common merit of performance of a VCO is phase noise. However, since this work has focused on low power and high tuning range, it is required to compare its performance with others on a different figure of merit, which also considers these issues. While there is no commonly accepted merit which includes tuning range, there does exist a Figure of Merit (FoM) [46], which takes into consideration power consumption and is defined by

$$FoM = 10log\left(\left(\frac{f_o}{\Delta f}\right)^2 \times \frac{1}{L\{\Delta f\}P}\right) \tag{5.1}$$

where f_o is the carrier frequency, Δf is the offset from f_o, $L\{\Delta f\}$ is the phase noise at that offset and P is the power consumed in the core in mW.

Table 5-1 shows the comparison between this work and recent VCO publications that have used either a MEMS C or a MEMS L. This is the first integration of a MEMS C with a MEMS L. [48] achieves

Table 5-1. Comparisons with MEMS VCOs

	This Work (Section 4.2.1)	Dec *et. al.* MTT 2000 [47]	Park *et. al.* MTT 2003 [48]
f_o (GHz)	2.84	2.4	5
L (dBc/Hz)	-122	-122	-122
P (mW)	2.75	13.5	3.75
FoM (dB)	187	178	190
Inductance (nH)	6.25	2.8	1
Capacitance (pF)	0.5	1.4	1
Idea	MEMS L & C	MEMS C	MEMS L

a better FoM than this work, but requires additional masking steps. Besides, with applications moving towards higher frequencies, there will come a time when the required inductance will be so small, that implementing the inductor on top will not be feasible.

Since there is a trend towards higher frequency RF communications, comparisons are made with integrated VCOs operating above 2 GHz in Figure 5-1. It can be seen that the FoM of this work outperforms all designs except [48] [49] [50] [51]. [50] [51] use bond wire inductors. Among the problems associated with bondwire inductors including reliability, controllability and consistency, the most critical is the pad parasitic capacitance. This limits the minimum capacitance in the tank, thereby severely reducing tuning range. Also the inductor size is limited by chip and package dimensions which can be a handicap to choosing bigger value inductors. One the other hand, micromachined inductors have no such issues involved and bigger inductors can be used without worrying about high frequency degradation due to substrate coupling

[48] uses an additional mask to implement the inductor. With cost driving most wireless applications today, the additional cost of a mask is not favourable. In contrast, the processing used in this work does

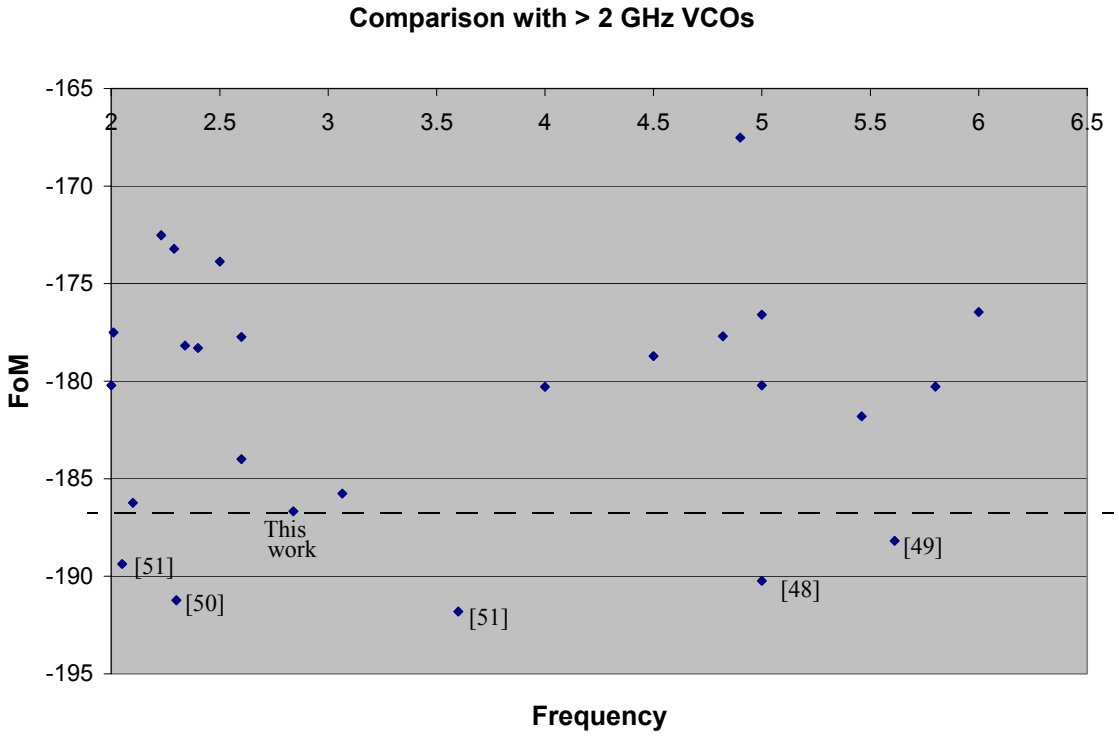


Figure 5-1. Comparisons with integrated VCOs operating above 2 GHz

Paper	Carrier Freq GHz	PN dBc/Hz	Offset Hz	Power mW	PN (dBc/Hz) @1MHz offset	FOM
Shin, RFIC 2002, pp 71	6	106	1000000	3.24	-106.00	-176.46
Bhattacharjee, RFIC, 2002, pp475	5.8	112	1000000	5	-112.00	-180.28
Fong, JSSC, Aug 2003, pp1333	5.612	113.2	1000000	1	-113.20	-188.18
Jacquinot, ESSIRC,2000	5.46	101	100000	24.8	-121.00	-181.80
Plouchart, RFIC, 2000 pp 57	5	98	100000	15	-118.00	-180.22
Park, MTT, Jan 2003	5	122	1000000	3.75	-122.00	-190.24
Samori, CICC, 2001, pp201	5	94	100000	13.75	-114.00	-176.60
ven de Ven, VLSI '01	4.9	113	2000000	21.2	-106.98	-167.52
Jacquinot, ESSIRC,2000	4.82	98.5	100000	27.9	-118.50	-177.70
Margarit, JSSC, July 2003, pp1284	4.5	119	1000000	21.6	-119.00	-178.72
Maget, JSSC, July 2002, pp953	4	117	1000000	7.5	-117.00	-180.29
Kucera, ESSCIRC, 2001	3.6	145	3000000	30	-135.46	-191.81
Fong, JSSC, Aug 2003, pp1333	3.065	120.8	1000000	3	-120.80	-185.76
CMU	***2.84***	***122***	***1000000***	***2.75***	***-122.00***	***-186.67***
Park, MTT, Jan 2003	2.6	117	300000	15	-127.46	-184.00
Ham, JSSC 2001	2.6	115	600000	10	-119.44	-177.74
Sanduleanu, ESSCIRC, 2002	2.5	128	3000000	18	-118.46	-173.86
Dec, MTTS, Nov.2000, pp1943	2.4	122	1000000	13.5	-122.00	-178.30
Wu, VLSI Symp '03	2.34	101	100000	10.5	-121.00	-178.17
Svelto, CICC, 2000, pp 577	2.3	107	100000	2	-127.00	-191.22
Stadius, MTTS, 2002	2.29	80	10000	25	-120.00	-173.22
Stadius, MTTS, 2002	2.23	81	10000	35	-121.00	-172.53
Svelto, CICC, 2000, pp 577	2.1	102.8	100000	2	-122.80	-186.23
Kucera, ISSCC, 2001, pp 374	2.05	114	100000	12.2	-134.00	-189.37
Ham, JSSC 2001	2.01	117	600000	10	-121.44	-177.50
De Mueur, JSSC, 2000	2	125.1	600000	34.2	-129.54	-180.22

Figure 5-2. Summary of performance of VCOs operating above 2 GHz, sorted by oscillation frequency.

not require any additional masks. [49] uses partially depleted SOI technology to realize the design. While SOI is a promising technology, SOI has not yet been commercially successful due to inherent problems in material, process, device, and design. High series resistance associated with source-drain in SOI drastically reduces the output currents. The body is floating in SOI and results in floating body effects like kink in the I-V characteristics, low breakdown voltage and hysteresis. On the other hand, micromachining does not change the active silicon area, and hence the characteristics of the active devices remain the same as they would have been without micromachining. A summary of performance of all VCO's plotted in Figure 5-1 is shown in Figure 5-2

The benefit of using a parallel reconfigurable capacitor with the non-linear varactor can be seen in Table 5-2. [52] uses a series fixed capacitor to improve linearity, and hence phase noise, but at the expense of tuning range. [53] uses a parallel implementation similar to the one used in this work, but requires additional mixed-signal control. This work (beam capacitor VCO design) not only gets the highest tuning range,

Table 5-2. Comparisons with MEMS VCOs

	This Work (Section 4.2.1)	Tiebout [52]	Kral [53]
f_o (GHz)	2.84	1.8	1.7
L (dBc/Hz)	-122	-130	-122
P (mW)	2.75	20	24
Tuning Range (%)	30	16	26
Idea	Parallel, no mixed-signal control	Series	Parallel, mixed-signal control

but also has the additional advantage of consuming an order of magnitude less power than the compared designs.

5.2 Conclusions

In summary, post-foundry micromachining of integrated RF passives was used to reduce loss. Integration with a cross-coupled pair led to low power and a wide tuning range VCO operation. The resulting FoM is better than all previous VCOs based on micromachining. The design uses a magnitude of less power than other VCOs at similar operating frequencies. The use of micromachining is particularly promising for low power operation at high frequencies as its enhancement of inductor Q increases with frequency, particularly since the quality factors of conventionally implemented passives is limited by both substrate loss and self-resonance at these frequencies. Also micromachining enables discrete reconfiguration, which is essential to extend the tuning range without stressing the continuous tuning varactor.

Bibliography

[1] V. K. Saraf, D. Ramachandran, A. Oz, G. K. Fedder, T. Mukherjee, "Low-Power LC-VCO using integrated MEMS passives," *RFIC 2004*, Fort Worth, TX, June 6-8, 2004.

[2] D. Ramachandran, A. Oz, V. K. Saraf, G. K. Fedder and T. Mukherjee, "MEMS-enabled Reconfigurable VCO and RF Filter," *RFIC 2004*, Fort Worth, TX, June 6-8, 2004.

[3] A. Oz, G. K. Fedder, "CMOS-Compatible RF-MEMS Tunable Capacitors," *2003 IEEE Int. RFIC Symp.*, pp. 611-614.

[4] G. K. Fedder, S. Santhanam, M. L. Reed, S. C. Eagle, D. F. Guillou, M. S.-C. Lu, and L. R. Carley, "Laminated High-Aspect-Ratio Microstructures In A Conventional CMOS Process," *Sensors & Actuators*, pp. 103-110, March 1997.

[5] H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. R. Carley, G. K. Fedder, "Micromachined High-Q Inductors in 0.18 μm Cu Interconnect Low-K CMOS," *JSSC*, SC-37(3), Mar. 2002, pp. 394-403.

[6] Y.-C. Chang, A.A. Abidi, M. Gaitan, "Large suspended inductors on silicon and their use in a 2-μm CMOS RF amplifier," *IEEE Elec. Dev. Lett.*, Vol. 14 no. 5, pp. 246-248.

[7] H. Jiang, J.-L.A.Yeh, Y. Wang, and N. Tien, "Electromagnetically shielded high-Q CMOS-compatible copper inductors," *ISSCC Dig. Tech. Papers*, pp. 330-331, 2000.

[8] A.Dec, K. Suyama, "A 1.9-GHz CMOS VCO with micromachined electromechanically tunable capacitors, *JSSC*, SC-35(8), Aug. 2000, pp. 1231-1237.

[9] A. Hajimiri, T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *JSSC*, SC-33(2), Feb. 1998, pp. 179-194.

[10] B. Razavi, *RF Microelectronics*. New Jersey: Prentice Hall PTR, 1997

[11] H. Darabi, A. A. Abidi, "Noise in RF-CMOS Mixers: A Simple Physical Model," *IEEE Transactions on Solid State Circuits*, Vol. 35, No. 1, Jan. 2000, pp. 15-25.

[12] J. J. Rael, A. A. Abidi, "Physical Processes of Phase Noise in Differential LC Oscillators," *2000 IEEE Custom Integrated Circuits Conference*, pp. 569-572.

[13] E. Hegazi, H. Sjoland, A. A. Abidi, "A Filtering Technique to Lower LC Oscillator Phase Noise," *JSSC*, SC-36(12), Dec. 2001, pp. 1921-1930.

[14] A. Ismail, A. A. Abidi, "CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise," *ISSCC Dig. Tech. Papers*, pp.98-99, 2003.

[15] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proc. IEEE*, 54(2), pp. 329-330, 1966.

[16] D. Scherer, "Design principles and measurements of low phase noise rf and microwave sources," presented at Hewlett Packard RF and Microwave Measurement Symp., Apr. 1979.

[17] A. A. Adronov, A. A. Vitt, S. E. Khaikin, *Theory of Oscillators*. New York: Pergamon, 1966.

[18] D. Ham, A. Hajimiri, "Virtual Damping and Einstein Relation in Oscillators," *JSSC*, SC-38(3), Mar. 2003, pp. 407-418.

[19] F. Reif, *Fundamentals of Statistical and Thermal Physics*. New York: McGraw-Hill, 1985.

[20] N. G. V. Kampen, *Stochastic Processes in Physics and Chemistry.* Amsterdam, The Netherlands: North-Holland, 1992.

[21] A. Einstein, *Investigation on the Theory of Brownian Motion*, Dover Publication, 1956.

[22] D. Ham and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," *JSSC*, SC-36(6), June 2001, pp. 896-909.

[23] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y.-C. Sun, B. S. Meyerson, T. Tice, "Si/SiGe Epitaxial-Base Transistors - Part I: Materials, Physics and Circuits," *IEEE Transactions on Electron Devices,* Vol. 42, No. 3, March 1995, pp. 455-468

[24] G. Niu, Z. Jin, J. D. Cressler, R. Rapeta, A. J . Joseph, D. Harame, "Transistor Noise in SiGe HBT RF Technology," *JSSC*, SC-36(9), Sep. 2001, pp. 1424-1428.

[25] C. P. Yue, S. S. Wong, "Physical modeling of Spiral Inductors on Silicon," *IEEE Transactions on Electron Devices,* Vol. 47, No. 3, March 2000, pp. 560-568.

[26] S. S. Mohan, "Modeling, Design and Optimization of On-Chip Inductors and Transformers," Ph.D. thesis, Stanford University, 1999.

[27] H.-S. Tsai, J. Lin, R. C. Frye, K. L Tai, M. Y. Lau, D. Kossives, F. Hrycenko, Y.-K. Chen, "Investigation of current crowding effect on spiral inductors," Wireless Applications Digest, 1997, *IEEE MTT-S Symposium on Technologies*, Feb. 1997, pp. 139-142.

[28] W. B. Kuhn, N. M. Ibraim, “Analysis of Current Crowding Effects in Multiturn Spiral Inductors,” *Trans. MTT*, MTT-49(1), Jan. 2001, pp. 31-38

[29] W. B. Kuhn, X. He, M. Mojaraddi, “Modeling Spiral Inductors in SOS Processes,” IEEE Transactions on Electron Devices, accepted for future publication, Issue 99, 2004.

[30] C. P. Yue, S. S. Wong, “On-Chip Spiral Inductors with Patterned Ground Shields for Si-based RF IC’s,” *JSSC*, SC-33(5), May 1998, pp. 743-752.

[31] J. R. Long, “Monolithic Transformers for Silicon RF IC Design,” *JSSC*, SC-35(9), Sep. 2000, pp. 1368-1382.

[32] S. H. A. Wheeler, “Simple Inductance Formulas for Radio Coils,” *Proc. IRE*, v. 16, no. 10, October 1928, pp. 1398-1400.

[33] B. Baidya, K. He and T. Mukherjee, “Layout Verification and Correction of CMOS-MEMS Layouts,” in *Technical Proceedings of the Fourth International Conference on Modeling and Simulation of Microsystems (MSM '01)*, pp. 426-429, March 19-21, 2001, Hilton Head, SC, USA

[34] J. R. Long, M. A. Copeland, “The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC’s,” *JSSC*, SC-32(3), Mar. 1997, pp. 357-369.

[35] A. Oz, *CMOS/BICMOS Self-assembling and Electrothermal Microactuators for Tunable Capacitors*, MS Thesis, Carnegie Mellon University, 2003. (http://www.ece.cmu.edu/~mems/pubs/)

[36] M.Tiebout, “Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS,” *IEEE JSSC*, SC-36(7), pp. 1018-1024, July 2001.

[37] A. Kral, F. Behbahani, and A.A.Abidi, “RF-CMOS oscilltors with switched tuning,” in *Proc. IEEE Custom Integrated Circuits Conference*, Santa Clara, CA, 1998, pp. 555-558.

[38] E. Hegazi, A. A. Abidi, “Varactor Characteristics, Oscillator Tuning Curves and AM-FM Conversion,” *JSSC*, SC-38(6), June 2003, pp. 1033-1039.

[39] S. Levantino, C. Samori, A. Zanchi, A. L. Lacaita, “AM-to-PM Conversion in Varactor-Tuned Oscillators,” *IEEE Transactions on Circuits & Systems - II: Analog & Digital Signal Processing*, Vol. 9, No. 7, Jul 2002, pp. 509-512

[40] E. Pedersen, *RF CMOS Varactors for Wireless Applications,* Industrial Ph.D. Thesis, February 2001. (http://cpk.auc.dk/risc/theses/2001/pedersen.pdf)

[41] K. Stadius, K. Halonen, “Wide-tuning-range dual-VCOs for Cable Modem Receivers,” Microwave Symposium Digest, 2002, *IEEE MTT-S International,* June 2002, vol. 1, pp. 581-584.

[42] P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley & Sons, Inc., 2001.

[43] A. Hajimiri, T. H. Lee, “Design Issues in CMOS Differential LC Oscillators,” *JSSC*, SC-34(5), May 1999, pp. 717-724.

[44] A. Oz, D. Ramachandran, V. K. Saraf, M. Sperling, G. K. Fedder, T. Mukherjee, “Toward a wide-band frequency hopping RF MEMS receiver”, *2003 SRC Design Challenge: Team 29 Phase 2 Final Report,* July, 2003.

[45] A. Oz, V. K. Saraf, D. P. Ramachandran, G. K. Fedder and T. Mukherjee, “Frequency Hopping Circuits based on Reconfigurable MEMS Capacitors”, *TECHON 2003*, Dallas, TX, August, 2003.

[46] P. Kinget, “Integrated GHz voltage controlled oscillators,” in *Analog Circuit Design: (X)DSL and Other Communication Systems; RF MOST Models; Integrated Filters and Oscillators*, W. Sansen, J. Huijsing, and R. van de Plassche, eds. Boston, MA: Kluwer, 1999, pp. 353-381.

[47] A.Dec, K. Suyama, “Microwave MEMS-based voltage controlled oscillators,,” *Trans. MTT*, MTT-48(11), Nov. 2000, pp. 1943-1949

[48] E.-C. Park, Y.-S. Choi, J.-B. Yoon, S. Hong and E. Yoon, “Fully integrated low phase-noise VCOs with on-chip MEMS inductors,” *Trans. MTT*, MTT-51(1), Jan. 2003, pp. 289-296.

[49] N. H. W. Fong, J.-O. Plouchart, N. Zamdmer, D. Liu, L. F. Wagner, C. Plett, N. G. Tarr, “Design of a Wide-band CMOS VCO for Multiband Wireless LAN Applications,” *JSSC*, SC-38(8), Aug. 2003, pp. 1333-1342.

[50] F. Svelto, S. Deantoni, R. Castello, “A 1 mA, -120.5 dbc/Hz at 600 kHz from 1.9 GHz fully tuneable LC CMOS VCO,” *2000 IEEE Custom Integrated Circuits Conference*, pp. 577-580.

[51] J. J. Kucera, “Wideband BiCMOS VCO for GSM/UMTS Direct Conversion Receivers,” *ISSCC Dig. Tech. Papers*, pp. 374-376, 2001.

[52] M.Tiebout, “Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS,” *IEEE JSSC*, SC-36(7), pp. 1018-1024, July 2001

[53] A. Kral, F. Behbahani, and A.A.Abidi, “RF-CMOS oscilltors with switched tuning,” in *Proc. IEEE Custom Integrated Circuits Conf.*, Santa Clara, CA, 1998, pp. 555-558.