Design and Characterization of a RF Frequency-Hopping Filter

by

Deepa Parvathy Ramachandran

A thesis submitted in partial fulfillment of the requirements for the

degree of

Master of Science

in

Electrical and Computer Engineering

at

Carnegie Mellon University

Department of Electrical and Computer Engineering

Carnegie Mellon University

5000 Forbes Ave, Pittsburgh PA

Advisor: Dr. Tamal Mukherjee

Second Reader: Dr. Larry Pileggi

August 2004

Abstract

Integrated RF filters in future radio applications are expected to be reconfigurable to support multifunction radio capabilities and low power for mobile applications. The incorporation of MEMS passives in integrated RF filters can help achieve these goals. MEMS capacitors can switch between a minimum and maximum capacitance value, giving reconfigurable capability to an LC-filter. Micromachining inductors improves quality factor, potentially enabling integration of an all-passive LC-filter with zero power consumption.

Several designs of a passive, RF, reconfigurable filter topology have been explored. The LC-filter topology is a π-network. The filters have been designed, simulated, fabricated, and tested. A reconfiguration range as high as 850 MHz has been demonstrated. Inductors used in these designs have been characterized with test structure measurements, lumped parameter models, and fast method-of-moments solver models. Inductor characterization has provided insight into quality factor improvement due to micromachining and quality factor for various inductor geometries. This project serves as one of the first attempts at integrating several MEMS passives together to form an electronic circuit. Future directions in this work include new filter topologies, improved design choices based on passive characterization results and wider reconfigurable ranges.

Acknowledgements

Table of Contents

1 Introduction

Devices operating in the gigahertz range are playing an increasing role in communications technology. There is a high interest in RF circuits operating in the communications spectrum, particularly for portable personal communication devices. Since all these devices have to share the same spectrum, there is increased desire for the devices to switch between operating frequencies to enable co-existence. Additionally, implementing the RF circuitry on chip can reduce overall power consumption and size. In transceiver technology, the level of circuit integration in the RF side is still challenged by issues of reconfiguration, power dissipation, quality factor, and cost [1][2][3].

These challenges can be addressed by integrating micromachined passives. Micromachining enables movable electrodes that can be used for variable capacitors and RF switches. By designing the range of the motion, capacitors that can vary over a wide range are possible [4][5]. Such variable MEMS capacitors allow for multi-frequency operation, or reconfiguration. Micromachining also improves inductor quality factor, or Q, thereby reducing the energy loss, and thus reducing power dissipation [6][7]. For example, prior approaches to integrating an inductor for RF filters have focused on using active circuitry to boost Q [8][9]. However, this approach increases power consumption. In contrast, the approach used in this work increases passive Q thus requiring no additional power. With the combination of MEMS and electronics, it can be seen that on-chip receiver building-block circuits are possible [10][11][12].

In addition to the electrical elements, micromachining enables movable devices that store energy in the mechanical domain, and circuits like high-Q resonant filters and electromechanical mixers can be designed [13]. Combining these features enables an integrated, dual-hopping, wideband, receiver front-end

architecture. This architecture [14][15] has driven the reconfigurable RF filter design [10] reported here and other RF-MEMS circuits [11][12] developed at Carnegie Mellon University.

1.1 Dual-Hopping Wideband Receiver

An example wideband receiver front-end is shown in Figure 1-1. Passives in the front-end of a receiver are found in the bandpass filters (BPF), and in the voltage-controlled oscillator (VCO). Wide tuning range is desirable for these building blocks to be reconfigurable across a broad spectrum. In addition to reconfiguration, high quality factor is desired for low insertion loss and narrow-bandwidth filters. High quality factor also helps to lower the power consumption of the entire front-end.

Figure 1-2 shows the dual-hop architecture. The input spectrum at the antenna ranges from mega-hertz to gigahertz. A narrow band of this wide input spectrum is filtered by the bandpass filter, removing most distant interferers [16]. This band is amplified through the low-noise amplifier (LNA) before down-conversion through the mixer using the local oscillator signal from a wide-range synthesizer (VCO). The filter and synthesizer are controlled by the same voltage V_C and hop within the input band in unison. The reconfigurable VCO and filter hop covers the input spectrum and selects bands wider than the final, desired signal bandwidth and is therefore termed as the "coarse hop". The VCO hop-step is set by a consideration of both the minimum achievable bandwidth of the filter, and also the minimum VCO hop resolution achiev-
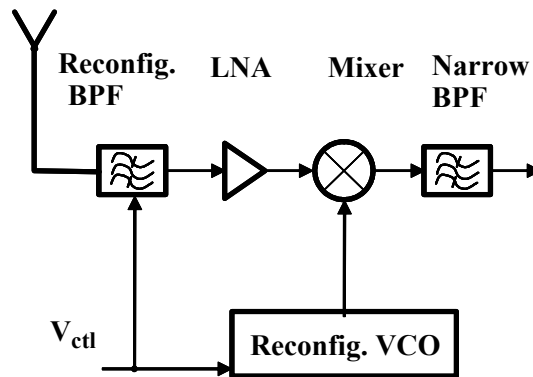
Figure 1-1 Wideband front-end architecture.

2
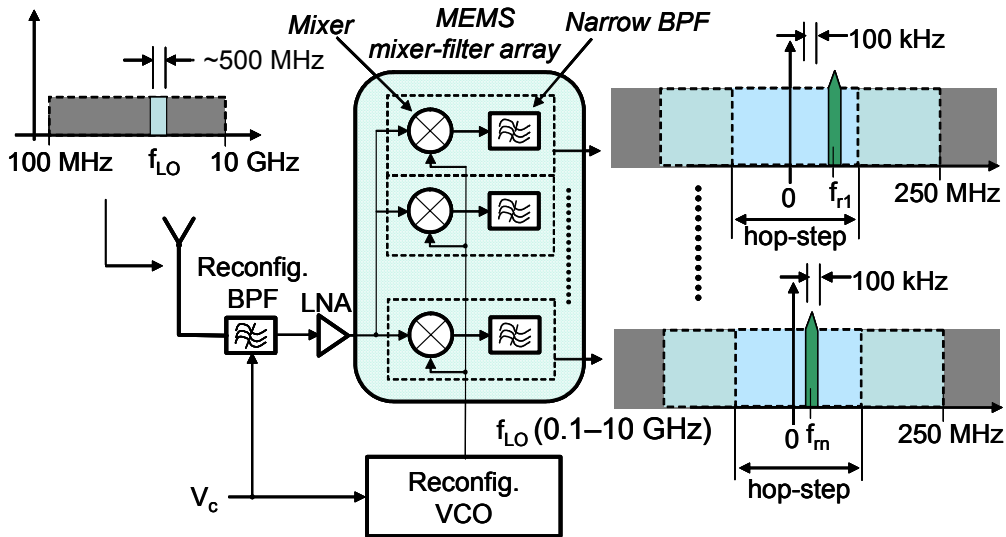
Figure 1-2 Dual-hopping wideband architecture. First-stage hop selects coarse band through coarse-hopping in filter and VCO. Second-stage hop selects signal band through fine-hopping in the MEMS mixer-filter array

able with low power. Due to the limitation on the minimum achievable hop-step, a second stage hop implemented using a mixer-filter array is required to select the signal band.

The mixer is implemented as a micromechanical resonator. MEMS resonators can perform both mixing and filtering. In the proposed design, a fine-hopping of about 100 kHz is set by the signal band. The mechanical resonance of the beam resonator performs the filtering operation, and can be designed to extract the 100-kHz signal band from the coarse band.

Since the mechanical mixer is small in area, fine-hopping is performed by designing an array of mixer-filters, each having a different mechanical resonance, to filter different 100-kHz signal bands. Fine-hopping is done by selecting between the outputs from the array. A dual-hop architecture is necessary to achieve the desired operation described — while coarse-hopping allows for coverage of a wide frequency spectrum, it is relatively slow. The electric switching between mixer outputs in fine-hopping is relatively fast (on the order of nanoseconds), and compensates for the relatively slow (on the order of milliseconds) coarse-hopping.

A key requirement for this on-chip architecture is low-power building-block RF circuits. Coarse-hopping, as described in the first-stage hop, requires circuit reconfiguration capabilities for the filter and VCO. This thesis focuses on the design of an all-passive, bandpass filter with MEMS-based reconfiguration.

1.2 Passive LC Filter

The bandpass filter in the integrated, front-end architecture can be implemented as a passive LC-filter. Bandpass filters on the receiver end require high quality factor and low power dissipation. This is commonly achievable only through external filters with high-Q passives [1][2][3][17]. Performance of on-chip filters is primarily limited by low quality factor of inductors, which leads to high insertion loss, or poor power transfer [18]. Low inductor Q also limits the overall filter Q, challenging a desired, narrowband response. Although on-chip active filters with Q-enhancement allow for high-Q passives [8][9], additional input power for loss cancellation and for dynamic range is required. Noise figure due to use of active components also becomes a design challenge. An on-chip, passive filter solution with high quality factor passives, which consumes no power is therefore preferable.

Several techniques have been implemented to improve on-chip inductor quality factor [19][20]. Micromachining is one technique that allows for this [6]. Unlike some of the conventional techniques, which trade off Q for reduced frequency operation, micromachining improves both Q and offers higher frequency performance. Another advantage with micromachining is reconfigurable capability over a wide frequency range, due to the mechanical movement of released MEMS structures. MEMS capacitors [4] in an LC-filter achieve reconfiguration without additional power, and cover a wider frequency range than that achievable by CMOS varactors.

The passive LC filter design discussed serves as an unprecedented attempt at integrating several RF-MEMS capacitors with RF-MEMS inductors and analyzing the micromachining benefits of RF-MEMS integration in an electronic circuit.

In this thesis, Chapter 2 describes RF MEMS passives (inductors and capacitors) used in the filter topology. Chapter 3 focuses on the passive LC filter topology, offering a design methodology, and defining the performance specifications. Chapter 4 contains simulated and measured results of several inductor characterizations and filter implementations. Finally, Chapter 5 presents a conclusion and suggests directions for this future work.

2 RF MEMS Passives

There are two types of passive components used in the chosen filter topology: capacitors, and inductors. The primary characteristics required of these passives are minimal energy dissipation and functionality over a wide frequency range. In on-chip implementations of passives, sub-performance parameters are often negatively affected by parasitic elements. For example, for an inductor, a parasitic capacitor may limit the frequency range in which it behaves like an ideal inductor; or, a parasitic resistor may lead undesirable energy dissipation. Micromachining removes some parasitic sources that limit performance, allowing for better RF operation [21].

2.1 Micromachining

The micromachining process developed at Carnegie Mellon University is a maskless process [22]. The MEMS devices are fabricated out of the back-end-of-line metal-dielectric stack and are laid out alongside active electronics from the front end of line processing in the same foundry. The top metal layer acts as a mask both to define the regions with MEMS devices that require micromachining as well as to protect the active circuitry from micromachining. While this micromachining process does not provide the better transduction properties of silicon MEMS [23], the ability to exploit RF metallization in foundry processes and close proximity to transistor electronics leads to CMOS/BiCMOS-MEMS outperforming silicon MEMS for RF applications.

MEMS post-processing involves a series of two steps. First, starting out with a foundry chip (Figure 2-1a), any dielectric unprotected by metal is etched to the silicon substrate (Figure 2-1b). In the second step, a combined anisotropic and isotropic etch removes around 30 μm of the substrate beneath the
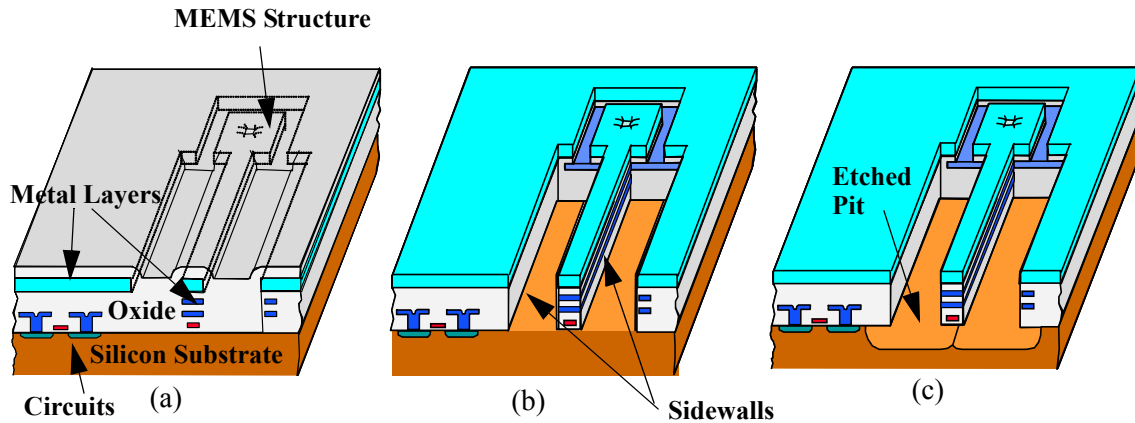
Figure 2-1. The micromachining process. a) Foundry chip containing active circuitry and metallization design required for intended MEMS device. b) Dielectric unprotected by metal is etched to the substrate. c) Substrate beneath the MEMS devices is etched.

MEMS structures for complete release of the devices (Figure 2-1c). We now consider the RF passive devices that can be fabricated using this process sequence.

2.2 MEMS Capacitor

Desired characteristics of an on-chip capacitor include high Q, wide tuning range with little or no mixed-signal control, and small area consumption. MEMS capacitors have better RF performance in tunability and Q, compared to other on-chip, variable capacitors, such as diode or accumulation region MOS varactors. Foundry MOS varactors with a nominal capacitance of about 500 fF tend to have a maximum to minimum capacitance ratio of 1:2.7. MEMS capacitors that vary as much as 1:3.52 have been demonstrated in the CMOS-MEMS process [4].

A 3-D cartoon of a MEMS capacitor design is shown in Figure 2-2. A capacitor can be made using two electrodes. The removal of the dielectric on the sides of a metal electrode (as in Figure 2-1b) and the silicon below the electrode (Figure 2-1c) allows it to move with respect to stationary metal electrodes on the chip, forming a variable capacitor. Capacitance can be changed by two types of electrode motion: varying the gap between the electrodes and varying the area between the electrodes. Additional capacitance comes

7
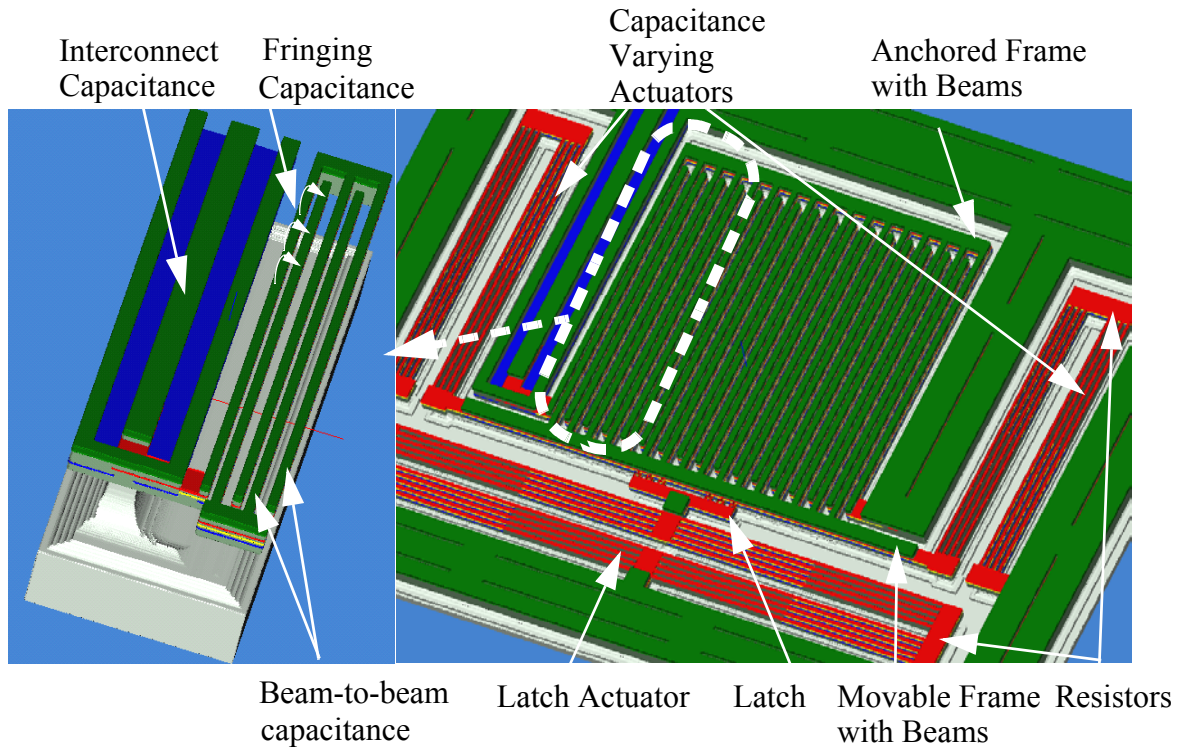
Figure 2-2. MEMULATOR drawing of gap-tuning, reconfigurable MEMS capacitor, showing layout, on right, and sources of capacitance, on left.

from fringing effects, one main source being the top and bottom of the beams to neighboring beams as shown in Figure 2-2. Also, the interconnect routing wires add some fixed parasitic capacitance to substrate.

The mechanical movement required for varying the gap or area is created using electrothermal actuators, shown in Figure 2-3. The top metal layer of an actuator defines the MEMS structure, as shown in Figure 2-3a. The lower metal layers are laterally offset as shown in the cross sections in Figure 2-3b. This offset causes a lateral stress gradient due to a difference in the temperature coefficients of expansion (TCE) of the dielectric and metal layers. The stress gradient causes an internal lateral bending moment that leads to actuator displacement. After microstructural release, an arch-like displacement is seen (Figure 2-3c). In this example, the laterally offset metallizations were designed for guided-end motion, or single-axis displacement [5]. Embedded within the actuator are polysilicon resistors which heat the actuator when voltage is applied, changing actuator displacement due to differences in the TCE of the metal and dielectric used to form the actuator. One end of the actuator is anchored, while the other end acts as a movable piston, that can

8
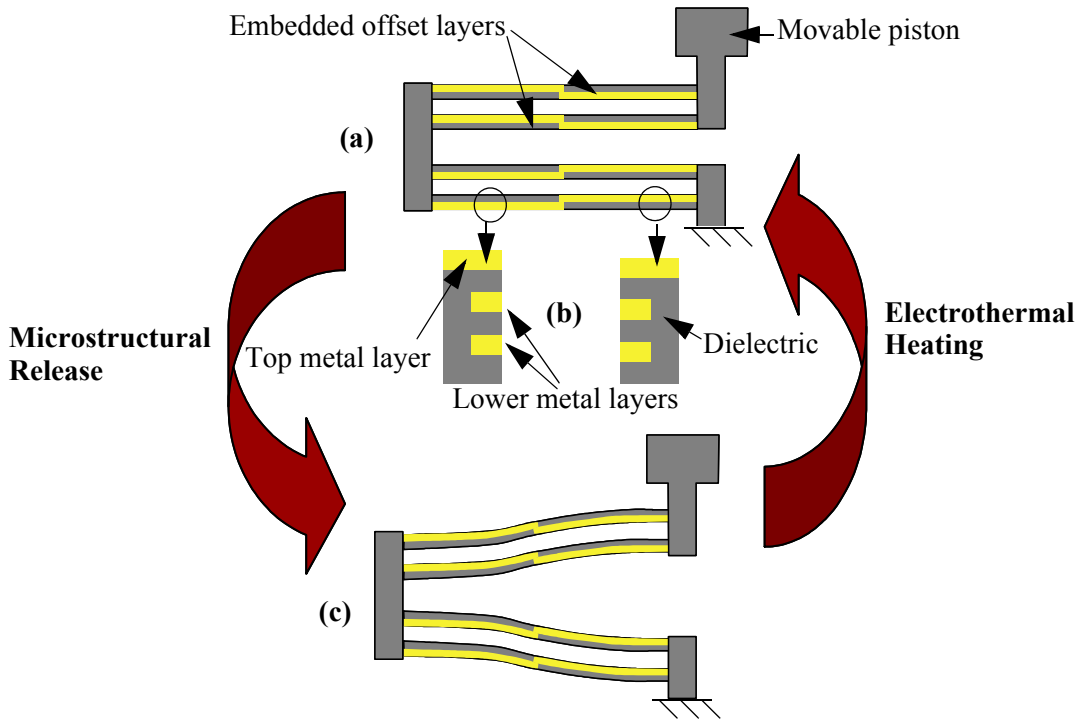
Figure 2-3. (a) Layout of an electrothermal actuator, with one end anchored and the other end intended for connection to the movable capacitor electrode. (b) Cross section showing lateral offset of lower metal layers to induce motion on release. (c) An arch-like displacement in the actuator due to lateral bending moment from the offset metal layers.

be used to mechanically move one or more electrodes. While power is needed to move the capacitor electrodes, zero standby power for capacitance operation is made possible by means of a latch mechanism. Capacitance variation can be made possible without any standby power required by means of a latch mechanism. The latch is designed to hold the capacitor electrodes in a specific configuration, providing a fixed value of capacitance. Designing multiple such configurations leads to operation as a reconfigurable MEMS capacitor without the need for mixed-signal control. Thus, this MEMS capacitor is reconfigurable between multiple fixed capacitance values with zero standby power.

2.2.1 Beam-Design Capacitor Characterization

The beam-design reconfigurable capacitor (Figure 2-4a) is composed of two frames with parallel, interdigitated beams that provide parallel-plate capacitance between sidewalls. One of the frames is movable, and variable capacitance is achieved through gap variation using the tuning actuator. This capacitor is
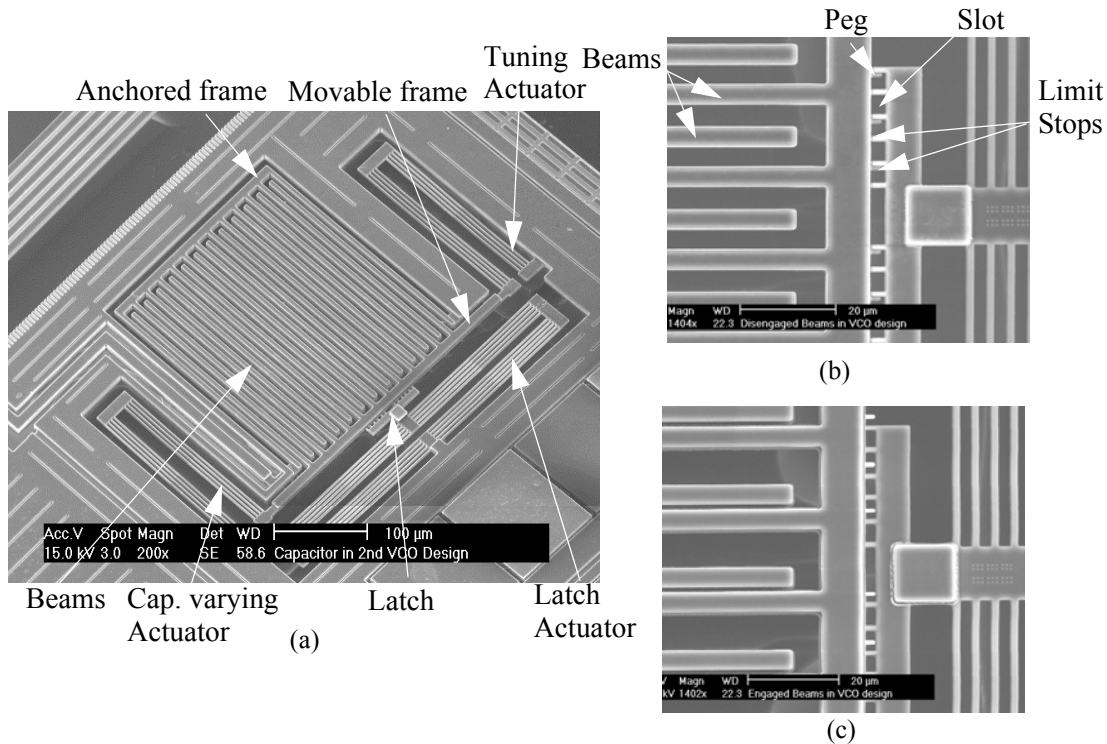
Figure 2-4. (a) SEM of reconfigurable beam-design MEMS capacitor. (b) Magnified view of latch at minimum capacitance state. (c) Magnified view of latch at maximum capacitance state.

reconfigurable between a minimum capacitance (Figure 2-4b) and a maximum capacitance (Figure 2-4c). The capacitor has a lateral latch, which operates with a peg-in-slot mechanism to hold the movable frame at a fixed position with respect to the anchored frame. In the minimum capacitance state, the pegs are held in the slots (limit stops), and the beams have maximum distance between them. After electrothermal actuation of the latch actuator, the slot is moved away from the pegs, and the frame is free to be moved to its new position. Electrothermal heating of the tuning actuator moves the frame to the maximum capacitance state (minimum distance between beams). The voltage heating the latch actuator is now removed, and it latches the peg in the slot again.

One beam-design capacitor (used in Design B filter in Chapter 4) had a measured tuning range of 1:2.17, from 400 fF to 866 fF. Quality factor for a typical MEMS capacitor (Figure 2-5) shows that Q's of 30-50 are achievable.
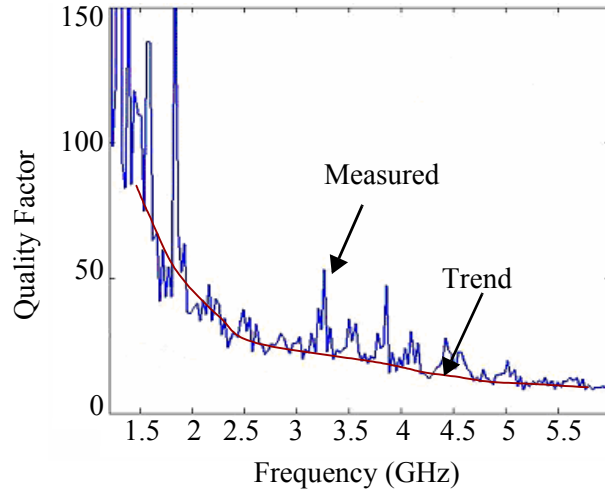
Figure 2-5. (a) Q vs. frequency for a beam-design capacitor, showing measured values and a trend curve.

2.2.2 Finger-Design Capacitor Characterization

The finger-design capacitor (Figure 2-6a) consists of a set of comb-like electrodes used for area tuning. For the minimum capacitance state (Figure 2-6b), the fingers are separated as far apart as possible with care to prevent the movable frame from getting too close to the fixed frame (as that leads to parasitic capacitance). In the maximum capacitance state, the fingers interleave with one another, and the movement
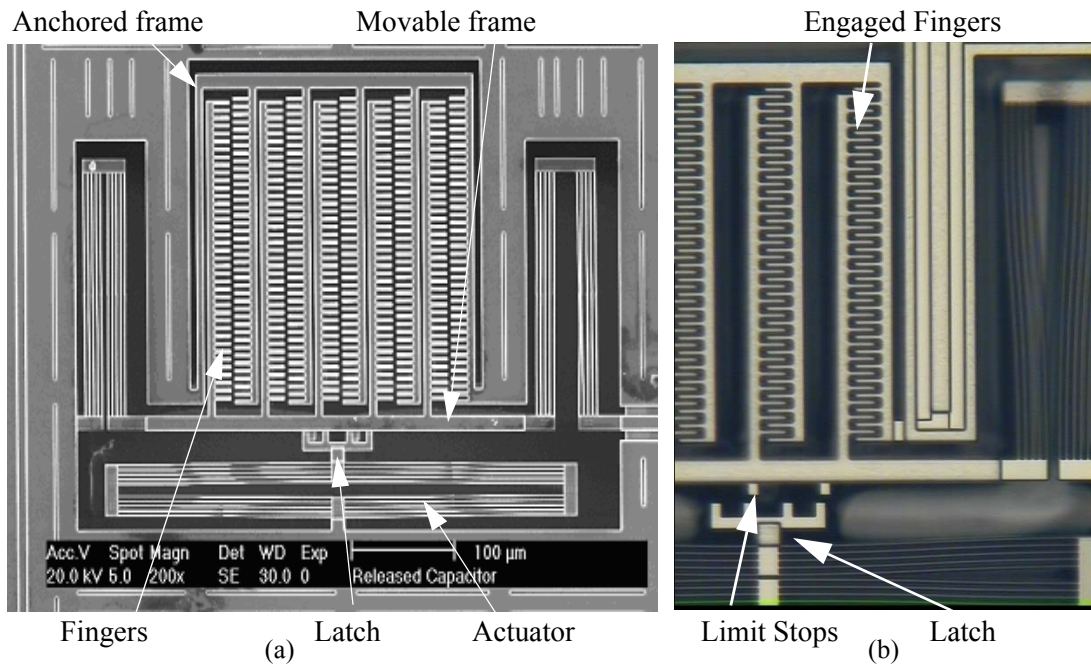
Figure 2-6. (a) SEM of reconfigurable finger-design capacitor. (b) Magnified view of latch at maximum capacitance state, showing engaged fingers.

11

changes the area overlap of the fingers. In the first generation design, due to insufficient space between fingers, interleaved movement did not occur. Instead, a maximum capacitance state was set by fixing minimum distance between adjacent beams. This alternate mode of operation restricted the tuning range. Measurements showed a 1:1.36 tuning range from 280 fF to 380 fF. The measured quality factor for this design was 5 in the operating frequency range [5]. A second generation design was fabricated with wider space between the fingers which exhibited finger engagement, leading to a wider reconfiguration (see Design D filter, Chapter 4).

2.3 MEMS Inductor

Quality factor is a major concern for on-chip inductors. Quality factor is given by the following equation, where Z is impedance:

$$Q = \frac{Im(Z)}{Re(Z)}$$

(2.1)

Based on the above definition, inductor quality factor is given by the following, where the loss $R_s(\omega)$ is represented as series resistance to the inductor L:

$$Q = \frac{\omega L}{R_s(\omega)}$$

(2.2)

At low frequencies, the series resistance R_s is dominated by the sheet resistance of the inductor metal windings. As this resistance is constant with respect to frequency, Q increases linearly with frequency in this regime. As frequency increases, the skin effect begins to play a role, reducing the effective cross-sectional area of the metal, and increasing the series resistance. Skin depth is given by [24]:

$$\delta = \sqrt{\frac{2}{\mu \sigma \omega}}$$

(2.3)

where μ is the magnetic permeability of the material, σ is the resistivity, and ω is the frequency of interest. The skin effect is inversely proportional to the skin depth, and the series resistance increases by

square root with respect to frequency. The skin effect becomes effective after about .5 GHz for typical RF

IC processes, when the skin depth is equal to the trace metal thickness [25]. Thus, the quality factor rise

slows down. The series resistance further increases due to another magnetic effect. Eddy current loops form

in metal turns due to the magnetic field lines of proximal turns. These field lines cancel out some of the exci-

tation current flowing through the turn, reducing the area through which excitation current flows, and

increasing the resistance [25]. This particularly affects the inner turns of the inductor [24]. This effect is

called the proximity effect, or current crowding effect. Current crowding effects increase linearly to qua-

dratically with frequency, affecting the concave downward shape in Q [25]. A third source of loss is elec-

trical and magnetic coupling to the conductive substrate, creating currents in the substrate and I^2R losses

[26]. Magnetic coupling occurs as an imaginary current loop is magnetically induced in the conductive sub-

strate [24]. In addition, this eddy current flows in the opposite direction as the current through the inductor,

which lowers the inductive reactance and lowers Q (see (2.2)). For higher resistivity substrates, magnetic

coupling is not so significant [27]. More significant is electrical coupling which creates displacement cur-

rents through the metal-to-substrate capacitance [25][27][28]. The different regimes for inductor Q and

series resistance are shown in Figure 2-7a and Figure 2-7b, respectively.

The self-capacitance of the inductor is the combined effect of metal-to-substrate capacitance, sub-

strate capacitance, turn-to-turn capacitance, fringing capacitance, and overlap capacitance from crossing

metal turns. Generally, the metal-to-substrate capacitance dominates [28], although for multi-turn or sym-

metrical inductors, the other sources of parasitic capacitance are not negligible. At the self-resonant fre-

quency, given by $\dfrac{1}{\sqrt{LC_{self}}}$, the inductor stops behaving as an inductor, and the quality factor is zero. A low

self-capacitance extends the inductor behavior to higher frequencies. As seen in Figure 2-7c, the reactance/

frequency is dominated by inductance at lower frequencies. Parasitic capacitance effects are seen as the

reactance graph changes from a relatively constant value, dominated by inductance, and enters the capaci-

tive reactance regime.
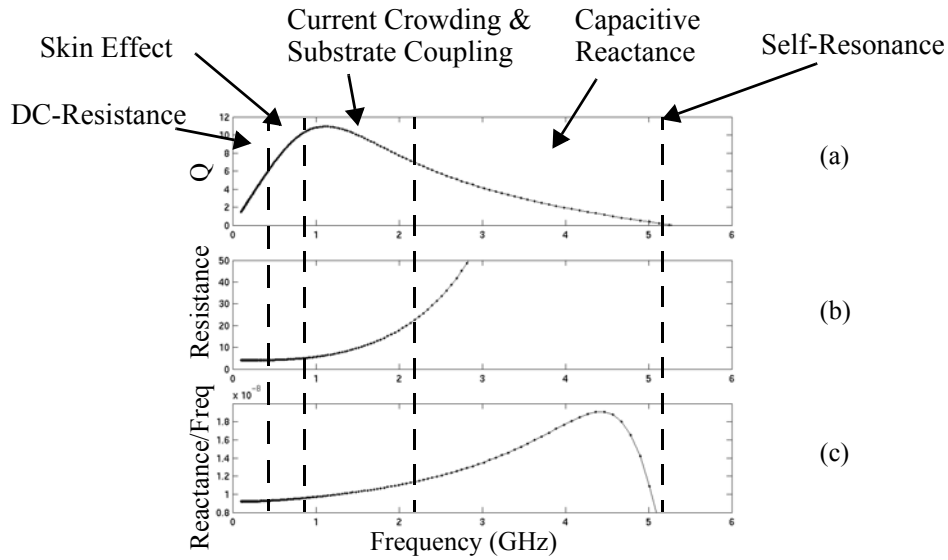
Figure 2-7. Different regimes across frequency for a 9.9-nH spiral inductor (400 μm outer diameter, 20 μm metal width, 4 turns) seen in (a) Q vs. frequency, (b) series resistance vs. frequency (c) reactance/frequency vs. frequency.

Several methods exist to improve inductor performance. Patterned ground shields [20] can increase the substrate resistivity and lower substrate losses, but at the expense of increasing parasitic capacitance to the substrate, as the substrate is closer to the metal turns. Self-resonance frequency is compromised with this method. If the conductive substrate is replaced with high-resistivity, insulating material (Silicon-On-Insulator processes), substrate losses are reduced.

Micromachining an inductor reduces both substrate losses and parasitic capacitance. Starting off with a foundry inductor (Figure 2-8a), micromachining first removes the oxide between turns, reducing the turn-to-turn capacitance (Figure 2-8b). The removed oxide capacitance C_{ox} is reduced by approximately four times, as the dielectric is replaced by air, as

$$C_{ox} = \varepsilon_{ox} C_{air} = 3.9 C_{air}$$

(2.4)

The silicon etch (Figure 2-8c) then removes the substrate, reducing the capacitive coupling, as the insulating layer of air above the substrate reduces the capacitance to the metal turns. The inductor perfor-

Figure 2-8. Micromachined inductor. (a) Foundry inductor with top dielectric layer removed to reveal lower layers. (b) Dielectric unprotected by metal etched, removing inter-turn dielectric. (c) Silicon substrate etched. Traces of substrate seen in figure, which results from the combined anisotropic and isotropic etch.

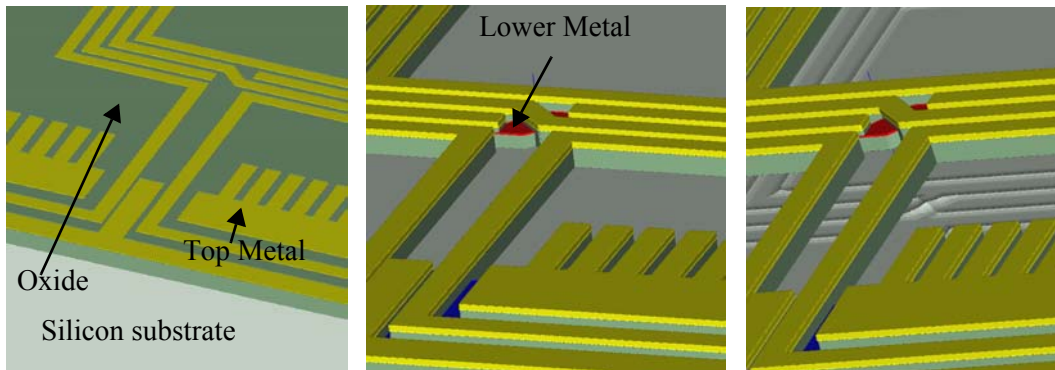mance improves in two ways. Firstly, the Q increases with reduced loss from the substrate. The second improvement is in self-resonant frequency. The parasitic capacitance is reduced, reducing self-capacitance. Increased self-resonant frequency allows the inductor to be operable at higher frequencies.

In the following subsections is a discussion on two different types of inductors that were fabricated and characterized.

2.3.1 Spiral Inductor

The inductance and Q of an inductor across frequency can be extracted using two-port S-parameters (see Appendix A). A lumped-parameter model of a micromachined, spiral inductor based on [29] is given in Figure 2-9. In this model, C_{t-t} is the inter-turn capacitance C_u is the underpass capacitance, C_{ox} is the oxide capacitance, C_{air} is the capacitance to substrate after substrate etching, C_{sub} is the substrate capacitance, R_s is the series resistance of the spiral and underpass, and R_{sub} is the substrate resistance.

NeoWave [30], a fast method-of-moments electromagnetic solver was also used to model the inductor. This solver is fairly accurate for unreleased inductors. However, as the solver uses a 2-D formulation, a lateral dielectric boundary cannot be specified. Therefore, the dielectric etch cannot be accurately modeled. The approximation used involves prediction both the minimum effect by only modeling substrate removal, and also the maximum effect by removing the SiO_2 altogether. A second limitation with NeoWave

is the amount of disk space needed for running the simulator, which allowed only small layouts to be simulated.

Figure 2-10 compares the micromachined and foundry inductor Q using both NeoWave and lumped-parameter schematic models. In the NeoWave model of the micromachined inductor, micromachining is simulated as a complete dielectric etch (maximum effect above). NeoWave predicts a 2X improvement in peak Q, and an improvement in self-resonant frequency of 2X. The lumped-parameter model predicts a 1.5X improvement in peak Q.
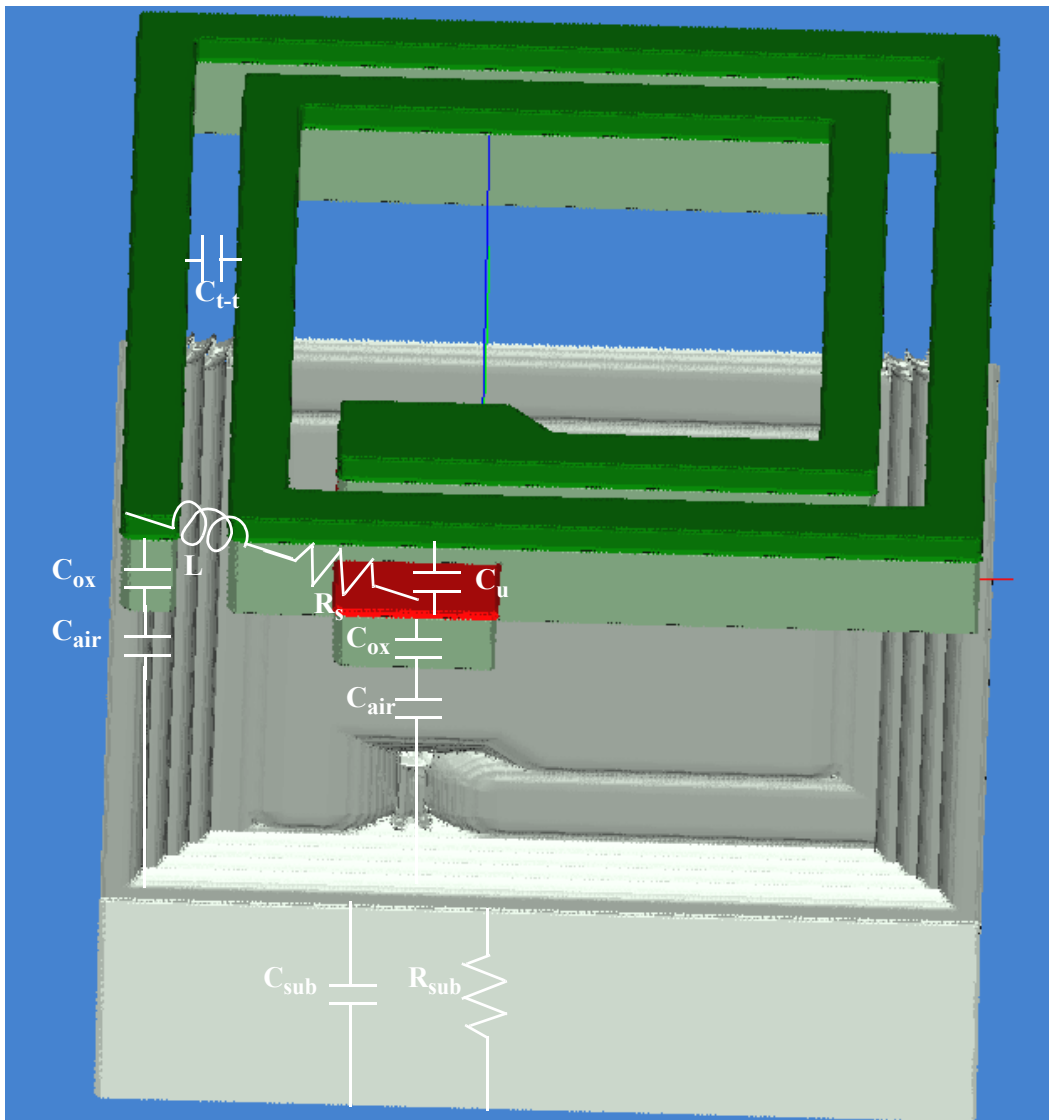
Figure 2-9. Lumped-parameter model of a spiral inductor.
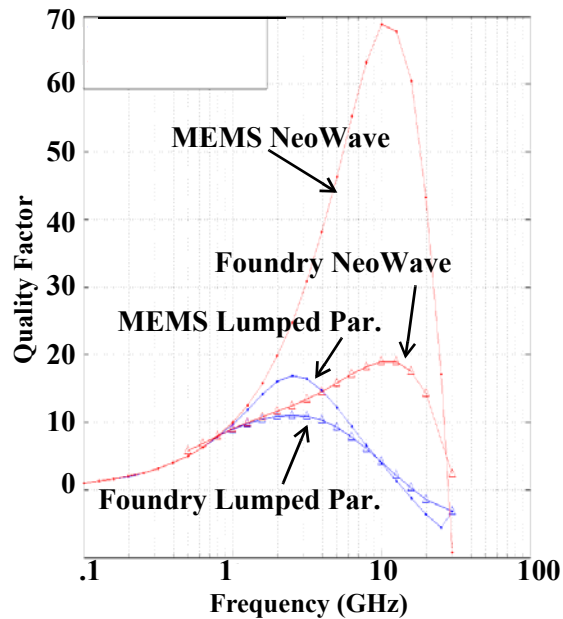
Figure 2-10. Q plots for a 3.122-nH octagonal, spiral inductor, showing lumped-parameter and NeoWave models before and after micromachining.

2.3.2 Symmetrical Inductor

A micromachined symmetrical inductor and its lumped-parameter model are seen in Figure 2-11. Since the currents through adjacent turns flow in the same direction, a positive mutual magnetic coupling occurs, enhancing the inductance per unit area [32]. Figure 2-12a shows a comparison of a 1-nH spiral and 1-nH symmetrical inductor. As can be seen, the symmetrical inductor has higher Q at lower frequencies. However, since the inter-turn and crossover capacitance is higher, the self-resonant frequency is lower in a symmetrical inductor.

Micromachining, as described earlier for a spiral inductor, improves both Q and self-resonant frequency for the symmetrical inductor. In fact, as seen in Figure 2-12b, a micromachined symmetrical inductor demonstrates more than .5X increase in peak Q and 3 GHz improvement in self-resonant frequency.
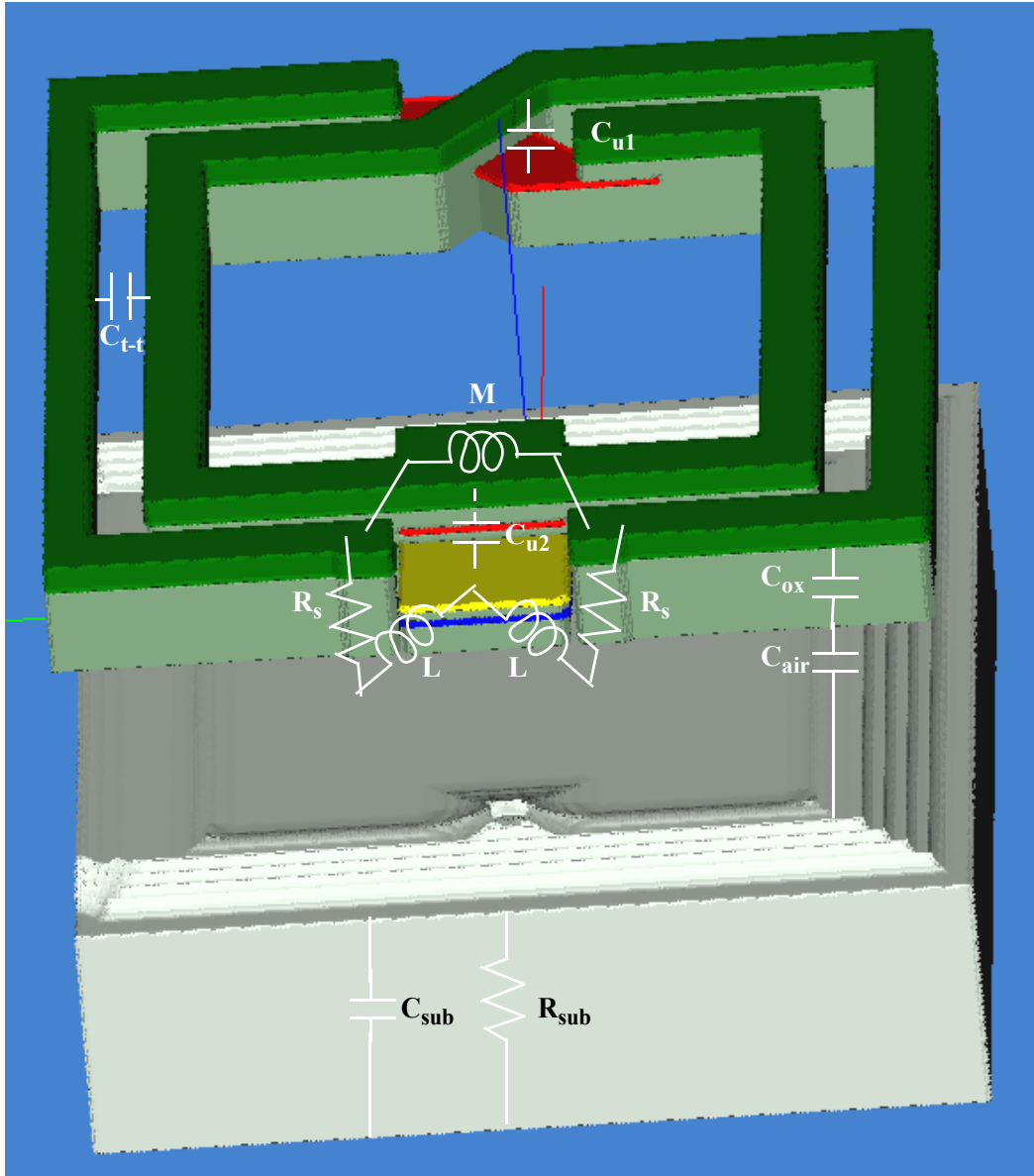
Figure 2-11. Lumped-parameter model of a symmetrical inductor.
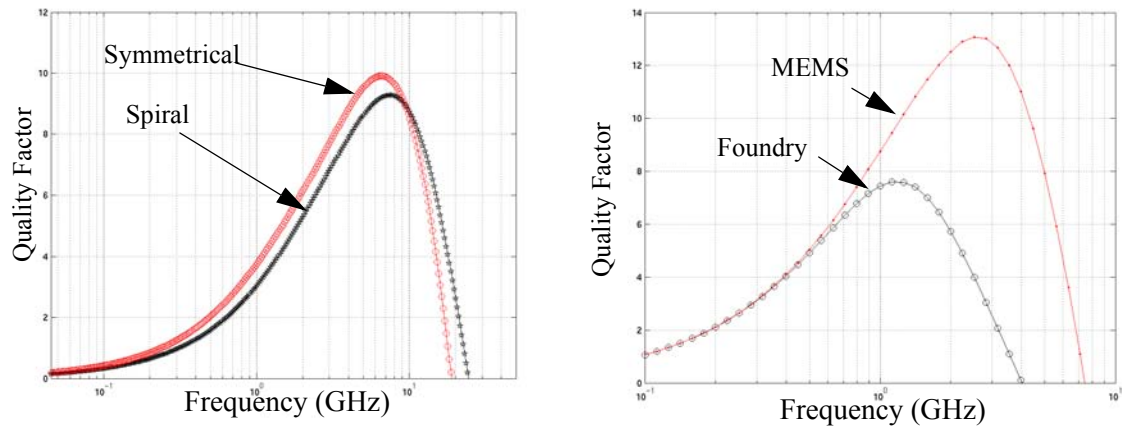
Figure 2-12. (a) Q plots comparing a 1-nH spiral inductor and 1-nH symmetrical inductor lumped parameter models. (b) Q of a symmetrical inductor before and after micromachining.

3 RF Filter Design

Filter design specifications include insertion loss (how much power is lost as the signal is transferred from input to output), ripple (the flatness of the signal in the passband), bandwidth (width of the passband), shape factor (sharpness of filter response), rejection (attenuation of undesired signals) and quality factor. As with most circuits, the circuit topology governs the scaling laws for each of these specifications. A π-network topology was chosen for the RF frequency-hopping filter. This topology was chosen primarily for its simplicity, as it was the first attempt in integrating MEMS capacitors with a MEMS inductor to compose an RF circuit. One disadvantage of this topology is its inherent narrowband response - insertion loss trade off. Since this filter is intended for use in the dual-hop MEMS receiver architecture described in Section 1.1, this trade-off is not very critical, as the filter bandwidth does not matter since the signal band filtering uses the high Q mechanical mixer filters later in the signal path.

3.1 Filter Topology

The filter topology is shown below in Figure 3-1. The filter is a Butterworth π-network, low pass filter, with dc-blocking capacitors to give a -20 dB/dec rolloff at low frequencies. This gives an effective
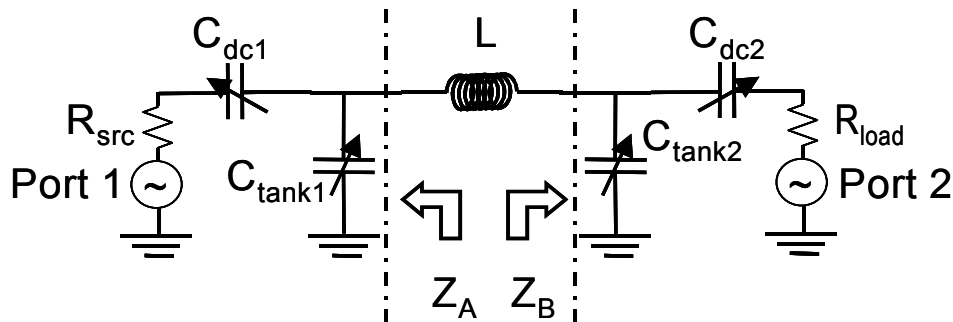
Figure 3-1. Butterworth π-filter topology. Topology contains four reconfigurable MEMS capacitors and a micromachined inductor.

bandpass response. The tank capacitors $C_{tank1,2}$ as well as the dc-blocking capacitors $C_{dc1,2}$ are reconfigurable MEMS capacitors and the inductor L is a micromachined inductor.

An analysis of the filter, assuming lossless passives, reveals a design methodology for obtaining the desired filter center frequency, Q, and insertion loss [35][36]. The impedances Z_A and Z_B as shown in Figure 3-1 need to be equal to ensure zero mismatch and full power transfer from the input to the output. Given that the input and output ports have equal impedance (50 ohms), the capacitance values have to be selected such that the design is symmetrical. The L and C value selection is also based on obtaining the quality factor Q_0 of the filter that gives the required bandwidth or harmonic rejection specification.

3.1.1 Lossless Π-Network Filter

To obtain an expression for Z_A and Z_B as shown in Figure 3-1, first the series combinations of C_{dc1} with R_{src} and C_{dc2} with R_{load} can be represented as parallel equivalents of R_1 with C_{pdc1} and R_2 with C_{pdc2}, respectively, as shown in Figure 3-2. Using the series-to-parallel transformation described in Appendix A, we obtain

$$R_1 = R_{src}(Q_{src}^2 + 1), R_2 = R_{load}(Q_{load}^2 + 1)$$

(3.1)

$$C_{pdc1} = C_{dc1}\left(\frac{Q_{src}^2}{Q_{src}^2 + 1}\right), C_{pdc2} = C_{dc2}\left(\frac{Q_{load}^2}{Q_{load}^2 + 1}\right)$$

(3.2)

where Q_{src} and Q_{load} are the series RC quality factors:
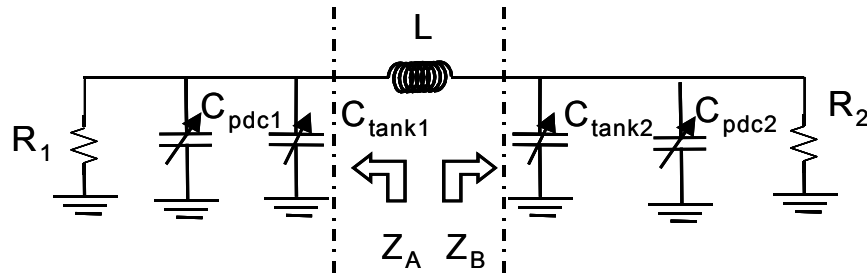
Figure 3-2. Circuit with transformation of series R_{src} and C_{dc1} to parallel R_1 and C_{pdc1} at input, and series R_{load} and C_{dc2} to parallel R_2 and C_{pdc2} at output.

21
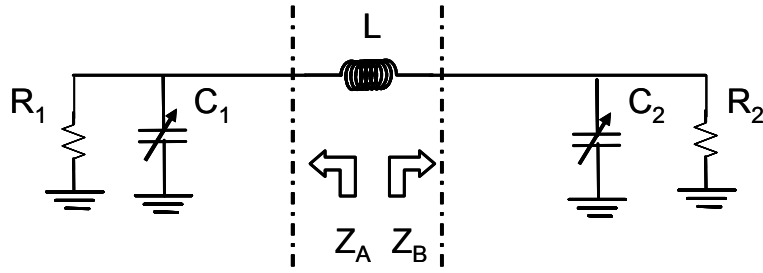
Figure 3-3. Circuit showing the combination of C_{pdc1} and C_{tank1} to form C_1 at input, and C_{pdc2} and C_{tank2} to form C_2 at output.

$$Q_{src} = \frac{1}{\omega R_{src} C_{dc1}}, Q_{load} = \frac{1}{\omega R_{load} C_{dc2}}$$

(3.3)

The new capacitances $C_{pdc1,2}$ can be added to $C_{tank1,2}$ respectively, as they are in parallel:

$$C_1 = C_{tank1} + C_{pdc1}, C_2 = C_{tank2} + C_{pdc2}$$

(3.4)

This is seen in Figure 3-3. Now the variables Z_A and Z_B shown in Figure 3-3 can be obtained. Z_A represents the equivalent impedance of R_1 and C_1, and Z_B, that of R_2 and C_2. For mathematical convenience, $R_{1,2}$ and $C_{1,2}$ are transformed to their series equivalents $R_{A,B}$ and $C_{A,B}$ (Figure 3-4). Using the parallel-to-series transformation in Appendix A the following is obtained:

$$R_A = \frac{R_1}{1 + Q_1^2}, R_B = \frac{R_2}{1 + Q_2^2}$$

(3.5)
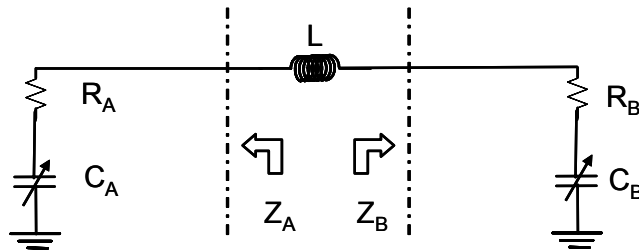
Figure 3-4. Circuit showing the transformation of parallel R_1 and C_1 to series R_A and C_A at input, and parallel R_2 and C_2 to series R_B and C_B at output.

$$C_A = C_1 \frac{Q_1^2 + 1}{Q_1^2}, C_B = C_2 \frac{Q_2^2 + 1}{Q_2^2}$$

<div align="right">(3.6)</div>

where Q_1 and Q_2 are the parallel RC quality factors:

$$Q_1 = \omega R_1 C_1, Q_2 = \omega R_2 C_2$$

<div align="right">(3.7)</div>

This transformation allows for simpler expressions for Z_A and Z_B, represented as:

$$Z_A = R_A - jX_A, Z_B = R_B - jX_B$$

<div align="right">(3.8)</div>

where $X_{A,B} = 1/(\omega C_{A,B})$. Q, by definition, can be represented as the imaginary part of an impedance divided by the real part of the impedance, as seen in Appendix A, (A.11). Thus $X_{A,B}$ is defined by the following equation.

$$X_A = R_A Q_1, X_B = R_B Q_2$$

<div align="right">(3.9)</div>

Now that Z_A and Z_B have been defined, the conditions for perfect matching can be derived. Perfect matching leads to full power transfer, for which the conjugate matching condition must be met (based on [35] and [37]). In the conjugate matching condition, Z_A must match the combination of the inductor impedance Z_L and Z_B.

$$\overline{Z_A} = Z_L + Z_B$$

<div align="right">(3.10)</div>

where the inductor impedance Z_L is

$$Z_L = 0 + jX_L = j\omega L$$

<div align="right">(3.11)</div>

Equation (3.10) is expanded by substituting in (3.8) and (3.11):

$$R_A + jX_A = jX_L + (R_B - jX_B)$$

<div align="right">(3.12)</div>

Equating the real terms we get Equation (3.13) and equating the imaginary terms we get Equation (3.14), which describe perfect matching:

$$R_A = R_B$$

(3.13)

$$X_L = X_A + X_B$$

(3.14)

Because $R_{src}=R_{load}$, the matching conditions imply a symmetrical design, leading to

$$C_{tank1} = C_{tank2} = C_{tank}, C_{dc1} = C_{dc2} = C_{dc}$$

(3.15)

The quality factor of the filter, viewed as a series RLC circuit, can be written in the inductive form as:

$$Q_0 = \frac{\omega_0(inductance)}{(resistance)} = \frac{X_L}{R_A + R_B}$$

(3.16)

When the filter is matched, it can be shown, with substitution of (3.9), (3.13), and (3.14) into (3.16) that

$$Q_0 = \frac{Q_1 + Q_2}{2}$$

(3.17)

Due to the symmetry of the filter, $Q_1 = Q_2$, which leads to

$$Q_0 = Q_1 = Q_2$$

(3.18)

Solving for $\omega = \omega_0$ from Equation (3.14), the resonant frequency is

$$\omega_0 = \frac{X_A + X_B}{L}$$

(3.19)

Substituting in (3.19) for $X_{A,B}$ using Equations (3.1), (3.2), (3.4), (3.9), (3.15), and (3.18), the resonant frequency can be written as
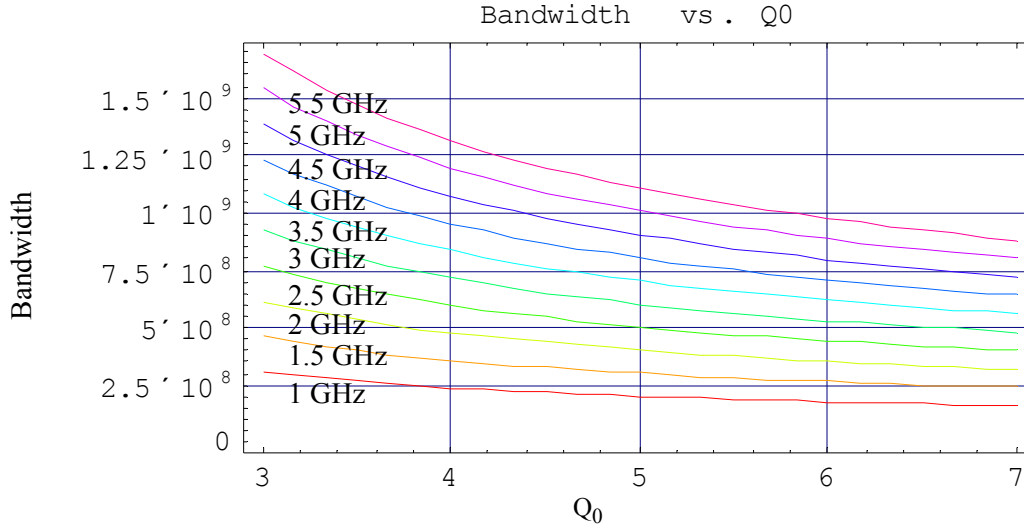
Figure 3-5. Bandwidth vs. Q plot. Plots for various center frequencies are shown.

$$\omega_0 = \sqrt{\frac{Q_0^2}{Q_0^2+1}} \frac{1}{\sqrt{\frac{L}{2}(C_{tank}+C_{pdc})}} \approx \frac{1}{\sqrt{\frac{L}{2}(C_{tank}+C_{dc})}}$$

(3.20)

Filter Q is essentially a measure of the harmonic attenuation around the center frequency ω_0. In a narrowband filter, high harmonic attenuation is desired. Often the harmonic attenuation specification is indicated by required bandwidth. Since 3-dB bandwidth is defined as

$$3\text{-dB bandwidth} = \frac{\omega_0}{Q_0}$$

(3.21)

the filter Q is the design variable to set filter bandwidth, given ω_0. Figure 3-5 shows bandwidth vs. Q_0 for several resonant frequencies between 1 and 5.5 GHz, showing the corresponding bandwidths for given Q.

3.1.2 Lossy Π-Network Filter

Another consideration in the filter design is the sensitivity to parasitic losses. A simplified model of the filter with lossy passives includes a series resistance r_{Ls} with the inductor L, and a series resistance $r_{Ci=A,Bs}$ with each total capacitance C_A and C_B (from Figure 3-6). Parasitic resistance introduces insertion
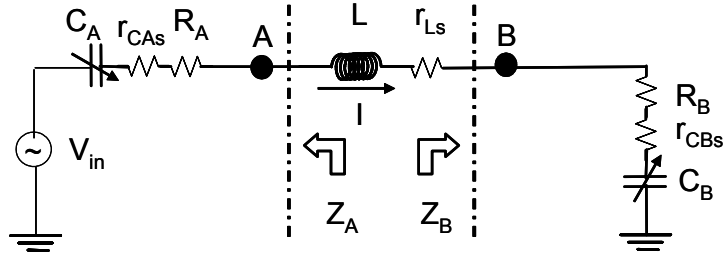
Figure 3-6. Circuit showing lossy components, series $r_{CA,Bs}$ with $C_{A,B}$ and series r_{Ls} with L.

loss due to both direct power dissipation and mismatch. However, insertion loss due to mismatch is gener-

ally negligible compared to direct power dissipation [36]. These parasitic resistances at the resonant fre-

quency can be approximated by using the series RL ((3.22)) and series RC ((3.23)) circuit models.

$$r_{Ls} = \frac{\omega_0 L}{Q_L}$$

(3.22)

$$r_{Cis} = \frac{1}{Q_{Ci}\omega_0 C_i}$$

(3.23)

In these expressions, Q_L is the inductor quality factor and Q_{Ci} is the capacitor $C_{i=A,B}$ quality factor.

In delivering the input power P_{in} to the output as P_{out}, some power P_N is dissipated in the circuit.

$$P_{in} = P_{out} + P_N$$

(3.24)

Given the expression in (3.24), the input to output power relation in terms of Q of the passives can

be derived. This is important in giving an idea of how quality factor affects the power transfer. First, the

loop current I shown in Figure 3-6 can be defined.

$$I = \frac{V_{in}}{(R_A + r_{CAs} + R_B + r_{CBs} + r_{Ls}) + j(X_L - X_A - X_B)}$$

(3.25)

where V_{in} is the input voltage, shown in Figure 3-6. Substituting (3.16) into (3.22), the lossy element r_{Ls}

can be represented as

$$r_{Ls} = \frac{X_L}{Q_L} = \frac{(R_A + R_B)Q_0}{Q_L}$$

(3.26)

Similarly, $Q_0 = Q_{1,2}$, which describes the relation between $R_{A,B}$ and $C_{A,B}$ in (3.9), can be substituted into Equation (3.23), and r_{Cis} can be represented as

$$r_{CAs} = \frac{X_A}{Q_{CA}} = R_A \frac{Q_0}{Q_{CA}}, r_{CBs} = \frac{X_B}{Q_{CB}} = R_B \frac{Q_0}{Q_{CB}}$$

(3.27)

Now, taking into account (3.13) and (3.14) which hold when the filter is matched, (3.25) can be simplified by substituting in (3.26) and (3.27), giving the following:

$$I = \frac{V_{in}}{2R_{A,B}\left(1 + Q_0\left(\frac{1}{Q_L} + \frac{1}{Q_{CA,B}}\right)\right)}$$

(3.28)

For convenience, δ is defined as $Q_0\left(\frac{1}{Q_L} + \frac{1}{Q_{CA,B}}\right)$ where $\delta = 0$ when there is no resistive loss. Then the net quality factor of the passives will be written as

$$Q_p = \frac{1}{\frac{1}{Q_L} + \frac{1}{Q_{CA,B}}}$$

(3.29)

leading to

$$\delta = \frac{Q_0}{Q_p}$$

(3.30)

Considering the matching condition in (3.13), it can be seen that

$$P_{out} = |I|^2 R_B = |I|^2 R_A$$

(3.31)

The direct power losses due to the parasitic resistances can be expressed as follows:

$$P_N = |I|^2(r_L + 2r_{Ci}) = |I|^2 R_A(2\delta)$$

(3.32)

27

The power transfer from output to input is given by the following equation. Any direct power loss during transmission leads to $P_{out} < P_{in}$.

$$\frac{P_{out}}{P_{in}} = \frac{1}{1 + 2\delta}$$

(3.33)

As can be seen from (3.33), high filter Q (Q_0) leads to high δ ((3.30)), lowering the power transfer if passive Q's are finite, presenting a trade-off in the desired filter response. This can be restated as, for a given center frequency, narrow bandwidth leads to high insertion loss.

The quality factor of the filter is degraded by the finite Q of passives. Inclusion of losses gives a filter quality factor Q_0^* of

$$Q_0^* = \frac{1}{\frac{1}{Q_0} + \frac{1}{Q_p}}$$

(3.34)

3.2 Performance Specifications

The bandpass filter requirements of a receiver front-end architecture set the design specifications for the frequency-hopping filter. In the front-end, the bandpass filter is fed by a 50-ohm antenna and is loaded by the 50-ohm input impedance of an LNA. This identical input and output impedance led to the design constraint of symmetry, as discussed in Section 3.1.1.

The filters have been designed to cover a wide range of the communications spectrum. The designs mostly operate within the 2GHz band (~1-3 GHz), the internationally allocated band for fixed and mobile services including mobile satellite services such as Personal Communication Services (PCS) [38]. A high frequency-hopping range is desired, exhibiting similar bandwidth and low insertion loss at both frequencies at which the filter operates.

Due to the desired narrowband response for the hop resolution requirement in the architecture, bandwidths less than 400 MHz were specified. As a comparison, off-chip passive filters such as SAW filters

achieve bandwidths of 100 MHz for low insertion loss (less than 2 dB) within the required operating range [39]. Considering the Q and insertion loss limitations for this on-chip topology, 400 MHz was a reasonable specification to achieve. This translates to Q around 5 (Figure 3-7).

As on-chip passive filters generally have high loss [18], minimizing insertion loss was also a constraint on bandwidth choice. As a rule of thumb, the filters presented here are designed for less than 5 dB insertion loss, which translates to about 30% power transfer.

When the filter is operating at the lower frequency, high attenuation at the higher frequency is required, and vice versa. High quality factor and identical insertion loss are needed for this capability. Considering insertion loss of 5 dB, at least 3X rejection of the alternate frequency is desired, or 15 dB rejection magnitude.

3.3 Design Procedure

Design of this topology is an iterative process, based on several trade-offs, including filter Q vs. insertion loss and inductor performance vs. capacitor tuning range.
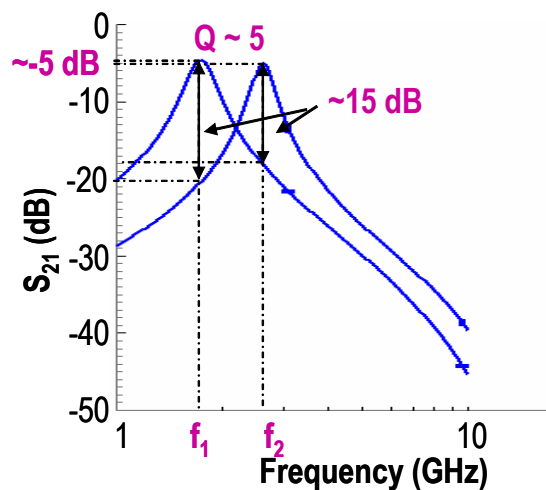
Figure 3-7. Example S_{21} response of a filter at both minimum and maximum frequency, showing the performance specifications.

3.3.1 Filter

The design process for a filter includes considerations of wide reconfigurable range, filter Q (band-width), and insertion loss. Filter Q and insertion loss must be designed at both resonant frequencies. Starting from (3.18) and (3.7), and substituting for R_1 and C_1 using (3.1), (3.2), and (3.4), and then substituting for Q_{src} using (3.3), and expression for filter Q is obtained, in terms of the circuit elements:

$$Q_0 = \left(1 + \frac{C_{tank}}{C_{dc}}\right)\frac{1}{C_{dc}R_{src}\omega_0} + C_{tank}R_{src}\omega_0$$

(3.35)

From (3.35), it can be seen that increasing the C_{tank}/C_{dc} ratio improves Q. When lossy elements are considered, the filter Q degrades overall, as demonstrated in (3.34).

When losses are considered, designing for high filter Q has the effect of increasing insertion loss, however, as explained in (3.33). An additional factor in this trade-off is the capacitive divider created by the tank and dc-blocking capacitors at the output, as shown in Figure 3-8a. For maximum voltage transfer to the output, the C_{tank}/C_{dc} must be decreased. This relationship between the C_{tank}/C_{dc} ratio and insertion loss is seen in Figure 3-8b, which shows the S_{21} response of several lossy π-filters, obtained by parametrically changing the C_{tank}/C_{dc} ratio.
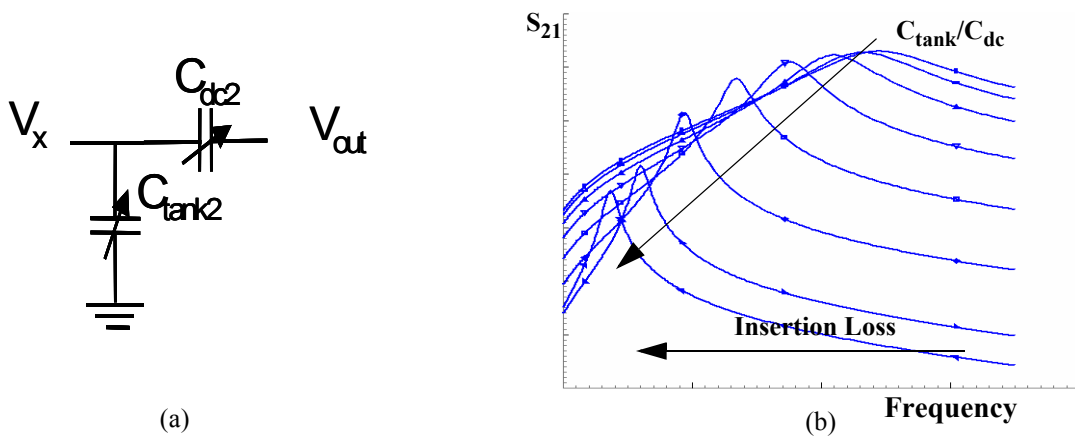
Figure 3-8. (a) Capacitive divider at output shown, created by C_{tank2} and C_{dc2}. (b) S_{21} response of several lossy filters. As C_{tank}/C_{dc} ratio increases, the insertion loss also increases, due to the capacitive divider at the output.
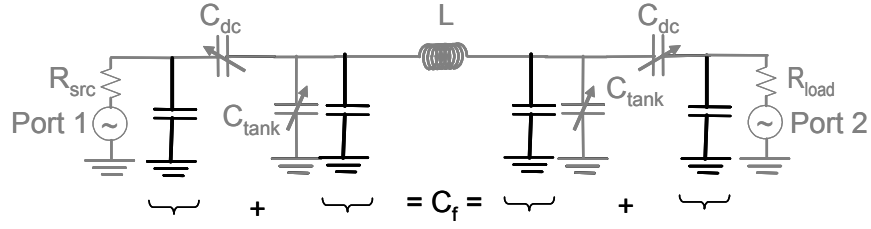
Figure 3-9. Filter schematic showing interconnect capacitances.

Next the values for C_{tank} and C_{dc} can be computed. The center frequency equation, (3.20), decides the total value of necessary capacitance, C_{tot}. In a realistic sense, a finite amount of fixed interconnect capacitance to substrate C_f is introduced by routing in the layout. The total required capacitance for each resonant frequency therefore, comes from the MEMS capacitors as well as this fixed interconnect capacitance. The filter schematic including interconnect is shown in Figure 3-9. C_{dc} and C_{tank} are set by solving the three simultaneous equations (3.9), (3.14), and (3.20):

$$C_{dc} \approx \frac{1}{\omega_0 \sqrt{\omega_0 \frac{L}{2} R_{src} Q_0^* - R_{src}^2}}$$

(3.36)

$$C_{tank} \approx C_{tot} - C_{dc} - C_f$$

(3.37)

The filter was simulated and the C_{tank}/C_{dc} ratios were iteratively adjusted to obtain matching insertion loss at both frequencies, for maximum attenuation at the alternate frequency. The chosen filter topology reveals the simplicity of the design due to symmetry, and the limitations of this topology due to trade-offs.

3.3.2 Capacitors

MEMS capacitor design is the beyond the scope of this thesis. The filters described in this thesis use the designs developed by Altug Oz, which are described in [4][5]. This section summarizes the device design issues from a circuit design viewpoint. Two designs were developed for the MEMS capacitor. The design methodology differs for the two designs.

31

In designing the capacitance value and the tuning range for a beam-based MEMS capacitor, the design parameters are the beam length, width, beam-to-beam spacing and number of beams. For larger capacitance values, multiple capacitors can be wired in parallel. One constraint includes the allowable spacing rules to ensure release [40], as well as area. The range of tunability is constrained by the voltage-displacement transfer function of the electrothermal actuator and amount of applied voltage on the polysilicon resistors without burning out the resistors. For the finger design topology, the design parameters and constraints are similar to the beam design capacitor.

3.3.3 Inductor

The primary considerations in designing a spiral inductor for a frequency-hopping filter are the inductance, the quality factor at the operating frequencies, and self-resonant frequency. The design parameters are the number of spirals n, metal width w, turn-to-turn spacing, s, outer diameter d, and inner radius r.

To determine the inductance value, the overall LC tank for the circuit should be considered first. With MEMS capacitors, the achievable tuning range constrains the choice of inductance for the given operating frequencies. A secondary consideration is the area.

The design parameters can be chosen based on maximizing quality factor, self-resonant frequency and minimizing area; however, there are trade-offs in these design choices. Increasing the number of turns has the effect of increasing inductance. The number of turns is especially important for symmetrical inductors, because the inter-turn and crossover capacitance is higher. Wider metal reduces the series resistance, and with micromachining the potential increase in substrate eddy currents is eliminated. Larger inner and outer diameters enhance the inductance as opposite currents on opposite sides do not cancel each other out, but at the expense of area. In general, the inner diameter should be greater than 5X the metal width for minimal negative coupling between opposite sides of the inductor [27]. Reduced spacing between turns is advantageous in increasing mutual coupling for higher inductance, but inter-turn capacitance increases, and minimum spacing for complete MEMS release [40] should be considered. A minimum distance of 5X the

metal width should be maintained between the outer edge of the inductor and other devices on chip to avoid parasitic electromagnetic coupling [27].

4 Results and Discussion

The inductors discussed in Chapter 2 and the π-filter discussed in Chapter 3 were designed, fabricated and tested. Each filter design incorporated improvements from previous designs. This chapter presents measurement results of these devices and circuits. Characterization and comparison to simulations are presented as well.

4.1 Inductors

Several inductors were characterized to assess the improvements due to micromachining, to compare simulation models to measured results, and to compare various inductor topologies. These comparisons were used to choose the inductor for subsequent filter designs. The following subsections discuss this characterization.

4.1.1 1st Design: Symmetrical Inductor

Figure 4-1a shows the layout of a 1-nH, symmetrical inductor fabricated in the IBM SiGe6HP process. The inductor is surrounded by a corrugated frame, which defines the opening needed to release the inductor. The corrugation on the inside of the frame is intended to break up the eddy currents circling in the closed frame loop. Two-port, S-parameter measurements were taken using a 2-port network analyzer (test setup shown in Appendix A). As can be seen from the measured results before and after release in Figure 4-1b, there is little improvement due to micromachining, showing peak Q's around 5. At higher frequencies, some Q improvement is seen. This limited Q improvement is due to the capacitance of the pads, that were not deembedded in measurement. Simulations using NeoWave inductor models with pad lumped-parameter models demonstrate their effect on Q. The pad model (Figure 4-1c) incorporates capacitance to substrate,
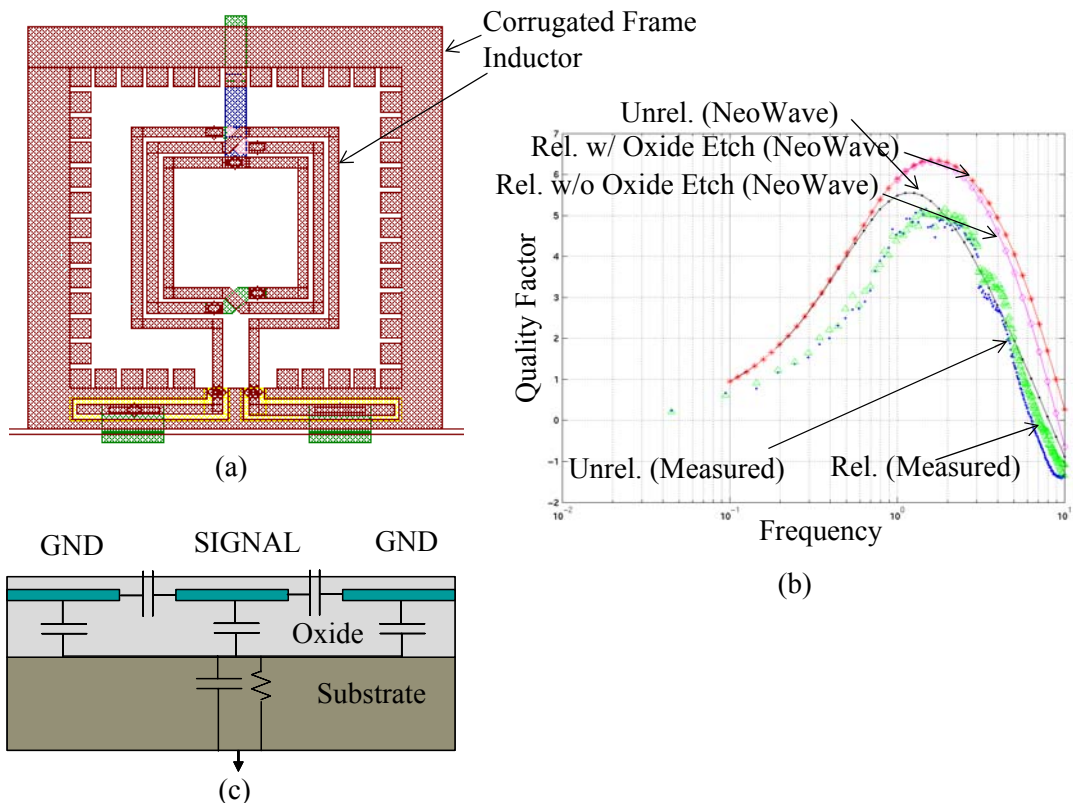
Figure 4-1. (a) 1st design symmetrical inductor layout. (b) Measurements and NeoWave simulations of Q vs. frequency for inductor before and after release. (c) Lumped parameter model of pad.

substrate capacitance and resistance, and pad-to-pad capacitance. The simulated micromachined inductor structure shows little Q-improvement. From this measurement it can be seen that a deembedding process is necessary to accurately characterize the inductor.

4.1.2 Deembedding

Several types of deembedding structures were fabricated to determine the best method for deembedding. They are listed below.

1. Open, short, thru, and 50-Ω load structures of pads with interconnect to inductor (Figure 4-2a)
2. Open, short, thru, and 50-Ω load structures of pads with interconnect to inductor, and corrugated frame (Figure 4-2b)

By comparing the deembedding of the pads and interconnect (Figure 4-2a), with the deembedding of the pads, interconnect, and frame (Figure 4-2b), the effect of the frame on Q could be observed. A loop

35
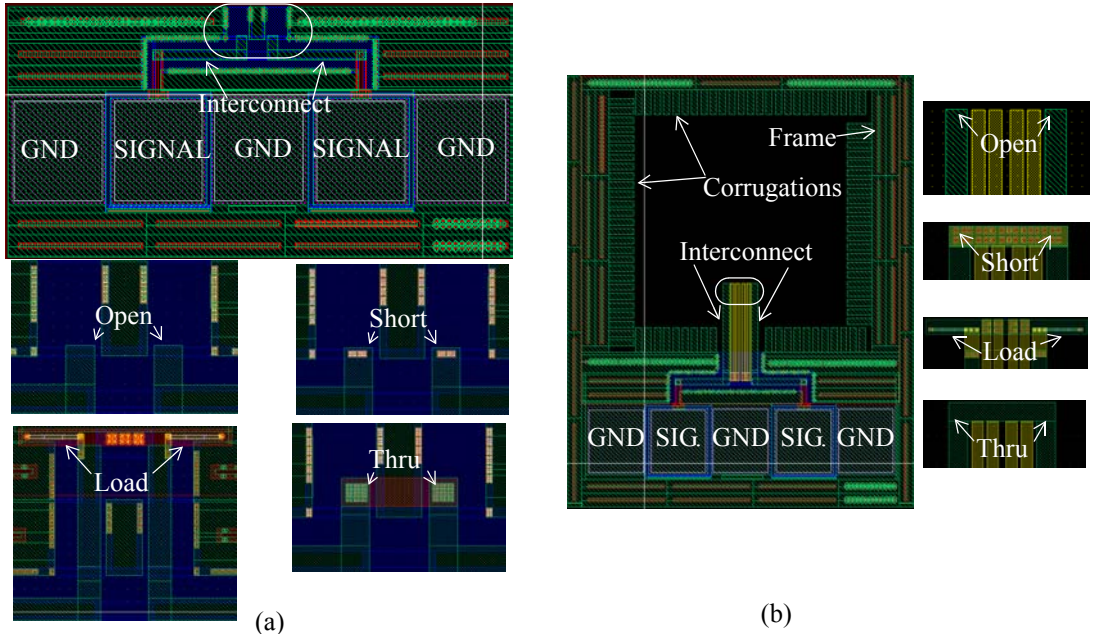
Figure 4-2. Deembedding structures, with enlarged view of open, short, load and thru shown along with complete structure. (a) Pads + interconnect (b) Pads + interconnect + frame

around an inductor can lower the Q, due to the eddy currents induced, if the distance between the frame and inductor is less than $5w$, where w is the width of the metal for a spiral inductor [6][22]. Measured results for a micromachined 2-nH symmetrical inductor with $8w$ distance to the frame are compared to measured results of the inductor with the frame deembedded (Figure 4-3a). In both cases, the pads and interconnect were deembedded. It can be seen that the frame does not lower Q. The apparent higher Q for the inductor with the frame is attributed to the observed fluctuations in the measured S-parameters. In testing the effects of the frame, a second experiment was done to observe the benefits of corrugations on the frame. Measure-
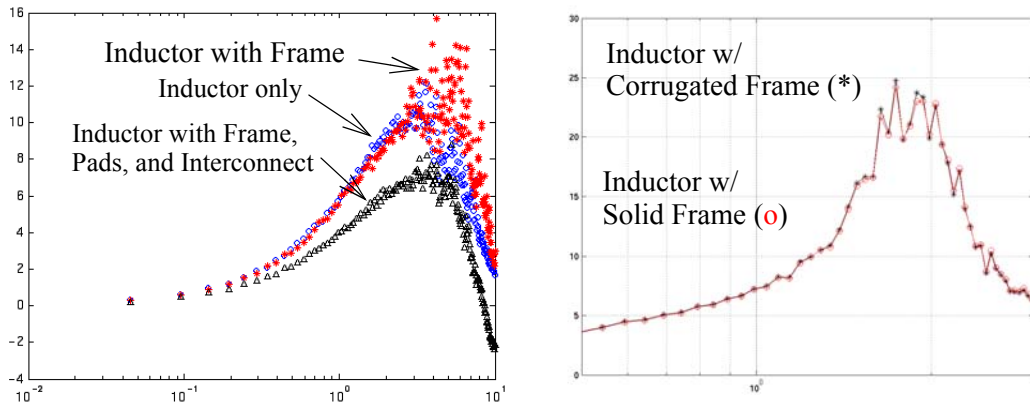
Figure 4-3. (a) Q for 2-nH symmetrical inductor shows that frame does not lower Q. (b) Comparison of Q for 6-nH symmetrical inductor with corrugated frame and solid frame. Q does not change.

36

ments on a 6-nH symmetrical micromachined inductor with and without corrugations on the frame showed little difference (Figure 4-3b). This shows that the primary consideration when designing the frame is that an adequate distance is maintained between the frame and inductor. With an adequate distance, the corrugations make no difference.

Several deembedding techniques were tested: (a) WinCal software was used to remove pad parasitics; (b) the network analyzer was calibrated with on-chip deembedding open, load, short and thru structures rather than to the Cascade Impedance Standard Substrate; (c) the Y-parameter deembedding technique using open and short deembedding structures; (d) the Y-parameter deembedding technique using just open deembedding structures on chip. Deembedding only open structures gave the least fluctuations in the measured S-parameters, so this method was used for the remaining measurements in this thesis.

4.1.3 2nd Design: Symmetrical Inductors

A 2-nH symmetrical inductor was characterized in the Jazz process applying the open-only deembedding process described above. This particular inductor was chosen for characterization as two of the filter designs incorporated this inductor (Designs A and C).

A lumped-parameter simulation model was created for this inductor, both for the unreleased and the released case. NeoWave was also used to simulate this inductor. Figure 4-4 shows the simulation models along with measured results (obtained by deembedding the pads, interconnect, and frame).

The inductance (Figure 4-4a) does not change after micromachining, as expected. The improvement in self-resonant frequency is seen in Figure 4-4a, as the onset of capacitance effects occurs at higher frequencies, seen by the rise in reactance/frequency. The peak Q increases by more than a factor of 1.5 after release as seen in measured data (Figure 4-4b). The self-resonant frequency also increases by more than 5 GHz. Both the simulation models are accurate at low frequencies. The lumped-parameter model accurately predicts the peak Q value, although the self-resonant frequency is slightly overestimated, which may be due to the assumption that all interconnect has been deembedded. The NeoWave model overestimates the

37
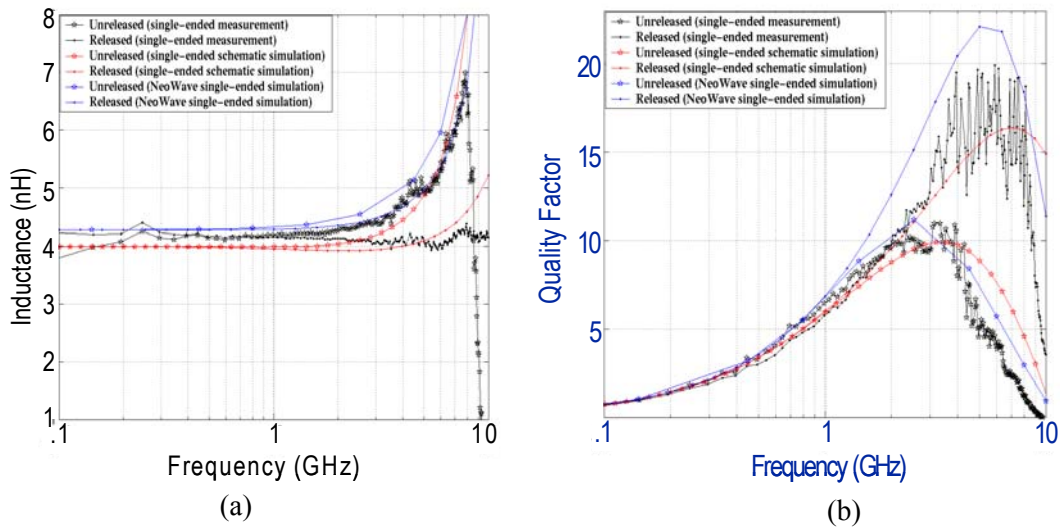
Figure 4-4. Simulation and measurement of unreleased and released 2-nH symmetrical inductors. (a) Inductance (reactance/frequency) vs. frequency plot (b) Q vs. frequency

improvement in peak Q, although the self-resonance and peak Q frequency match measured data. This is

due to the inability to exactly recreate dielectric etching in the NeoWave process definition - a complete

dielectric etch was used as an estimation.

As can be seen in Figure 4-4b, there is a slight degradation in Q at low frequencies after micromachining. This can be explained by the thinning of the metal due to the ion milling in the post-processing, which increases the series resistance.

4.1.4 3rd Design: Spiral vs. Differential Inductors

A simple spiral inductor and a differential inductor of 2.5-nH inductance were laid out and fabricated. The simple inductor was a square spiral and the differential inductor had square, symmetrical topology and a grounded center-tap. These test structures were created in order to compare the performance of different inductor geometries. As can be seen from the pre-micromachining, lumped-parameter simulation in Figure 4-5a, the differential inductor shows improvement in peak Q by a factor of 20%. The self-resonant frequency is lower in the differential case, due to the crossover capacitance in the symmetrical geometry. In the micromachined case, overall improvement in peak Q and self-resonant frequency is expected in both cases (see Chapter 2). In measurement (Figure 4-5b), close to 30% peak Q improvement due to microma-
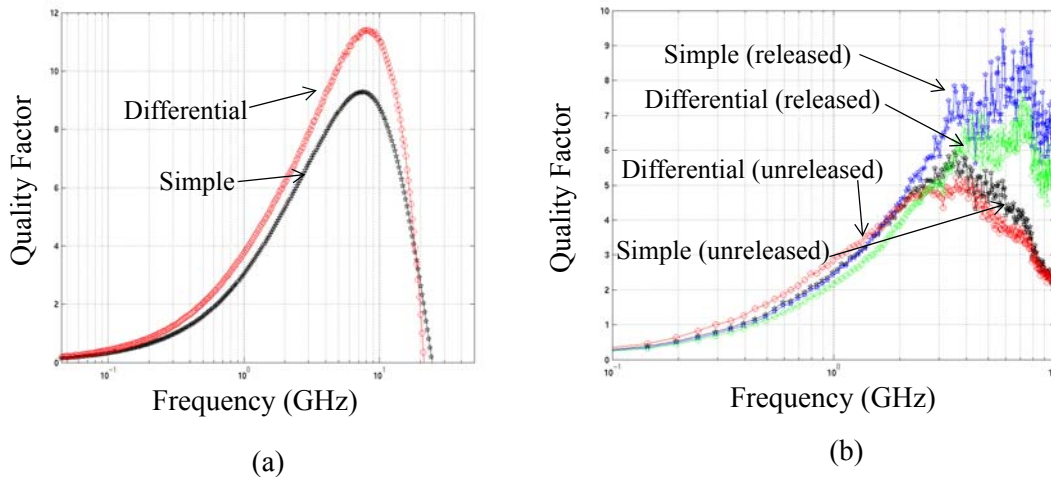
Figure 4-5. Q vs. frequency for 2.5-nH simple spiral inductor and differential inductor. (a) Lumped-parameter simulation of unreleased inductors. (b) Measurement of unreleased and released inductors.

chining is observed for both the simple and differential inductors. However, the differential inductor does not show superior performance to the simple inductor, as expected. This is due to the center tap being grounded to the top metal layer, rather than an off-chip ground, so the ground introduces parasitics. Improvements to this experiment can be made by comparing a simple inductor to a symmetrical inductor with open center tap. A symmetrical inductor with open center tap can be measured both single-endedly and differentially, which allows for three inductor comparisons.

Below is a summary table of the measured inductors described in this section.

Table 4-1. Summary of inductor measurement results.

Inductor	Geometry	Micromachined?	Inductance	Peak Q	Self-Resonant Freq.
1st Design (IBM 6HP)	Symmetrical	No	1 nH	5	6.5 GHz
		Yes	1 nH	5	7 GHz
2nd Design (Jazz SiGe60)	Symmetrical	No	4 nH	10	10 GHz
		Yes	4 nH	15	15 GHz
3rd Design (Jazz SiGe60)	Simple spiral	No	2.5 nH	5.5	15 GHz
		Yes	2.5 nH	7.5	20 GHz
	Symmetrical (differential measurement)	No	2.5 nH	5	15 GHz
		Yes	2.5 nH	7	15 GHz

4.2 RF Filter

Four π-filter designs were fabricated and tested on the Cascade RF probe station. The first design was done in the IBM SiGe6HP process, while the succeeding designs were in the Jazz SiGe60 process. The following subsections show design simulations and results from measurement. A summary of the designs and measured results is presented at the end of the section.

4.2.1 Design A

A frequency hop from 1.2 GHz to 2.1 GHz, Q's greater than 5 and equal insertion loss at both frequencies, were the goals for this design. The inductor value was chosen to be 28 nH. Due to the large number of turns that would require, the inductance was split into two series 14-nH octagonal, spiral inductors. For a 14-nH inductor, the peak Q is around 1.2 GHz. After micromachining the peak Q is expected to increase, such that 1.5X improvement in Q can be observed at 1.2 GHz and 6X improvement in Q at 2.1 GHz (Figure 4-6a). An RC-model for the MEMS capacitors was used in the design process.

Figure 4-6b shows the simulated S_{21} response at both capacitance configurations, showing the two resonant frequencies. The functionality of the filter can be demonstrated by simulating the antenna input signal with a PWL voltage source feeding into a VCO to create a chip signal. As shown in the transient response in Figure 4-6c, the signal at 1.2 GHz and 2.1 GHz is passed through. At maximum capacitance, the Q is 7.6 with 15 dB insertion loss. At minimum capacitance, the Q is 5.5 with 17.8 dB insertion loss.

To compare using MEMS capacitors with other existing on-chip variable capacitors for this filter, Figure 4-6d shows the S_{21} response incorporating accumulation mode NMOS varactors, instead of MEMS capacitors. The achievable frequency hop range is lower (1.19 GHz to 1.75 GHz).

The design schematic is shown in Figure 4-7a and the layout in Figure 4-7b. The extracted layout was simulated to show the expected unreleased filter S_{21} response (Figure 4-7c). As can be seen, a peak is seen at the frequency 699 MHz, which is close to the measured filter peak at 678.9 MHz (Figure 4-7d). The
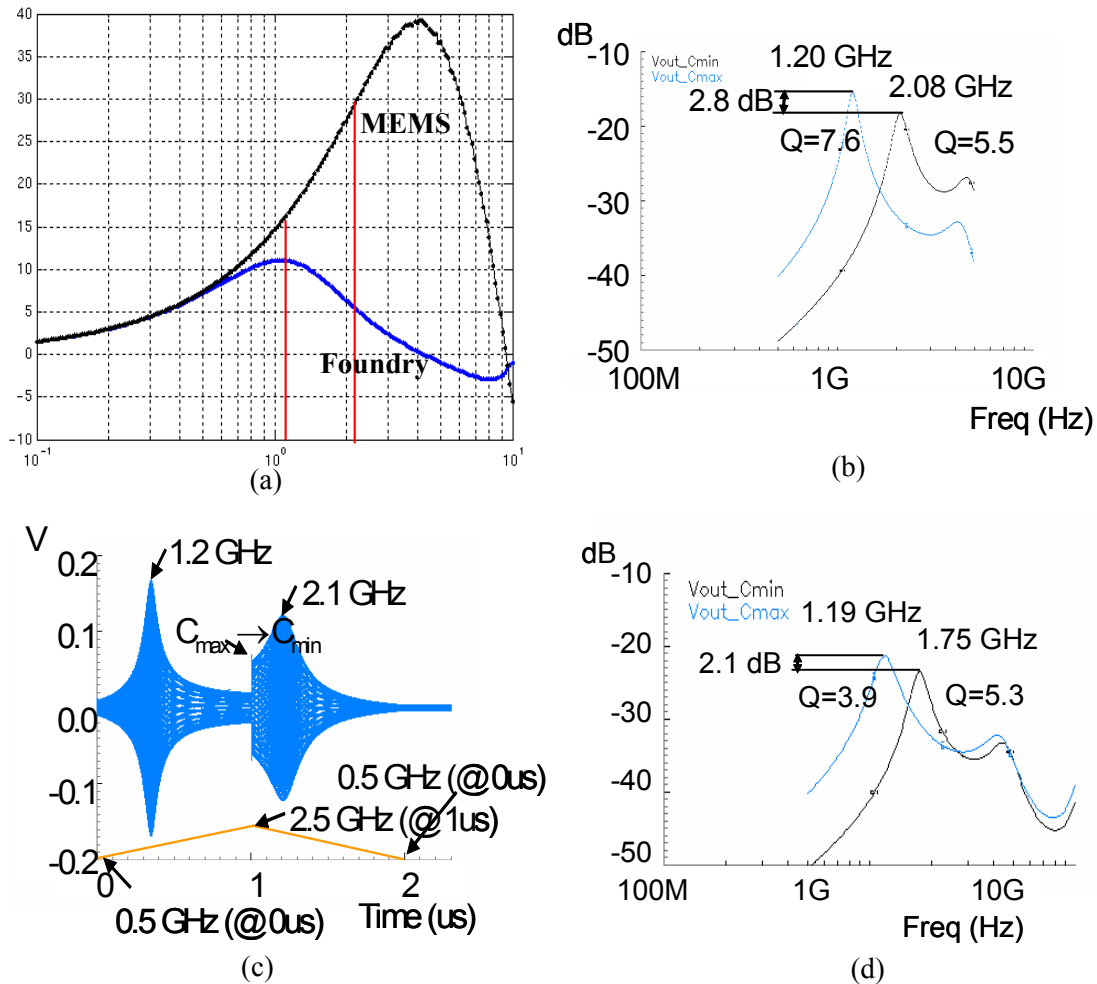
Figure 4-6. (a) Q vs. frequency for a 14-nH, spiral inductor using lumped-parameter models, before and after micromachining. (b) S_{21} response of Design A filter at the two capacitor configurations. (c) Transient response simulation with antenna input signal modeled as a PWL voltage source. (d) s_{21} response with accumulation mode NMOS varactor.

other (larger) peak around 2.3 GHz is due to the parasitic self-capacitance in the inductor (estimation method shown in [20]) and the inductor forming an LC resonating tank. This peak can also be seen in the simulation curve of Figure 4-6b at 5 GHz.The measured insertion loss is 30 dB and Q is 2.8.

The S_{21} response after release is shown in Figure 4-8a and Figure 4-8b at both capacitor configurations. A hop of 1.18 GHz to 1.24 GHz was observed (60 MHz). The resulting Q and insertion loss are 5.4 and 31 dB respectively, at both frequencies. Several simulations were performed to explain the results achieved. An extracted simulation replacing the MEMS capacitors with ideal capacitors (Figure 4-8c) showed the S_{21} response considering the actual inductors laid out. When fixed interconnect capacitance was

41

(a)

(b)

(c)

(d)
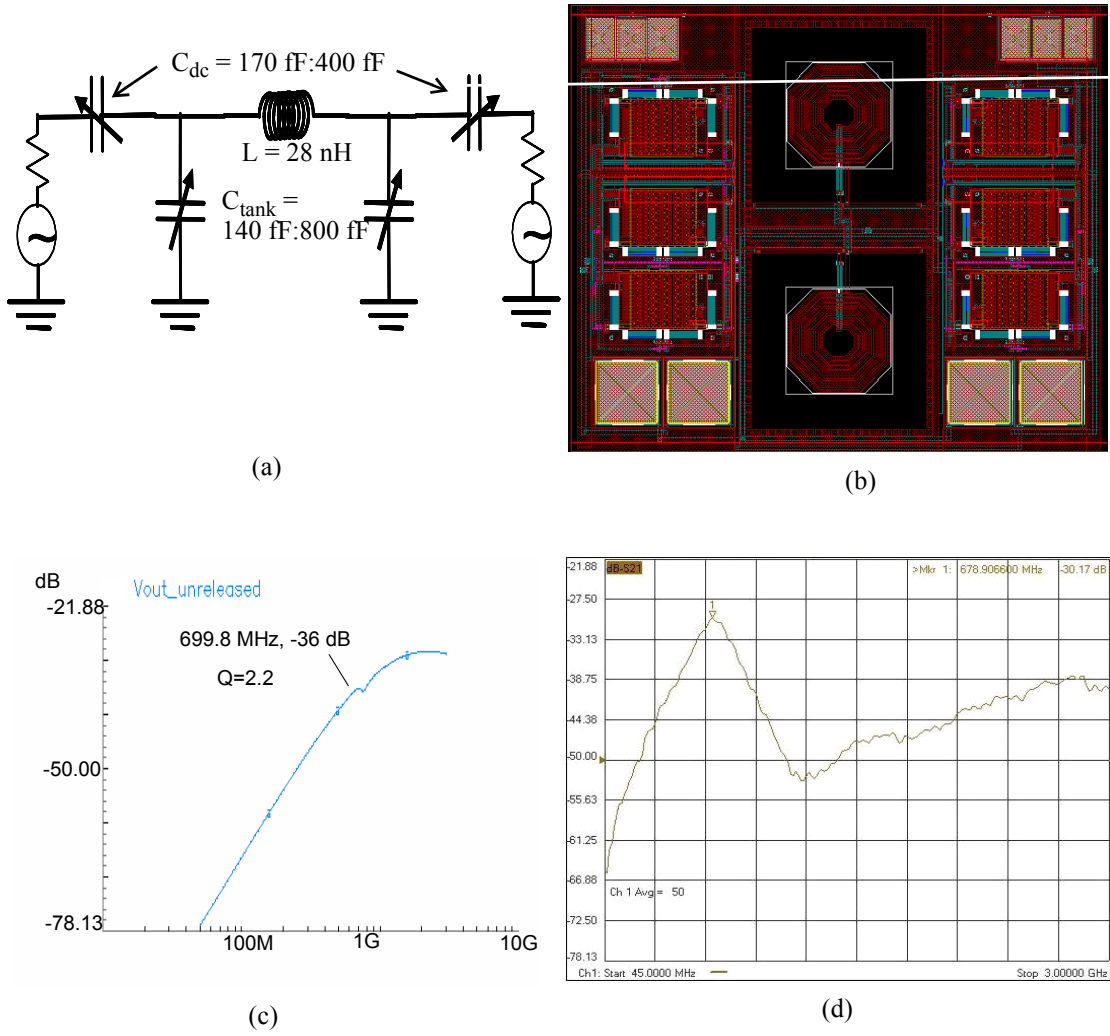
Figure 4-7. (a) Schematic showing design values. (b) Layout of filter. (c) Extracted simulation of S_{21} response of the Design A unreleased filter. (d) Measured S_{21} response for unreleased filter.

taken into account (Figure 4-8d), the center frequencies dropped to 889 MHz and 1.1 GHz, a narrower hop. The insertion loss increased significantly as well. Finally, Figure 4-8e shows the response when the designed capacitance values were replaced with measured capacitance values, giving center frequencies of 931 MHz and 964 MHz, a hop closer to that measured. These simulations showed that fixed interconnect capacitance is a significant factor to consider in the design process. The higher resonant frequencies after release could be attributed to the removal of parasitic capacitances to substrate in the MEMS inductor and capacitor that increased the overall operating frequency range.
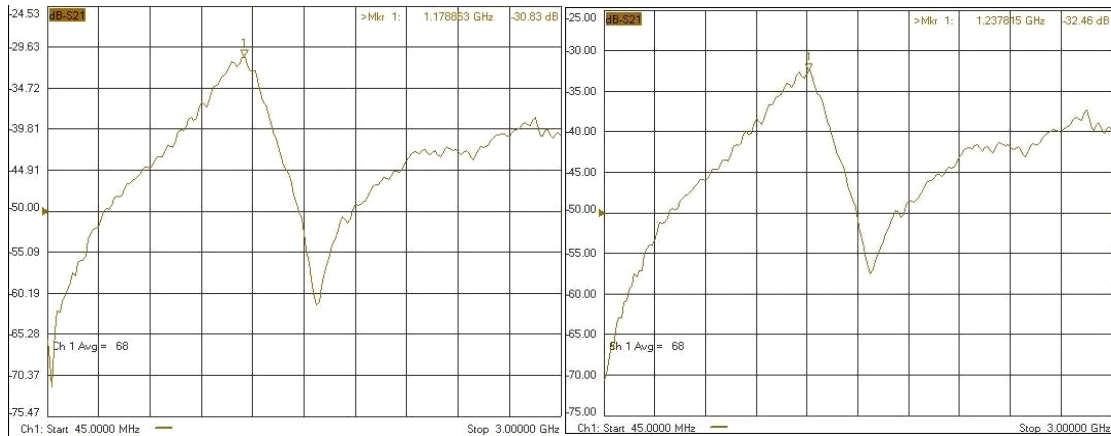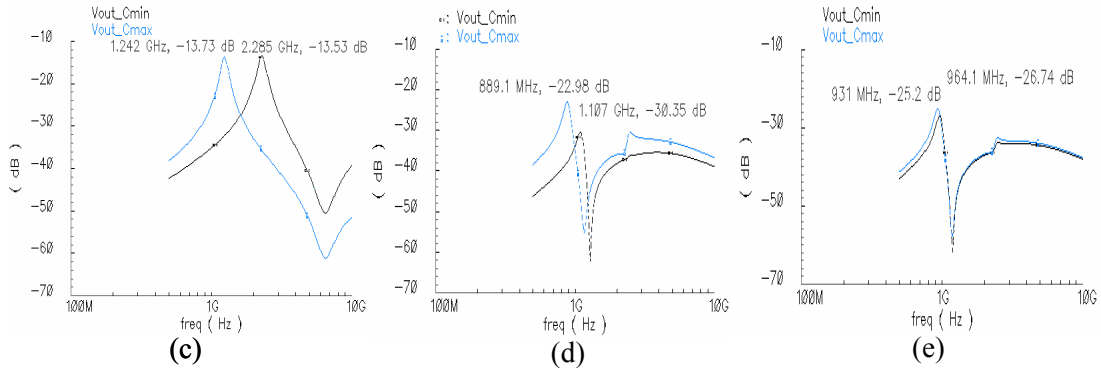
Figure 4-8. (a) S_{21} response of measured Design A filter after release, at both capacitor configurations. (b) Extracted simulation using ideal capacitors (c) Extracted simulation including fixed interconnect capacitance. (d) Simulation from (c), and replacing designed capacitance values with measured capacitance values.

4.2.2 Design B

One goal of this design was to ensure better insertion loss by taking into account fixed sources of capacitance (interconnect) in the design process. A second goal was to obtain a higher frequency-hopping range by incorporating finger-design capacitors. Because a higher capacitance ratio was expected with these capacitors, a 2.4 GHz to 5.2 GHz frequency hop was designed. A symmetrical inductor of 2 nH was chosen to ensure Q-improvement after release (Figure 4-9a), and dimensions were fixed according to the design procedure in Chapter 3. As a MEMS capacitor model did not exist during the design process, ideal capacitors were used in simulation, both for C_{dc} and C_{tank}, as well as for the fixed interconnect capacitance, to obtain the final design (Figure 4-9b). The total estimated interconnect capacitance was 130 fF. Assuming that the layout view (Figure 4-9c) of the capacitors was at the minimum capacitance state, the unreleased

43

S_{21} response was simulated, incorporating foundry inductors. Incorporating the lumped parameter MEMS inductor model, the simulated design showed lower insertion loss (3 dB better) (Figure 4-9d). MEMS capacitor reconfiguration switched the filter from 2.5 GHz to 6.3 GHz. At the minimum and maximum frequency, Q's of 6.1 and 13.4, and insertion losses of 7.3 and 10.8 dB were obtained.
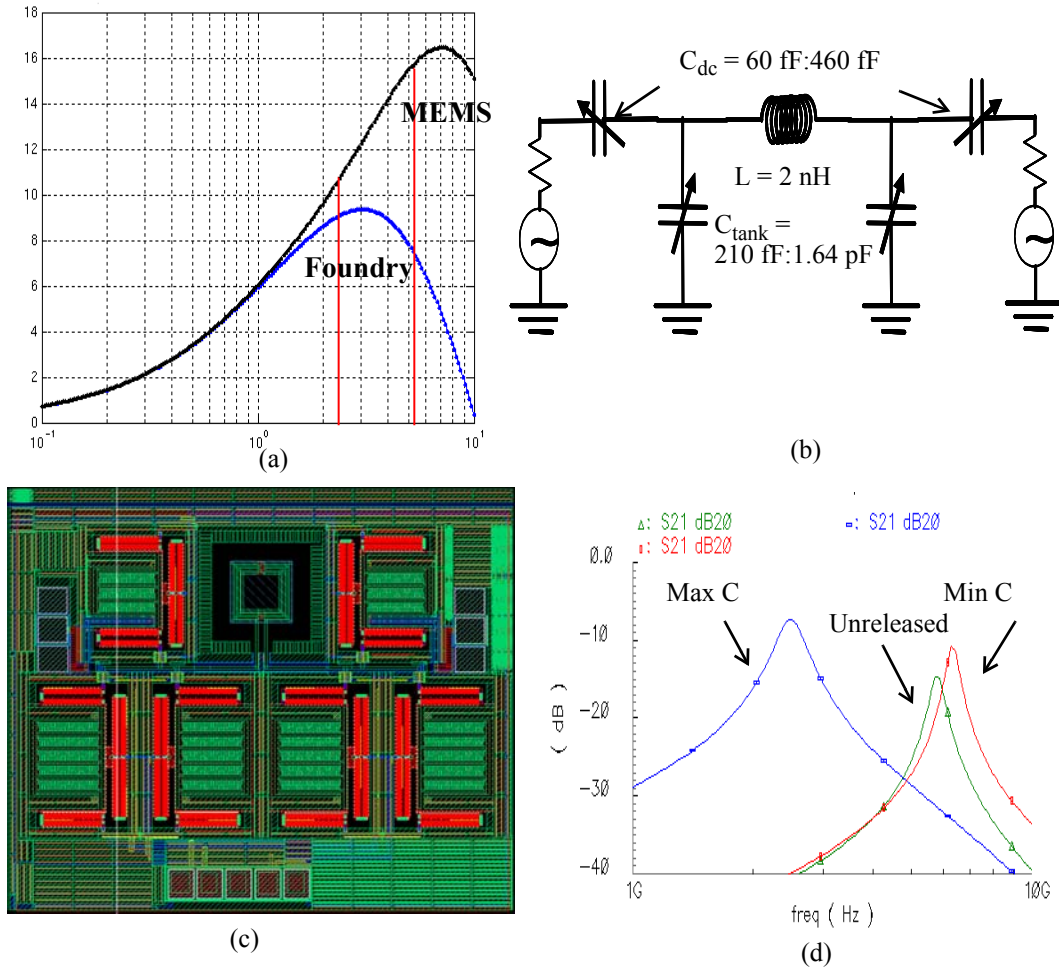
Figure 4-9. (a) Q vs frequency for 2-nH symmetrical inductor using lumped-parameter models before and after release. (b) Design B schematic showing design values. (c) Layout of Design B filter. (d) S_{21} response of simulated filter before and after release, at both capacitor configurations.

Several chips were tested to take into account variation across chips due to post-processing. The filter with the largest measured hop is reported. Applying 4 volts on the latch to release it, the capacitors switched between maximum to minimum configuration with 0 or 4 V applied on the tuning actuators, respectively. The S_{21} response is shown in Figure 4-10a for the unreleased case, with 1.66 GHz resonance

and 45.4 dB insertion loss. Figure 4-10b and Figure 4-10c show the released case at the maximum and minimum capacitance configuration, respectively. A switch from 3.04 GHz to 3.47 GHz gave a 430 MHz hop. Due to the unintended minimum and maximum capacitance configurations explained in Chapter 2 for these 1st generation finger-design capacitors used, the intended capacitance values were not reached, and the frequency hop was much lower than expected. As can be seen, the insertion loss is quite high with 47.83 dB and 50.87 dB, and the Q is low at 2.6 and 2.7. Since the designed C_{tank}/C_{dc} ratio was not obtained after fabrication, the insertion loss suffered, which can explain the low insertion loss even after release. Another factor is the low Q (~5) of these capacitors (Chapter 2).

(a)
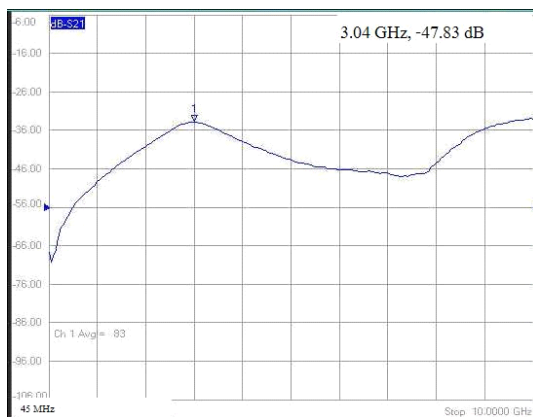
(b)
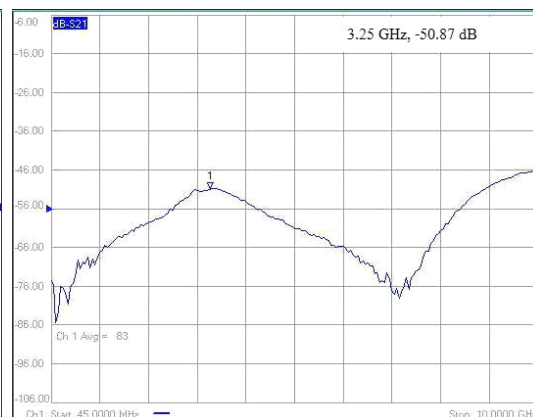
(c)

Figure 4-10. Measured s_{21} Design B response of filter when (a) unreleased (b) at maximum capacitance configuration (c) and at minimum capacitance configuration.

45

4.2.3 Design C

This third design was intended for frequency hopping achievable through the beam-design capacitor, with higher expected Q. A goal during this design process was to better predict the measurement results after micromachining, by taking into account fixed interconnect capacitance, the micromachined inductor, and by designing a more realistic frequency hop. The MEMS capacitors were again estimated as ideal, due to lack of design models during the design phase. The frequency hop chosen for this design was 1.7 GHz to 2.6 GHz. A conservative hop was chosen as the beam-design capacitor has a lower designed switching range than that of the finger-design capacitor. The inductor value was again chosen such that the Q value at the desired frequencies would improve with micromachining, namely, lie near the rise to peak Q. A second consideration was that the inductor value be high enough such that the small capacitors had high Q, as seen by the circuit model for capacitor Q (Appendix A), and low enough such that the capacitor size was realizable. A 6-nH inductor was chosen, and as seen by the Q plot in Figure 4-11a, the Q of the inductor potentially increases from 7 to 11.5 at 1.7 GHz (1.6X increase) and 4 to 13 at 2.6 GHz (3.2X increase).

An ideal filter Q specification of 10 or higher was set for this design. The estimated overall passive Q (see Section 3.1.2) was 10. This was arrived at by estimating capacitor Q as 40 from measured results in Figure 2-5, and inductor Q as 15 from measured results in Figure 4-4. Taking passive Q into account using (3.34), the filter Q becomes 5 or higher. For the operating frequency range, this translates to bandwidths around 400 MHz, a goal discussed in Section 3.2. With this range of Q, insertion losses less than 5 dB are achievable, another goal discussed in Section 3.2. Considering these goals, the design values and layout are shown in Figure 4-11b and Figure 4-11c, respectively.

In simulation it was assumed that the unreleased capacitor is in its minimum capacitance state. After release, the filter frequency with the capacitor in minimum capacitance state, increased due to the reduction in parasitic capacitance (Figure 4-11d). Another expected improvement in performance due to higher inductor Q was also seen, as the insertion loss improved by 3 dB. The simulation results obtained for Q were 6.5
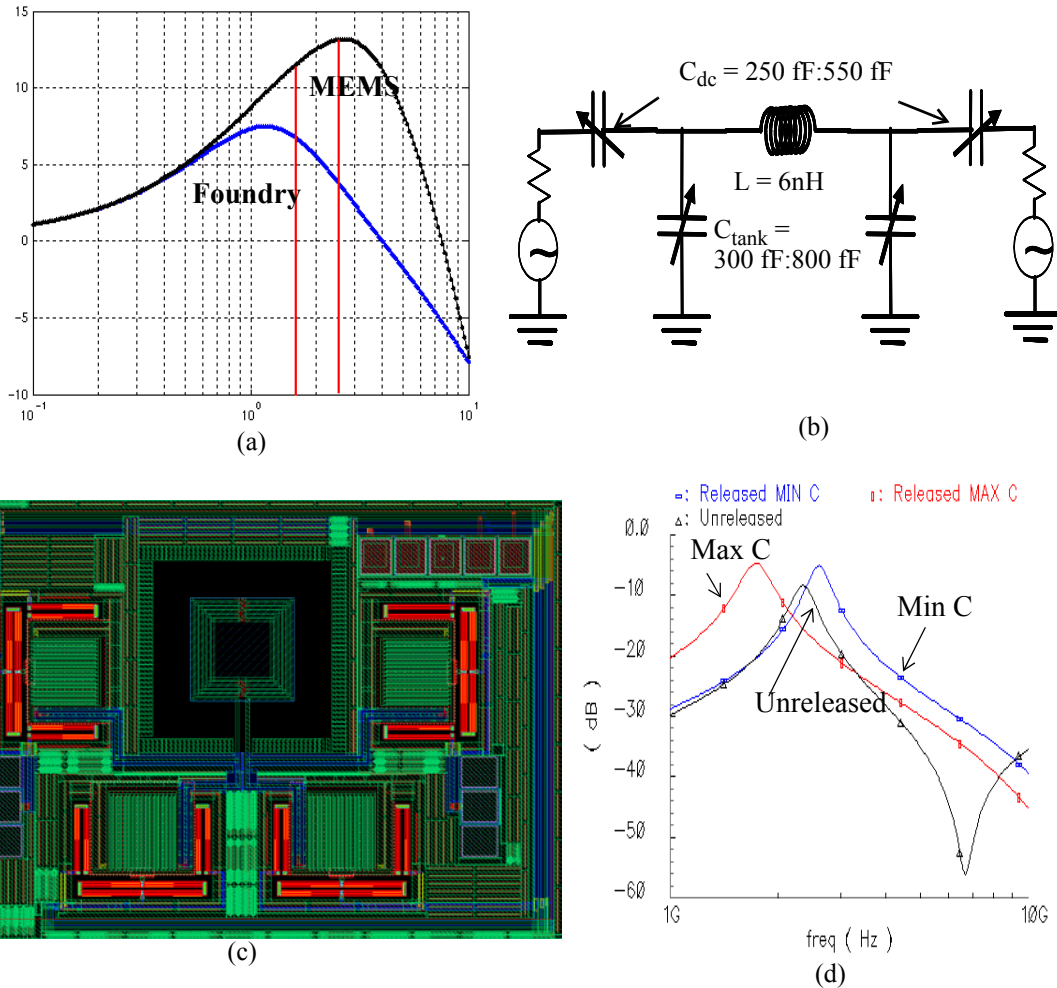
Figure 4-11. (a) Q vs frequency for 6-nH symmetrical inductor using lumped-parameter models, before and after release. (b) Design C schematic showing design values. (c) Layout of Design C filter. (d) S_{21} response of simulated filter before and after release, at both capacitor configurations.

for the unreleased case, 5.2 at the minimum frequency and 7.1 at the maximum frequency. Insertion losses of 8.3 dB, 4.7 dB, and 5.0 dB, respectively, were obtained.

Several filters of this design were tested due to variations across chips. Figure 4-12 shows the S_{21} response of one filter before release, and after release at the C_{max} and C_{min} configurations. A 490 MHz hop was observed from 1.87 GHz to 2.36 GHz, with insertion losses of 14.3 dB and 19.3 dB, respectively. The Q values were 4.4 and 9.5. In this filter, one of the tank capacitors did not release which increased the overall tank capacitance due to parasitics and increased insertion loss. The difference from the designed C_{tank}/C_{dc}

47

Figure 4-12. Measured S_{21} response of first Design C filter when (a) unreleased (b) at maximum capacitance configuration (c) and at minimum capacitance configuration.

ratio also increased the insertion loss. The increased capacitance lowered the frequency hopping range as well.

This is a possible explanation, as another Design C chip showed lower insertion loss and higher hop when all capacitors released. The measured results in Figure 4-13a and Figure 4-13b show this filter, with a 1.64 GHz to 2.36 GHz hop (720 MHz), and 6.6 dB and 10.2 dB insertion loss. Calibration was not performed before this measurement, however, resulting in the fluctuations on the curves.
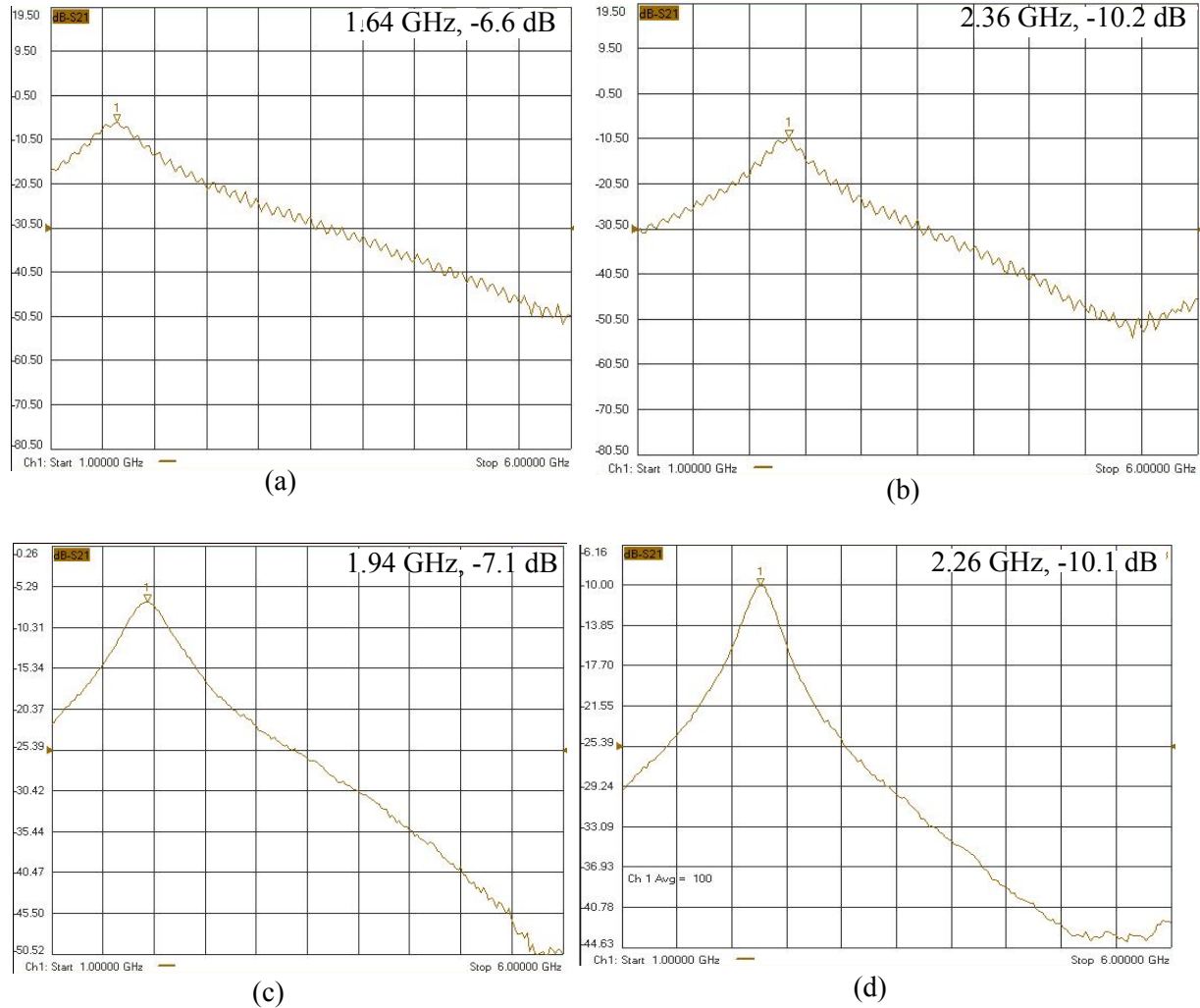
Figure 4-13. Measured S_{21} response for second and third Design C filters. (a) Shows second Design C filter at maximum capacitance configuration, (b) shows second Design C filter at minimum capacitance configuration, (c) shows third Design C filter at maximum capacitance configuration, (d) shows third Design C filter at minimum capacitance configuration.

A third Design C chip that was measured in which only two capacitors released. These measured results are shown in Figure 4-13c and Figure 4-13d. A frequency hop from 1.94 GHz to 2.26 GHz (320 MHz hop) and low insertion losses of 7.1 dB and 10.1 dB, respectively, were observed. The Q values were 7.8 and 5.5, respectively. Two of the capacitors did not release, which accounts for the narrower hop.

4.2.4 Design D

This fourth design was done using 2nd generation finger-design capacitors with larger gaps between fingers to allow them to engage. The specifications did not change from Design B, but different performance

49

was expected as the capacitor values had changed. No simulations were done on this design prior to tape-out, due to the limited design time. Only the layout was changed to increase the gap between the fingers.

The measured results are shown in Figure 4-14, before and after release. Before release the resonant frequency is 1.7 GHz, with an insertion loss of 40 dB. A wide hop of 2.6 GHz to 3.45 GHz was measured (850 MHz) after release. Insertion losses of 38.5 dB and 44.5 dB were obtained. The high insertion losses were expected for several reasons: one of the capacitors did not move, which changed the designed C_{tank}/C_{dc} ratio. Secondly, the capacitor Q was measured to be low (~5 as shown in Chapter 2).

(a)

(b)   (c)

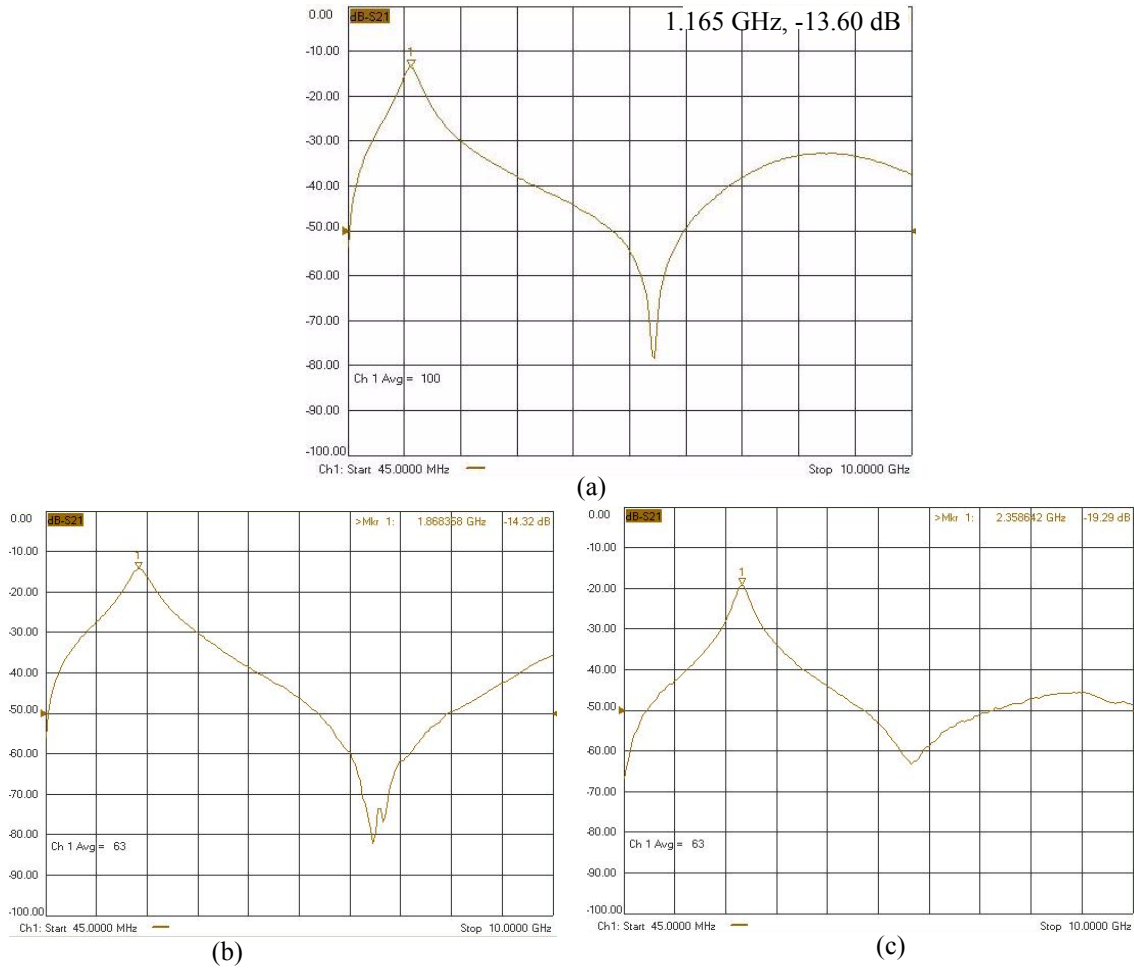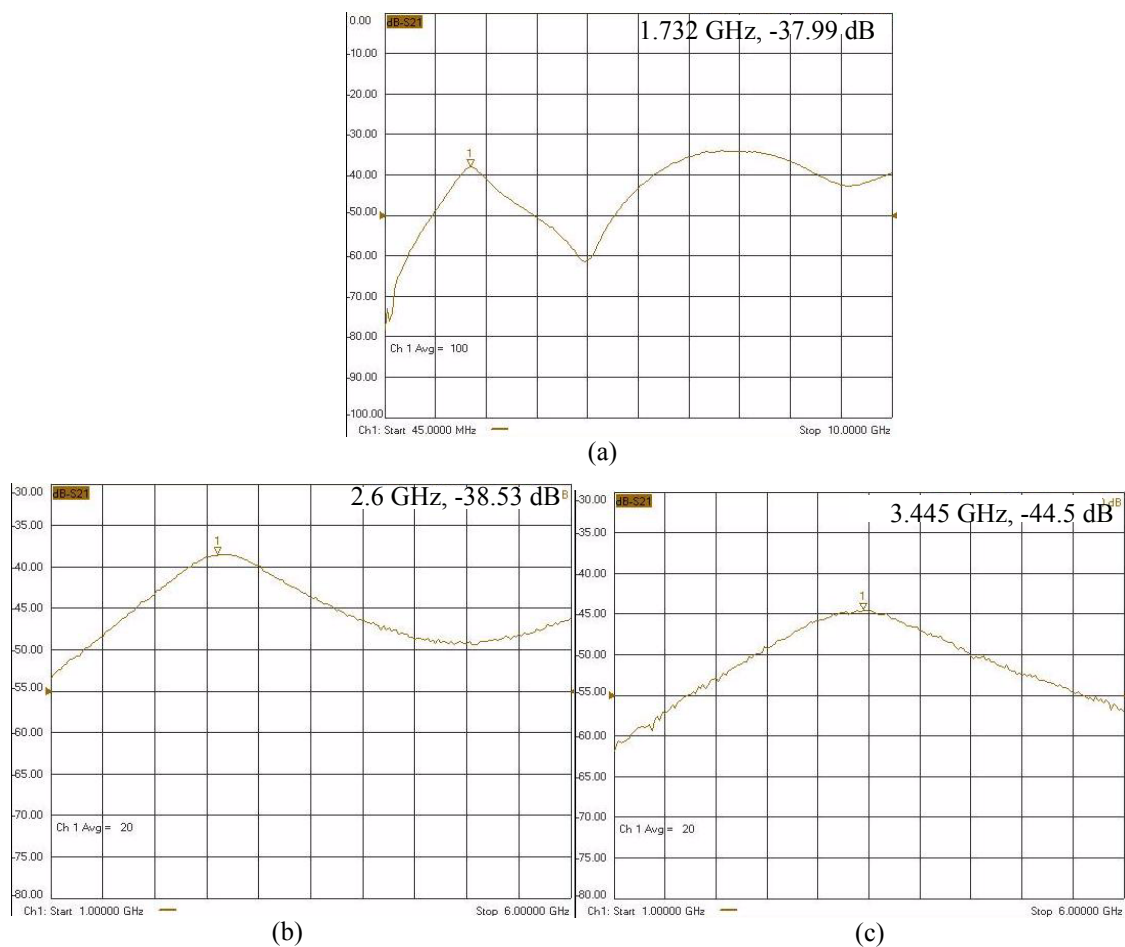**Figure 4-14.** Measured S_{21} response of Design D when (a) at maximum capacitance configuration (b) and at minimum capacitance configuration.

50

The following table summarizes the designs described above:

Table 4-2. Summary of fabricated designs described.

Design (Chip)	Microma-chined?	Center Freq.	Insertion Loss	Q	V_{ctl} Latch Max, Min C	Capacitor
Design A (IBM 6HP)	No	678.9 MHz	30 dB	2.8	~6 V ~0V, 6V	Beam
	Yes	1.18 GHz	31 dB	5.4		
		1.24 GHz	32 dB	5.4		
Design B (jz60_002)	No	1.67 GHz	45.4 dB	2.9	4 V 0V, 4V	Finger (1st generation)
	Yes	3.04 GHz	47.83 dB	2.6		
		3.47 GHz	50.87 dB	2.7		
Design C (1) (jz60_003)	No	1.17 GHz	13.6 dB	3.8	12 V 0V, 8.6V	Beam
	Yes	1.87 GHz	14.3 dB	4.4		
		2.36 GHz	19.3 dB	9.5		
Design C (2) (jz60_003)	Yes	1.64 GHz	6.6 dB	not measured	not recorded	Beam
		2.36 GHz	10.2 dB	not measured		
Design C (3) (jz60_003)	Yes	1.94 GHz	7.1 dB	7.8	not recorded	Beam
		2.26 GHz	10.1 dB	5.5		
Design D (jz60_006)	No	1.73 GHz	40.0 dB	3.9	~11 V 0V, 15 V	Finger (2nd generation)
	Yes	2.60 GHz	38.5 dB	2.7		
	Yes	3.45 GHz	44.5 dB	2.9		

5 Conclusions and Future Work

5.1 RF Frequency-Hopping Filter

This thesis describes the exploration of a passive filter topology that exhibits reconfigurability. The maximum achieved hopping range was 850 MHz, which is a wider range than that achievable using other common tuning CMOS tunable capacitors. Wider ranges are possible as many of the fabricated filters were limited by capacitors that did not release or did not move. The low yield of capacitors and time-consuming post-processing made it difficult to obtain a filter with all functional capacitors. The results so far however, show progress towards achieving reconfiguration above 1 GHz.

The choice of topology served the purpose of demonstrating the primary goal of reconfigurability. While several design steps were described to optimize this topology's performance, a topology that caters to lower insertion loss is desirable. The current topology has the limitation that there is a stronger dependence on C_{tank}/C_{dc} ratio for insertion loss rather than on passives Q. Since a lumped parameter model did not exist for the MEMS capacitors during most of the duration of this work, it was difficult to predict the final capacitance values after fabrication. There was also capacitance variation across chips due to differences in tunability and release. With these factors present, future designs could be made with a topology more robust with respect to insertion loss despite differences in element values. The contribution to insertion loss made by the finite Q of passives is still a design challenge, but micromachining inductors has proven to improve Q. Furthermore, models to predict micromachining improvements to Q have been developed that can aid in

future designs. Future work also includes development and application of a MEMS capacitor model.

5.2 Inductor Characterization

Micromachining inductors proved to enhance inductor behavior. Peak quality factor increased by more than 1.5 times, and self-resonant frequency increased, allowing a wider functional range. Several refinements to inductor characterization were made in this work, including substantiating a deembedding process, and obtaining models to predict micromachining effects.

The experiments described in this thesis can be extended for better characterization and comparison of different inductor geometries. Test structures with identical inductance values can be designed to compare all the geometries explored in this thesis, based on the conclusions made about deembedding and measurement processes. Other inductor topologies exist that have not yet been modeled or tested. A balun inductor has potentially high Q and micromachined baluns (already fabricated) can be tested and explored.

A better understanding of inductors can lead to improved circuit designs. Choice of size, metal width, spacing, diameter, etc. proved critical in obtaining desired and optimal circuit behavior. The study of inductor behavior across frequency leads to future considerations of not only increasing the peak Q, but also widening the frequency range across which maximum Q is exhibited. This challenge involves not only reducing the losses in the substrate, but also decreasing the current crowding effects.

Bibliography

[1] A. A. Abidi, "RF-CMOS Comes of Age", *IEEE Microwave Magazine,* vol. 4, issue 4, pp. 47-60, Dec. 2003.

[2] B. Razavi, "RF CMOS Transceivers for Cellular Telephony", *IEEE Communications Magazine,* pp. 144-149, Aug, 2003.

[3] P.R. Gray, R.G. Meyer, "Future Directions in Silicon ICs for RF Personal Communications" presented at Customs Integrated Conference, 1995.

[4] A. Oz, G. K. Fedder, "CMOS-Compatible RF-MEMS Tunable Capacitors", *2003 IEEE MTT-S Int. RFIC Symposium,* pp. 611-614.

[5] A. Oz, *CMOS/BiCMOS Self-assembling and Electrothermal Microactuators for Tunable Capacitors,* MS Thesis, Carnegie Mellon University, 2003. (http://www.ece.cmu.edu/~mems/pubs/)

[6] H. Lakdawala, X. Zhu, H. Luo, S. Santhanam, L. R. Carley, G. K. Fedder, "Micromachined High-Q Inductors in 0.18-μm Cu Interconnect Low-K CMOS", *IEEE J Solid-State Circuits,* SC-37(3), pp. 394-403, Mar. 2002.

[7] X. Zhu, D. W. Greve, G. K. Fedder, "Characterization of silicon isotropic etch by inductively coupled plasma in post-CMOS processing", *2000 IEEE MEMS*, pp. 568-573, 23-27 Jan. 2000.

[8] W.B. Kuhn, N. K. Yanduru, A.S. Wyszynski, "Q-Enhanced LC Bandpass Filters for Integrated Wireless Applications", *IEEE Trans. on Microwave Theory and Techniques,* vol. 46, no. 8, pp. 2577-2586, Dec. 1998.

[9] D. Li, Y. Tsividis, "Design Techniques for Automatically Tuned Integrated Gigahertz-Range Active LC Filters", *IEEE J Solid-State Circuits,* vol. 37, no. 8, pp. 967-977, Aug. 2002.

[10] D. Ramachandran, A. Oz, V.K. Saraf, G.K. Fedder, T. Mukherjee, "MEMS-enabled Reconfigurable VCO and RF Filter", *2004 IEEE Int. RFIC Symposium,* pp. 251-254, Dallas, TX, Jun. 2004.

[11] V.K. Saraf, D. Ramachandran, A. Oz, G.K. Fedder, T. Mukherjee, "Low Power LC-VCO using integrated MEMS Passives", *2004 IEEE Int. RFIC Symposium,* pp. 579-582, Dallas, TX, Jun. 2004.

[12] V.K. Saraf, "Low Power Wide Tuning Range LC-VCO using MEMS Passives", Masters Thesis, Carnegie Mellon University, Aug. 2004.

[13]   F. D. Bannon, J. R. Clark, C. T-C. Nguyen, "High-Q HF Microelectromechanical Filters", *IEEE J Solid-State Circuits,* vol. 35, no.4, pp. 512-526, Apr. 2000.

[14]   A. Oz, D. Ramachandran, V. K. Saraf, M. Sperling, G. K. Fedder, T. Mukherjee, "Toward a Wideband Frequency Hopping RF MEMS Receiver", 2003 *SRC SiGe Design Challenge: Team 29*, *Phase 2 Final Report,* Jul. 2003.

[15]   A. Oz, V. K. Saraf, D. Ramachandran, G. K. Fedder, T. Mukherjee, "Frequency Hopping Circuits Based on Reconfigurable MEMS Capacitors", *TECHCON 2003,* Dallas, TX, Aug. 2003.

[16]   R. Gharpurey, "Design Considerations in Wireless Front-Ends", http://engr.smu.edu/orgs/ssc/slides/ 20010130.pdf, Texas Instruments, Inc.

[17]   S. Mattisson, "Architecture and Technology for Multistandard Receivers", *IEEE BCTM 5.1*, pp. 82-85, 2001.

[18]   T. Soorapanth, S. S. Wong, "A 0-dB IL 2140 +- 30 MHz Bandpass Filter Utilizing Q-Enhanced Spiral Inductors in Standard CMOS", *IEEE J Solid-State Circuits*, vol. 37, no. 5, pp. 579-586, May 2002.

[19]   W.B. Kuhn, X. He, M. Mojaraddi, "Modeling Spiral Inductors in SOS Processes", *IEEE Trans on Electron Devices,* vol. 51, no. 5, May 2004.

[20]   C. P. Yue, S. S. Wong, "On-chip Spiral Inductors with Patterned Ground Shields for Si-Based RF ICs", *IEEE J Solid-State Circuits,* SC-33(5), pp. 743-752, May 1998.

[21]   H. A. C. Tilmans, W. De Raedt and E. Beyne, "MEMS for wireless communications: from RF-MEMS components to RF-MEMS-SiP," *J. Micromech. Microeng.* 13 (2003) S139–S163.

[22]   G. K. Fedder, S. Santhanam, M. L. Reed, S. C. Eagle, D. F. Guillou, M. S.-C. Lu, L. R. Carley, "Laminated High-Aspect-Ratio Microstructures in a Conventional CMOS Process", *Sensors & Actuators,* pp. 103-110, Mar. 1997.

[23]   O. Paul, P. Ruther, "Testing the Limits of Silicon Technology Based MEMS Materials", *Proceeding of 2003 IEEE Intl Symposium on Micromechatronics and Human Science,* pp. 1-9, 19-22 Oct. 2003.

[24]   J. Craninckx, M. S. J. Steyadrt, "A 1.8-GHz, Low Phase Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE J Solid-State Circuits,* vol.32, no. 5, pp. 736-744, May 1997.

[25]   W. B. Kuhn, N. M. Ibrahim, "Analysis of Current Crowding Effects in Multiturn Spiral Inductors", *IEEE Trans. on Microwave Theory and Techniques,* vol. 49, no. 1, pp. 31-38, Jan. 2001.

[26] W. B. Kuhn, N. K. Yandaru, "Spiral Inductor Substrate Loss Modeling in Silicon RFICs", *1998 IEEE Radio and Wireless Conference,* pp. 305-308, Aug 9-12, 1998.

[27] J. R. Long, M. A. Copeland, "The Modeling, Characterization and Design of Monolithic Inductors for Silicon RF IC's", *IEEE J Solid-State Circuits,* pp. 357-369, Mar. 1997.

[28] N. M. Nguyen, R. G. Meyer, "Si IC-compatible inductors and LC Passive Filters", *IEEE J Solid-State Circuits,* pp. 1028-1031, Aug. 1990.

[29] C. P. Yue, C. Ryu, J. Lau, T. H. Lee, S. S. Wong, "A Physical Model for Planar Spiral Inductors on Silicon", *Proc. IEEE Int. Electron Device Meetings,* pp. 155-158, 1996.

[30] F. Ling, V. Okhmatovski, W. Harris, S. McCraken, A. Dengi, "Large Scale, Broadband Parasitic Extraction for Fast Layout Verification for 3D for RF and Mixed Signal On-chip Structures," *IMS 2004,* Fort Worth, TX, Jun 6-11, 2004.

[31] BiCMOS-6HP Model Reference Guide, Dept. CL4V, RF/Analog Product Development, IBM Microelectronics Division, IBM Corporation, p. 241, 2002.

[32] M. Danesh, J. R. Long, "Differentially Driven Symmetric Microstrip Inductors", *IEEE Trans on Microwave Theory and Techniques,* vol. 50, no. 1, pp. 332-341, Jan. 2002.

[33] M. Danesh, J. R. Long, R. A. Hadaway, D. L. Harame, "A Q-Factor Enhancement Technique for MMIC Inductors", *1998 IEEE MTT-S Intl Microwave Symposium Digest,* vol. 1, 7-12, pp. 183-186, Jun. 1998.

[34] J. N. Burghartz, B. Rejaei, "On the Design of RF Spiral Inductors on Silicon", *IEEE Trans on Electron Devices,* vol. 50, no. 3, pp. 718-729, Mar. 2003.

[35] Y. Sun, J. K. Fidler, "Design Method for Impedance Matching Networks", *IEE Proc-Circuits Devices Syst.,* vol. 143, no. 4, pp. 186-194, Aug. 1996.

[36] Y. Sun, J. K. Fidler, "Practical Considerations of Impedance Matching Network Design", *IEE HF Radio Systems and Techniques,* Conference Publication no. 392, pp. 229-233, 4-7 July 1994.

[37] S. Orfanidis, "Electromagnetic Waves and Antennas", Rutgers University, New Jersey, 2004.

[38] U.S. Department of Commerce, National Telecommunications and Information Administration, Office of Spectrum Management, *United States Frequency Allocations: The Radio Spectrum*, http://www.ntia.doc.gov/osmhome/allochrt.pdf, Oct. 2003.

[39]   M. Koshino, K. Kanasaki, N. Akahori, M. Kawase, R. Chujyo, Y. Ebata, "A Wide-band Balanced SAW Filter with Longitudinal Multi-Mode Resonator", *IEEE Ultrasonics Symposium,* pp. 387-390, 2000.

[40]   B. Baidya, K. He, T. Mukherjee, "Layout Verification and Correction of CMOS-MEMS Layouts", *Technical Proceedings of the Fourth International Conference on Modeling and Simulation of Microsystems (MSM 2001),* pp. 426-429, Mar. 19-21, 2001, Hilton Head, SC.

[41]   I. Kwon, M. Je, K. Lee, H. Shin, *New RF MOSFET Small Signal SPICE Model*, 1984-2004 SIL-VACO   International,   https://src.silvaco.com/ResourceCenter/en/SimulationStandard/showArticle.jsp?year=2000&article=a3&month=apr.

[42]   T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, NY, 1998.

[43]   Franz Sischka, *Basics of S-Parameters part 1: Characterization Handbook*, Agilent, Mar. 18, 2002, http://eesof.tm.agilent.com/docs/iccap2002/MDLGBOOK/1MEASUREMENTS/3VNA/3SPAR/ 1SparBasics_1.pdf.

[44]   www.rfcafe.com, 1996-2004.

Appendix A: Analyzing RF Passives

A.1 Measuring Inductor S-Parameters

A macroscopic input-output behavior of a high-frequency circuit or device is commonly quantified using scattering parameters, or S-parameters. S-parameters are preferred over impedance parameters, or Z-parameters, since at high frequencies, impedances tend to vary, or oscillations or decaying occur when terminated by opens and shorts. S-parameters define input and output variables in terms of incident and reflected voltage waves, rather than port voltages or currents, using a characteristic impedance as a termination, rather than an open or short [42].

1.1.1 Single-Ended Inductors

1.1.1.1 Two-Port to One-Port S-Parameter Conversion

For the inductors measured in this thesis, two-port S-parameters were used to obtain Q and inductance. The test setup is seen in (Figure 1-1a). The two-port S-parameters were converted to one-port S-parameters, as the device characteristics of one port might be affected by the characteristic impedance of the opposite port [43]. Two-port relations (Figure 1-1b) may be defined as:
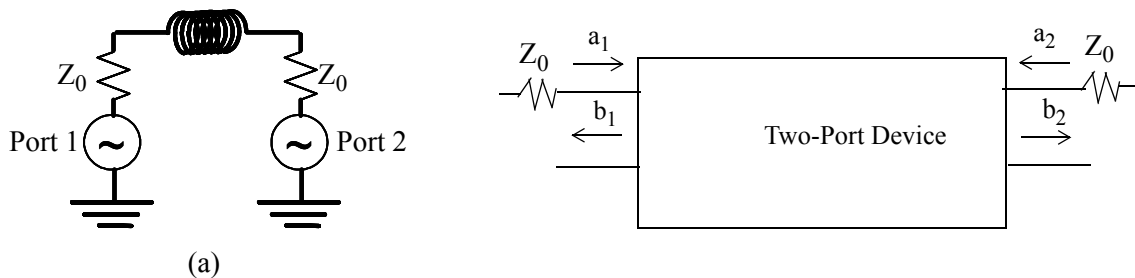
$$b_1 = S_{11}a_1 + S_{12}a_2$$

(A.1)

(a)

Figure 1-1. (a) Test setup for 2-port S-parameter measurement for inductor.

$$b_2 = S_{22}a_1 + S_{21}a_2$$

(A.2)

To convert to one-port, Port 2 can be defined to have the incident and reflected waves equal each other, such that there is only one port. This implies that

$$b_2 = -a_2$$

(A.3)

This leads to

$$S_{11oneport} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}}$$

(A.4)

1.1.1.2 Q and Inductance Extraction

Q is given by

$$Q = \frac{Im(Z_{11})}{Re(Z_{11})}$$

(A.5)

Based on Equation A.5, the one-port S-parameters should be converted to Z-parameters in order to obtain Q. This is done by the following conversion:

$$Z_{11oneport} = Z_0 \frac{1 + S_{11}}{1 - S_{11}}$$

(A.6)

Reactance/frequency, which is essentially inductance at low frequencies, can be calculated from

$$L = \frac{Im(Z_{11})}{\omega}$$

(A.7)

Similar analysis can be done for a capacitor. The quality factor for a capacitor is the negative of Equation A.5.

1.1.2 Differential Inductors

Using two-port s-parameters, the following calculation shows the response to a differential excitation [33]:

$$S_{dd} = S_{11} - S_{21}$$

<div align="right">(A.8)</div>

Then, S_{dd} is converted to z-parameters and multiplied by two, considering differential excitation:

$$Z_{dd} = 2Z_0 \frac{1 + S_{dd}}{1 - S_{dd}}$$

<div align="right">(A.9)</div>

Then, similar to a spiral inductor, Q and inductance can be formulated from the impedance Z_{dd}.

A.2 Passives Quality Factor

A simplified model of loss for an inductor or capacitor is either a series or parallel resistance. Based on these circuit models, formulae for Q can be derived. Q, by definition, is

$$Q \equiv \omega \frac{\text{energy stored}}{\text{average power dissipated}}$$

<div align="right">(A.10)</div>

In the inductor or capacitor lumped-parameter model, energy is stored by either inductance or capacitance (imaginary components), and power is dissipated through resistance (real components). Letting Z be the impedance of the model, Q can also be represented as

$$Q \equiv \frac{Im(Z)}{Re(Z)}$$

<div align="right">(A.11)</div>

Using this definition, Q of an inductor with loss represented as a series resistance R_{sind} is written below:

$$Q_{ind} = \frac{\omega L_s}{R_{sind}}$$

<div align="right">(A.12)</div>

The series model can be converted to a parallel model by doing the following series-to-parallel transformation, where L_p and R_{pind} are in parallel:

$$R_{pind} = R_{sind}(Q_{ind}^2 + 1)$$

<div align="right">(A.13)</div>

$$L_p = L_s \frac{Q_{ind}^2}{Q_{ind}^2 + 1} \approx L_s$$

<div align="right">(A.14)</div>

Substituting for the series variables R_{sind} and L_s leads to Q_{ind} for an inductor with parallel resistance:

$$Q_{ind} = \frac{R_{pind}}{\omega L_p}$$

<div align="right">(A.15)</div>

Similar equations can be formulated for a lossy capacitor. The Q of a capacitor with series resistance is given by

$$Q_{cap} = \frac{1}{\omega C_s R_{scap}}$$

<div align="right">(A.16)</div>

Series-to-parallel transformations for a capacitor are

$$R_{pcap} = R_{scap}(Q_{cap}^2 + 1)$$

<div align="right">(A.17)</div>

$$C_p = C_s \frac{Q_{cap}^2}{Q_{cap}^2 + 1} \approx C_s$$

<div align="right">(A.18)</div>

After substitution, Q_{cap} can be rewritten for a capacitor with parallel resistance:

$$Q_{cap} = \omega R_{pcap} C_p$$

<div align="right">(A.19)</div>

Appendix B:Y-Parameter Deembedding

Y-parameter deembedding [41][44] can be used to deembed pads and other routing wires for inductors in measurement. This procedure requires open and short deembedding structures to be laid out on chip.

B.1 Y-Parameter Deembedding Procedure

Following is the procedure to deembed open and short structures from a two-port inductor.

1. Measured two-port, S-parameters (in $Re(S_{ij}) + jIm(S_{ij})$ format) for the inductor (S_{ijD}), open structure (S_{ijO}), and short structure (S_{ijS}) are converted to Y-parameters using the following formulas. Here, R_0 is the port resistance, or 50 Ω.

$$Y_{11} = \frac{1}{R_0} \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

(B.1)

$$Y_{21} = \frac{1}{R_0} \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

(B.2)

$$Y_{12} = \frac{1}{R_0} \frac{-2S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

(B.3)

$$Y_{22} = \frac{1}{R_0} \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}$$

(B.4)

2. Subtract open structure Y-parameters from inductor Y-parameters to give Y_{ijDO}.

3. Subtract open structure Y-parameters from short structure Y-parameters to give Y_{ijSO}.

4. Convert Y_{ijDO} and Y_{ijSO} to Z-parameters (Z_{ijDO} and Z_{ijSO}, respectively) using the following formulas:

$$Z_{11} = \frac{Y_{22}}{Y_{11}Y_{22} - Y_{12}Y_{21}}$$

(B.5)

$$Z_{21} = \frac{-Y_{21}}{Y_{11}Y_{22} - Y_{12}Y_{21}}$$

(B.6)

$$Z_{12} = \frac{-Y_{12}}{Y_{11}Y_{22} - Y_{12}Y_{21}}$$

(B.7)

$$Z_{22} = \frac{Y_{11}}{Y_{11}Y_{22} - Y_{12}Y_{21}}$$

(B.8)

5. Compute $Z_{ijF} = Z_{ijDO} - Z_{ijSO}$.

6. Convert Z_{ijF} to Y-parameters Y_{ijF} using

$$Y_{11} = \frac{Z_{22}}{Z_{11}Z_{22} - Z_{12}Z_{21}}$$

(B.9)

$$Y_{21} = \frac{-Z_{21}}{Z_{11}Z_{22} - Z_{12}Z_{21}}$$

(B.10)

$$Y_{12} = \frac{-Z_{12}}{Z_{11}Z_{22} - Z_{12}Z_{21}}$$

(B.11)

$$Y_{22} = \frac{Z_{11}}{Z_{11}Z_{22} - Z_{12}Z_{21}}$$

(B.12)

7. Convert Y_{ijF} to S-parameters, S_{ijF}:

$$S_{11} = \frac{(G_0 - Y_{11})(G_0 + Y_{22}) + Y_{12}Y_{21}}{(G_0 + Y_{11})(G_0 + Y_{22}) - Y_{12}Y_{21}}$$

(B.13)

$$S_{21} = \frac{-2Y_{21}G_0}{(G_0 + Y_{11})(G_0 + Y_{22}) - Y_{12}Y_{21}}$$

(B.14)

$$S_{12} = \frac{-2Y_{12}G_0}{(G_0 + Y_{11})(G_0 + Y_{22}) - Y_{12}Y_{21}}$$

(B.15)

$$S_{22} = \frac{(G_0 + Y_{11})(G_0 - Y_{22}) + Y_{12}Y_{21}}{(G_0 + Y_{11})(G_0 + Y_{22}) - Y_{12}Y_{21}}$$

(B.16)

For only open deembedding, Y_{ijDO} can be directly converted to S-parameters. Deembedded

S-parameters can then be processed to obtain inductance and Q as described in Appendix A.