SiGe BiCMOS RF Circuit Design: A Wideband LNA Example

by

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TABLE OF CONTENTS

Abstract

A wideband amplifier with 15 dB gain and a 3-dB bandwidth of 2.8 GHz implemented in an advanced SiGe bipolar technology is presented. The noise figure is less than 4.4 dB while dissipating only 16 mW from a 2.5-V supply. The resulting figure of merit Gain / (Power * Noise Figure) of 0.213 exceeds those of recently published SiGe and RFCMOS wideband designs. The architecture chosen is a noise-canceling topology with shunt resistive feedback for wideband matching to 50 Ohms. Finally, the importance of modeling test bed parasitics is emphasized in the context of RF circuit design.

4

I. Introduction

Design of circuits at RF frequencies differs slightly from that of classical analog components. RF specifications such as input and output matching, as well as higher sensitivity to coupling and testing losses require new design methodologies that address these issues in a logical manner. Contained in this paper is one such methodology in the context of SiGe technology, where dramatic tradeoffs must be made during transistor choice and sizing. Test board parasitics can be a limiting factor in the circuit performance and care must be taken during simulation to model all chip signals. This methodology will be explored through the example of a wideband low noise amplifier in two different SiGe technologies.

Wideband Low Noise Amplifiers (LNAs) have several applications in emerging broadband communications systems such as multi-band mobile terminals and base stations. RFCMOS wideband LNAs have been reported with good noise performance, but high power (about 35 mW) [1], low bandwidth [2] and low gain. GaAs wideband designs have shown exceptional noise figures down to 1.3 dB at frequencies up to 2 GHz and 2.5 dB at frequencies up to 6 GHz [3]. However, GaAs circuits typically cost two to four times more than SiGe circuits on a $/mm^2 basis [4]. A cheaper 80 GHz SiGe HBT based wideband LNA [5] acheived results similar to those of other wideband LNAs at frequencies up to 15 GHz, but used 24 mW of power with a large area due to an on-chip inductor. By combining the high f_T SiGe HBT and the inductorless architecture used in [1] a low power, low area, high bandwidth wideband LNA has been designed.

The topology chosen for the wideband LNA presented in this thesis is a common emitter amplifier with shunt feedback and active noise cancellation. Design for two different SiGe

technologies were completed. One has been fabricated with the measurements documented in this thesis. Simulation showed comparable results to other wideband designs, though testing showed degraded noise and bandwidth performance. Even so, the measured figure of merit Gain / (Power * Noise Figure) exceeds that of [1], [2] and [5]. Future work includes probe based testing (both bias and RF signals) as opposed to board level testing, and exploration of other topologies.

II. Circuit Design

II.1 Figures of Merit

In the receiver architecture of Figure 1, the LNA must amplify the signal from the antenna without degrading the signal to noise ratio significantly. This antenna signal can range from hundreds of nanovolts up to hundreds of millivolts and must be amplified linearly throughout this range. Furthermore the band-select and image-reject filters are typically realized as external components requiring 50 Ω impedance at both the input and output of the LNA (from page 126 of [6]). This rules out many common LNA topologies due to their inability to achieve this impedance, or to amplify over a range of frequencies without adding excess noise [7].
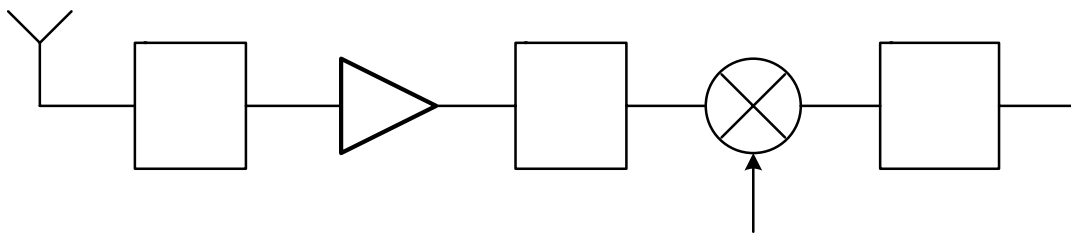
Figure 1. Heterodyne RF Receiver architecture (adapted from page 127 of [6])

II.2 Topology Choice & Design

II.2.A Common Emitter Design

One topology that can achieve the low impedances necessary for RF operation is the common emitter amplifier with shunt feedback shown in Figure 2(a). By applying KCL at the output node and applying an input voltage v_{IN} to the base of the transistor we get equation 1. If the designer

can guarantee a 50 Ω match to the source resistance R_S this voltage v_{IN} will be equal to half the source voltage v_S.

$$g_{m1} * v_{IN} \frac{r_\pi}{r_b + r_\pi} = \frac{v_{IN} - v_{OUT}}{R_F} - \frac{v_{OUT}}{r_O} \qquad \{1\}$$

Assuming that the physical base resistance (r_b) is much smaller than r_π (transistor current gain β divided by transconductance g_{m1}), the feedback resistance R_F is much smaller than the transistor output resistance r_O and β is large (such that $1/g_{m1}$ is much smaller than r_π) the input resistance is merely $1/g_{m1}$ and the unloaded gain v_{IN} / v_{OUT} is equal to $-(g_{m1}R_F - 1)$. In order to match the input impedance to the 50 Ω source impedance R_S, the transconductance g_{m1} is set to $1/R_S$, or 1/50 Ω. If the feedback resistor approaches the same magnitude as r_o, the small signal current will no longer completely flow through R_F and the input match will be degraded.

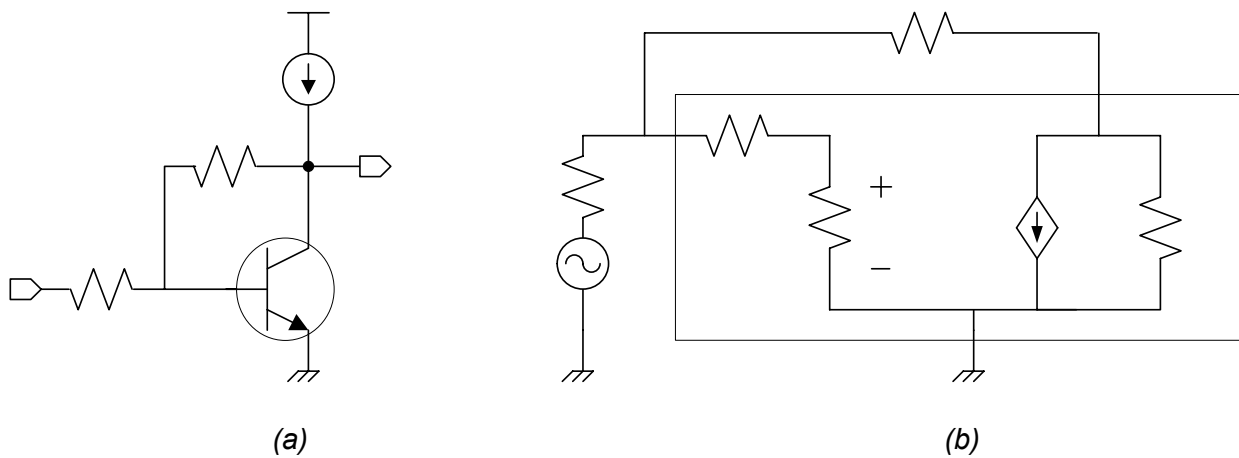*(a)*   *(b)*

Figure 2. Common Emitter with Shunt Feedback; Schematic (a) & Small Signal Model (b)

The output resistance of this stage can be computed by shorting v_S to ground and computing the impedance of the resistive network. Figure 3(a) shows this small signal circuit model for the
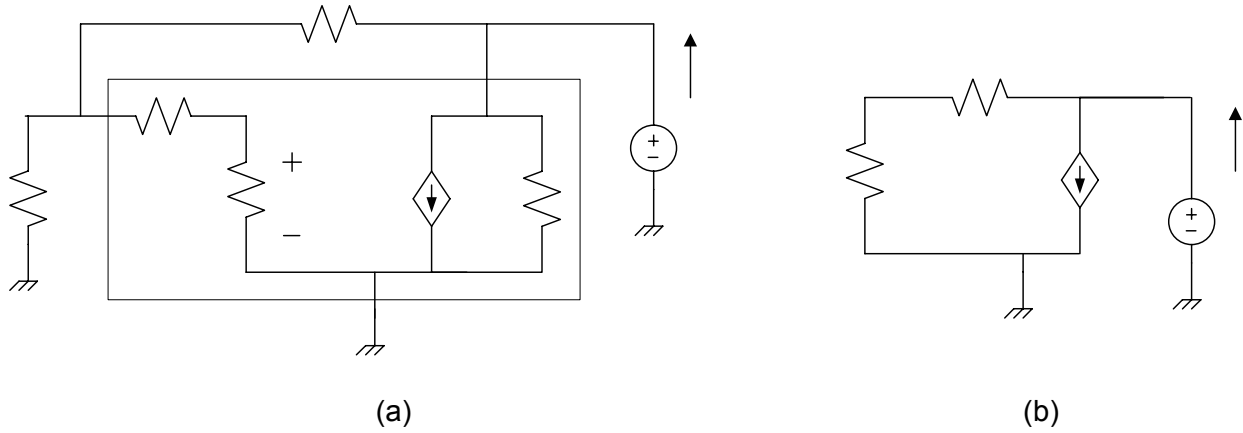
(a)   (b)

Figure 3 Output Impedance Circuit Model (a) and Simplification (b)

output impedance calculation. It is assumed that r_b is much smaller than r_π, R_S is much smaller

than r_π and r_o is much larger than the series combination of R_F and R_S. The circuit shown in

Figure 3(b) takes these assumptions into account. By placing a test voltage v_T on the output and

dividing by the resulting output current i_T the output resistance may be found. This current is

given by equation 2 where v_{IN} is equal to $v_T R_S / (R_F + R_S)$ because of the voltage divider nature

of R_F and R_S. Equation 3 gives the output impedance by solving equation 2 and dividing v_T by i_T

(note that g_{m1} equals $1/R_S$).

$$i_T = g_m v_{IN} + \frac{v_T}{R_F + R_S} = \frac{g_m v_T R_S}{R_F + R_S} + \frac{v_T}{R_F + R_S} = \frac{v_T}{R_F + R_S} + \frac{v_T}{R_F + R_S} \qquad \{2\}$$

$$i_T = \frac{2v_T}{R_F + R_S} \qquad \longrightarrow \qquad \frac{v_T}{i_T} = \frac{R_F + R_S}{2} = R_{OUT} \qquad \{3\}$$

A disadvantage of this architecture can be seen if matching to 50 Ω at the output is necessary.

R_F will be constrained to be 50 Ω, causing the circuit to have no gain. An approach to decouple

the output impedance from R_F will be discussed in section II.2.C.

9

II.2.B Noise Analysis of Shunt Feedback Stage

In addition to impedance matching and gain, the circuit noise of the shunt feedback stage is critical to its operation as an LNA. The noise of the circuit will be investigated by first identifying the various sources of noise. By superposition each noise source contributes independently to the total circuit noise. By referring these noise sources back to the input as noise voltages we may calculate the ratio of noise added by the circuit compared with the noise incident to the circuit from the 50 Ω input impedance, R_S (ratio also known as Noise Factor). The Noise Figure is the $\log_{10}$ of this ratio expressed in dB.
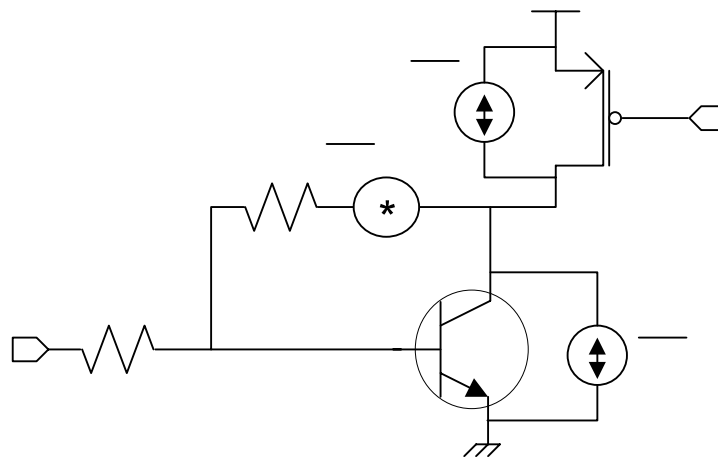

Figure 4. Sources of Noise in the Common Emitter with Shunt Feedback Topology

From Figure 4 it can be seen that the three sources of noise in this circuit are the thermal noise of the feedback resistor, the shot noise due to the collector current of transistor Q_1 and the thermal noise of the PFET current source P_1. These three noise sources are given by equations 4 (a), (b), and (c) respectively where k is Boltzman's constant, T is the temperature in Kelvin, Δf is the noise bandwidth, q is the electronic charge and γ is a parameter given by process and

channel length. The shot noise due to the base current is ignored as the collector noise will be β times larger. Also ignored is the PFET flicker noise due to the fact that the *1/f* nature of the flicker noise is negligible compared with the thermal noise at the frequencies of interest for this amplifier (GHz).

$$\overline{V_{n-R_F}}^2 = 4kT\Delta f R_F \qquad \overline{I_{n-Q_1}}^2 = 2qI_{C1}\Delta f \qquad \overline{I_{n-P}}^2 = 4kT\gamma g_{mPFET}\Delta f \qquad \{4\}$$

$\qquad\qquad$ (a) $\qquad\qquad\qquad\qquad\qquad$ (b) $\qquad\qquad\qquad\qquad\qquad$ (c)

In order to refer the noise sources back to the input v_{IN}, one must follow a four step approach. First, the noise sources must be converted into small signal sources. Next, the small signal transfer function from each small signal source to the output is calculated. This number is then squared and multiplied by the noise power of the noise source to find the noise power at the output. Finally this noise power is divided by the gain transfer function of the circuit to find the input referred noise for each source. Taking the summation of the input referred noises, the total input referred noise contributed by the circuit can be compared with the noise incident from the source resistance R_S. Presented below is an intuitive approach to this technique. Appendix sections A.I and A.II contains a more detailed approach in order to verify the correctness of the analysis. The small signal model is shown in Figure 5(a). If it is assumed that r_b is much smaller than r_π, R_S is much smaller than r_π and r_o is much larger than the series combination of R_F and R_S the circuit shown in Figure 5(b) is left.

11

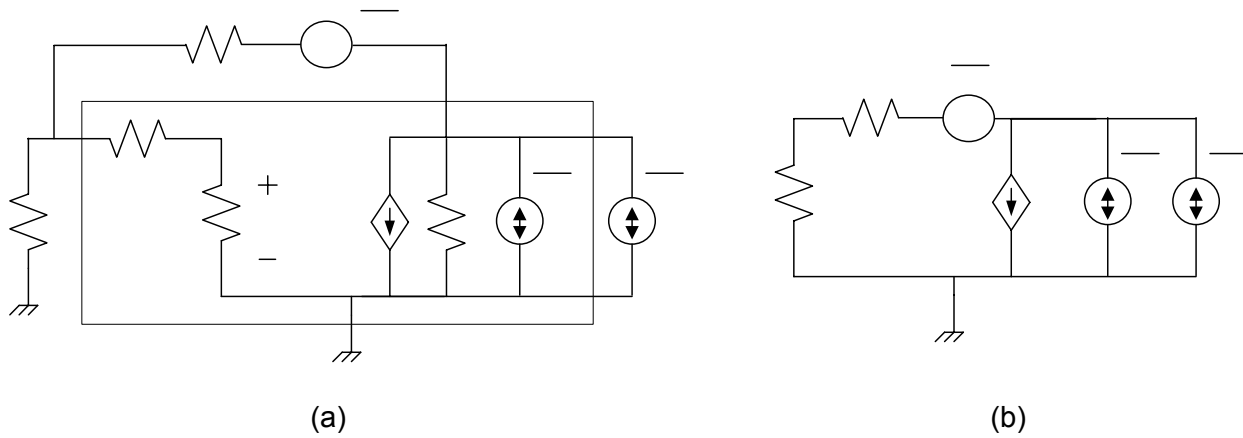(a)   (b)

Figure 5. Small signal circuit model including noise sources (a) and simplification (b)

Beginning the analysis with R_F, the two noise current sources from Q_1 and P_1 are ignored (by open circuiting them). Changing the noise source $\overline{V_{n\text{-}RF}}^2$ into a small signal source $v_{nss\text{-}RF}$ (where $_{nss}$ is a notation for noise small signal) the output voltage v_{OUT} equals $v_F + v_{nss\text{-}RF}$. Because of the feedback resistance there will be no current flowing through R_F or R_S (see Appendix section A.I) and v_F will equal zero volts. Therefore the output voltage will be equal to the small signal noise voltage source $v_{nss\text{-}RF}$. This is divided by the gain from section II.2.A of, $-(g_m R_F - 1)$ squared to refer the noise power to the input. The value of this input referred noise is given in equation 5 where g_{m1} is equal to $1/R_S$ and $R_F/R_S \gg 1$.

$$\overline{V_{ni-R_F}}^2 = \frac{4kT\Delta f R_F}{\left(g_{m1}R_F - 1\right)^2} \approx \frac{4kT\Delta f R_F}{\left(\dfrac{R_F}{R_S}\right)^2} = \frac{4kT\Delta f * R_S^2}{R_F} \qquad \{5\}$$

The noise currents from transistors P_1 and Q_1 are both connected from the output node to the small signal ground node, so the analysis for each source is identical. Converting the noise current sources $\overline{I_{n\text{-}Q1}}^2$ and $\overline{I_{n\text{-}P1}}^2$ to small signal current sources $i_{nss\text{-}Q1}$ and $i_{nss\text{-}P1}$ the output voltage is equal to these currents multiplied by the output resistance $(R_F + R_S) / 2$ from equation 3. So,

the output noise power is equal to the noise current sources multiplied by this output resistance squared. This is divided by the gain from section II.2.A of, $-(g_mR_F-1)$ squared to refer the noise power to the input. Equation 6 gives this value where *CS* refers to either noise current source, g_{m1} is equal to $1/R_S$ and $R_F/R_S >> 1$ (necessary for gain).

$$\overline{V_{ni-CS}}^2 = \frac{\overline{I_{n-CS}}^2(R_S + R_F)^2}{4(g_{m1}R_F - 1)^2} \approx \frac{\overline{I_{n-CS}}^2 * R_F^2}{4\left(\dfrac{R_F}{R_S}\right)^2} = \frac{\overline{I_{n-CS}}^2 * R_S^2}{4} \qquad \{6\}$$

Expanding from equation 6, equations 7 (a) and (b) contains the input referred noise voltages of Q_1 and P_1 respectively.

$$\overline{V_{ni-Q_1}}^2 = \frac{qI_{C1}\Delta f * R_S^2}{2} \qquad\qquad \overline{V_{ni-P_1}}^2 = kT\gamma g_{mPFET}\Delta f * R_S^2 \qquad \{7\}$$

<div align="center">(a)   (b)</div>

The total input referred noise is the sum of equations 5, 7(a) and 7(b) (from page 208 of [10]) and the resulting summation is used to compute the noise factor. The noise factor of a generic circuit is given by equation 8 where $\overline{V_{ni-Circuit}}^2$ is the total input referred noise at node v_{IN} and $\overline{V_{ni-Source}}^2$ is equal to $4kT\Delta fR_S$. This equation is expanded to the shunt feedback common emitter circuit by equation 9.

$$N.F. = \frac{\overline{V_{ni-Source}}^2 + \overline{V_{ni-Circuit}}^2}{\overline{V_{ni-Source}}^2} = \frac{4kT\Delta fR_S + \overline{V_{ni-Circuit}}^2}{4kT\Delta fR_S} = 1 + \frac{\overline{V_{ni-Circuit}}^2}{4kT\Delta fR_S} \qquad \{8\}$$

13

$$N.F. = 1 + \frac{\dfrac{4kT\Delta f R_S^{\ 2}}{R_F} + \dfrac{qI_{C1}\Delta f R_S^{\ 2}}{2} + kT\gamma g_{mPFET}\Delta f R_S^{\ 2}}{4kT\Delta f R_S} = 1 + \frac{R_S}{R_F} + \frac{I_{C1}R_S}{8V_T} + \frac{\gamma g_{mPFET}R_S}{4} \qquad \{9\}$$

From the above equation we may gain some intuition of how to minimize the noise. Assuming

that $R_F \gg R_S$ (needed for gain) the first term is negligible. The second term is effectively

reduces to $g_{m1}R_S / 8$ which will be fixed as g_{m1} is set by the input matching. The third term may

be minimized by decreasing the transconductance of transistor P_{Bias} by increasing the quantity

$V_{GS-P1} - V_{TH-P1}$. This will directly affect the linearity of the circuit as the maximum voltage swing is

equal to the supply voltage minus the drain to source saturation voltage (V_{DS-SAT}) of transistor

P_{Bias}. Concluding this discussion, the gain, input matching and linearity objectives prevent the

designer from reducing the noise of the shunt feedback common emitter amplifier.

II.2.C Second Stage

As discussed previously, the disadvantages of the shunt feedback common emitter amplifier

include the inability to simultaneously provide gain and a 50 Ω output impedance (see section

II.2.A) as well as the direct relationship between noise, gain, input matching and linearity (see

section II.2.B). Another stage must be added such the gain and the output impedance will be

decoupled from one another and also to decouple the noise, gain, linearity and input matching.

An emitter follower is one solution, able to provide a very low output impedance while passing

the signal from input to output with unity gain. Figure 6 shows a diagram of the emitter follower

with Q_3 as the emitter follower transistor and Q_2 as a fixed current source (biasing not shown).

C_{HP} and R_{HP} form a high pass filter that decouples the DC value from the first stage to the
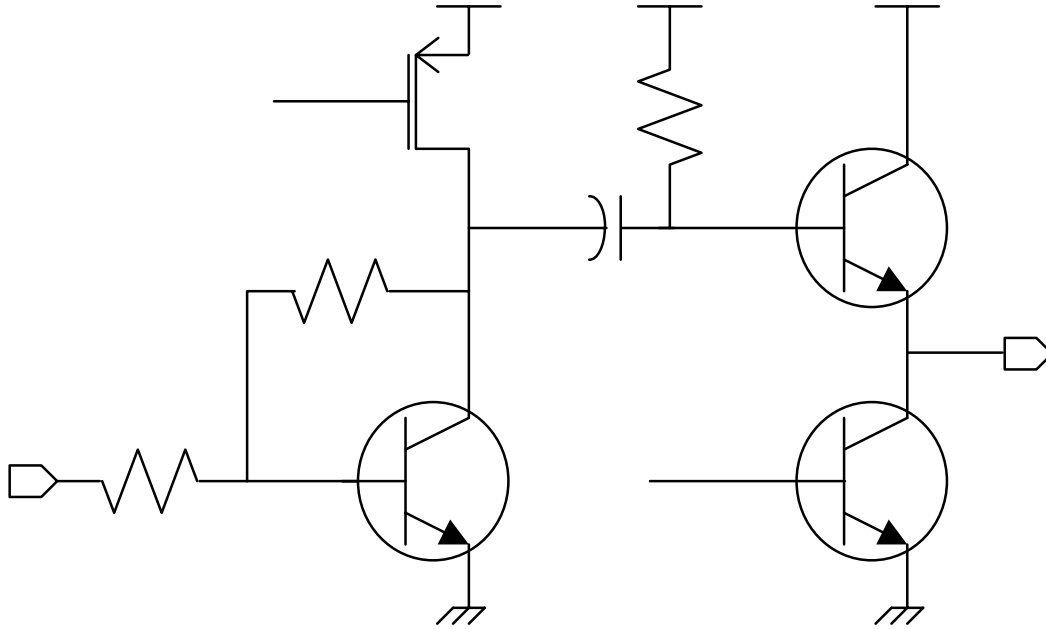
second stage.

Figure 6. Emitter Follower as Second Stage

A disadvantage of this second stage is that it will add even more noise to the circuit (see section II.2.E.i for noise analysis of the emitter follower second stage) without adding more gain. One approach to minimizing this noise is to take advantage of the resistive feedback and cancel the noise from the transistors Q_1 and P_1. Typically noise is only present at the output and the input referred noise is merely a model of the equivalent input noise that leads to the same output noise. The resistive feedback, however, causes the noise from transistors Q_1 and P_1 to appear at v_{IN} with an attenuation through R_F. The exact value of this attenuation can be taken from the small signal model of the first stage noise of Q_1 and P_1, seen in figure 5(b). R_F and R_S form a voltage divider and the equation for the relationship between v_{IN} and v_{OUT1} is given by equation 10.

$$v_{IN} = v_{OUT1} \frac{R_S}{R_F + R_S} \qquad \longrightarrow \qquad \frac{v_{OUT1}}{v_{IN}} = \frac{R_F}{R_S} + 1 \qquad \{10\}$$

$$V_S$$

$$R_S$$

Therefore the small signal noise currents experience an attenuation of $R_F/R_S + 1$ (hereafter referred to as A) from output to the base of transistor Q_1. This means that the physical noise voltage at v_{IN} will be *in phase* and completely correlated with the noise at v_{OUT1}. This is contrast to the gain of the source signal v_S, $-(g_{m1}R_F - 1)$ from v_{IN} to v_{OUT1} *(180° out of phase)* (see section II.2.A).
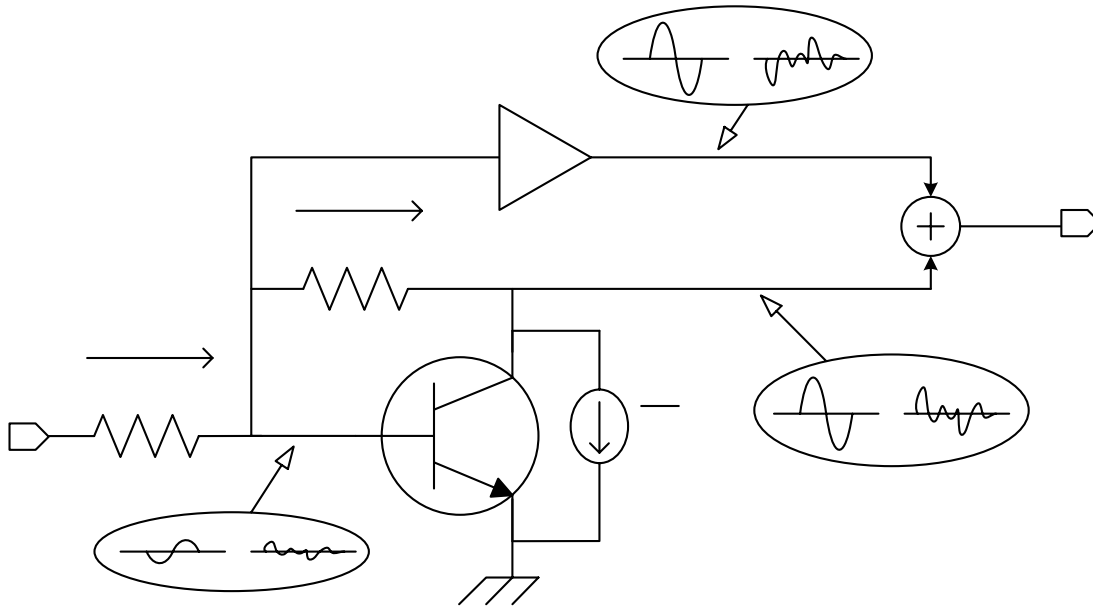

Figure 7. Noise Canceling Principle (adapted from [1])

We can take advantage of the phase difference to cancel the noise of the first stage. The principle can be illustrated with Figure 7 (adapted from [1]) where $\overline{I_n^2}$ models the total noise current from collector to emitter of Q_1. At node X (same as v_{OUT1} from Figure 6) there will be two waveforms: the input signal having gone through a gain of, $-(g_{m1}R_F - 1)$ and the output noise (equal to the noise at W multiplied by $+A$). If an ideal amplifier with a gain of $-A$ is connected to node W (same as v_{IN} from Figure 6), the two waveforms present at node Y will be: *input noise* -A* and the *input signal * -A*. Noise cancellation can occur if these waveforms at node Y are summed with those at node X. Node Z will contain only the signal, having gone through an

amplification of $-(g_{m1}R_F - 1) + -A$ or, setting g_{m1} equal to $1/R_S$ and A to equation 10, the gain equals $-(R_F/R_S - 1) + -(R_F/R_S + 1)$. This is more than twice the gain of the common emitter amplifier alone. Because the noise of Q_1 and P_{Bias} have been canceled the noise figure is dominated by the second amplifier (the noise from the summer is divided by the gain of the first stage when referred to the input, hence it is insignificant).

The topology from Figure 6 can be modified to include this noise canceling principle by connecting the base of transistor Q_2 to v_{IN} and adding a current source (I_{B2}) at the output for an extra degree of freedom when selecting transistor transconductance values. The topology for the second stage can now be seen in Figure 8(a) where v_X (previously named v_{OUT1}) is the output of the first stage and v_W is the input to the shunt feedback common emitter amplifier (previously named v_{IN}).

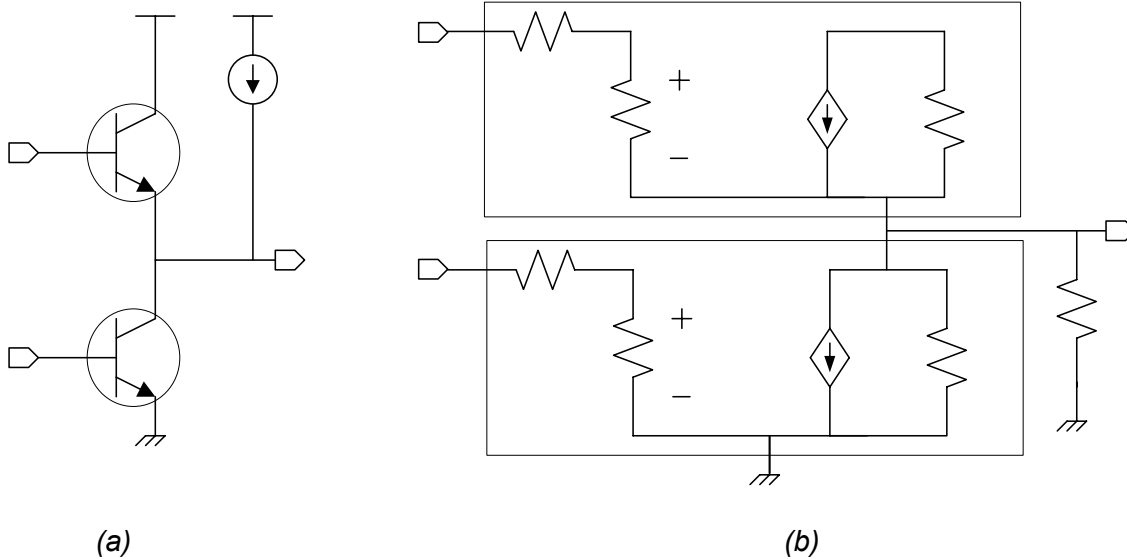
(a)   (b)

Figure 8. Amplifier/Summer Schematic (a) & Small Signal Model (b)

The output impedance is given by equation 11 where r_b has been ignored due to its low value compared to r_π and the output resistances of Q_2, Q_3 and I_{B2} are ignored due to their large value as compared to $1/g_{m3}$. Note that $r_{\pi3}$ is equal to, β / g_{m3}.

$$R_{OUT} = \frac{1}{g_{m3}} \| \frac{\beta}{g_{m3}} = \frac{1}{g_{m3}} * \frac{\beta}{\beta+1}$$ {11}

Since β is typically in the range of 50-200, the output impedance can be expressed as $1/g_{m3}$. The gain from the input of transistor Q_2 to the output is derived from equation 12 (KCL at the output with v_X shorted to AC ground). If it is assumed that r_b is much smaller than r_π, β is large (i.e. $r_{\pi3} >> 1/g_{m3}$) and $1/g_{m3}$ is much smaller than the parallel combination of r_{O2}, r_{O3} and r_{O-IB2} the gain reduces to $-g_{m2}/g_{m3}$. This is an intuitive answer as the gain of a common emitter amplifier is equal to $-g_m * R_{OUT}$ and $R_{OUT} = 1/g_{m3}$ from equation 11.

$$g_{m3} v_{OUT} * \left(\frac{r_{b3}}{r_{b3} + r_{\pi3}} - 1 \right) = g_{m2} v_W \frac{r_{\pi2}}{r_{b2} + r_{\pi2}} + \frac{v_O}{r_{b3} + r_{\pi3}} + \frac{v_O}{r_{O2}} + \frac{v_O}{r_{O3}} + \frac{v_O}{r_{O-IB2}}$$ {12}

In order to set the gain to be equal to $-A$ as derived by the analysis of figure 7, the ratio g_{m2}/g_{m3} is set to be equal to A. This is accomplished by sizing transistor Q_2 to $A*Q_1$ such that it pulls A times the current. This can be done by either increasing the emitter width or by connecting A transistors in parallel. This second method was used for better matching during layout. The current source I_{B2} robs current from Q_3, lowering it's g_{m3} and simultaneously helps in matching to the output impedance.

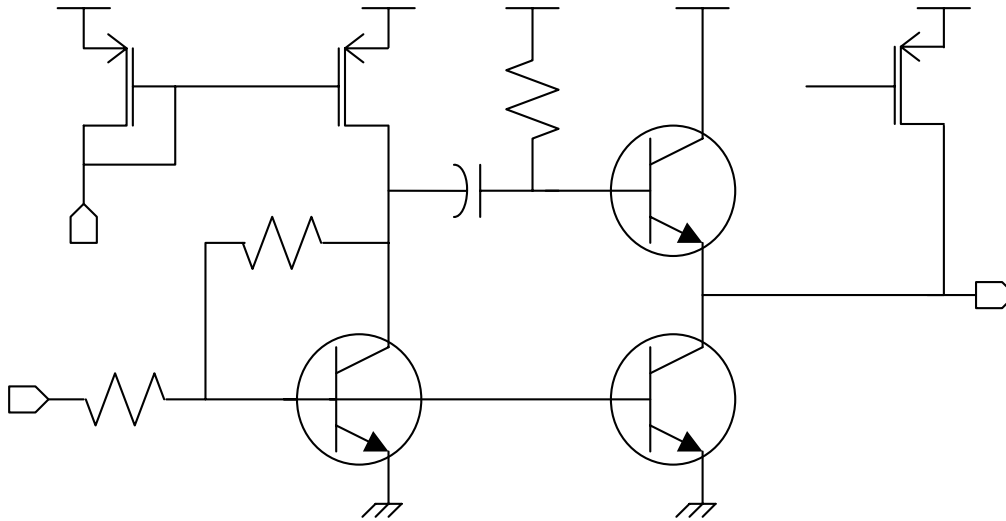## II.2.D Overall Topology

Figure 9. Final Topology

The circuit shown in Figure 9 is the incorporation of all the ideas in Sections II.2.A through

II.2.C. The gain is equal to the summation of the first stage gain, $- (g_{m1}R_F - 1)$ and second stage

gain, $-g_{m2}/g_{m3}$. Therefore the total gain is, $- \{(g_{m1}R_F - 1) + g_{m2}/g_{m3}\}$. The current sources are

implemented as PFET current mirrors, where P_2 is sized (A-1) times larger than P_1. The bias

current is provided by an off-chip resistor (see section III.3), enabling post-fabrication

modification of the bias current.

II.2.E Noise Comparison of Second Stages

A comparison of the final topology found in figure 9 to the topology found in figure 6 is

necessary to determine the overall improvement of noise performance by using the noise

canceling principle. The noise factor of each amplifier will be computed intuitively in this section,

19

with detailed analysis found in the appendix. These two noise factors will be compared against each other to highlight the differences between the two topologies.

II.2.E.i Second Stage with Emitter Follower and Current Source Load

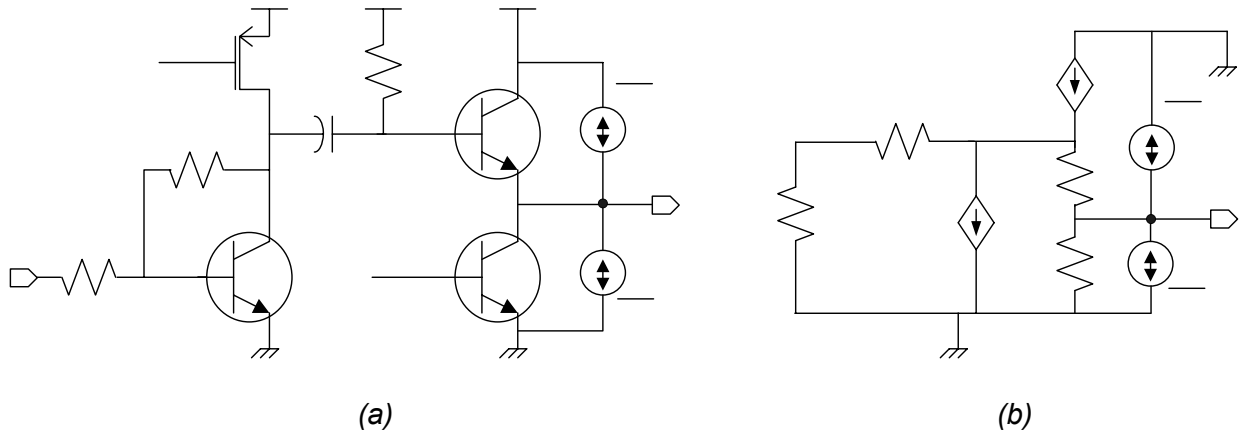(a)   (b)

Figure 10. Noise Sources in Original Second Stage Topology:

schematic (a) and small signal model (b)

The main noise sources contributed by the second stage in the original emitter follower with current source load topology from figure 6 are the shot currents of transistors Q_2 and Q_3, as seen in Figure 10(a). The resulting small signal model is shown in Figure 10(b) where the t-model is used for transistor Q_3 and an output resistance r_{o2} is used to model current source transistor Q_2. It can be seen that the two shot noise sources are in parallel with each other and are thus referred to the input in the same manner.

Changing the noise current sources $\overline{I_{n\text{-}Q2}}^2$ and $\overline{I_{n\text{-}Q3}}^2$ to small signal current sources $i_{nss\text{-}Q2}$ and $i_{nss\text{-}Q3}$ the noise transfer function is equal to these small signal currents multiplied by the output impedance $1/g_{m3}$ (from equation 11). The output noise power is therefore the noise current source power multiplied by $1/g_{m3}^2$. To find the input referred noise voltage, this value is divided

by the gain squared of the circuit, equal to the gain of the first stage, $-(g_{m1}R_F-1)$ squared. This is due to the fact that the gain of the second stage emitter follower is unity (see section II.2.C). For full analysis see Appendix section A.III. The resulting input referred noise voltages are given in equations 13 (a) and (b) for the shot noises from Q_2 and Q_3 respectively.

$$\overline{V_{ni-Q_2}}^2 = \frac{2qI_{C2}\Delta f}{g_{m3}^2 * (g_{m1}R_F - 1)^2} \qquad\qquad \overline{V_{ni-Q_3}}^2 = \frac{2qI_{C3}\Delta f}{g_{m3}^2 * (g_{m1}R_F - 1)^2} \qquad\qquad \{13\}$$

(a)   (b)

Because both g_{m1} and g_{m3} are constrained to be $1/50\ \Omega$ or $1/R_S$ due to impedance matching, the denominators from equations 13 (a) and (b) are equal to $(R_F - R_S)^2 * 1/R_S^4$. Assuming $R_F \gg R_S$ (needed for gain), the simplified noise voltages are given in equations 14 (a) and (b) for the shot noises from Q_2 and Q_3 respectively.

$$\overline{V_{ni-Q_2}}^2 = \frac{2qI_{C2}\Delta f * R_S^4}{R_F^2} \qquad\qquad \overline{V_{ni-Q_3}}^2 = \frac{2qI_{C3}\Delta f * R_S^4}{R_F^2} \qquad\qquad \{14\}$$

(a)   (b)

Combining these terms with the input referred noise voltages of the first stage (from equations 5 and 7) the noise factor of the amplifier is computed by adding and then dividing by the source resistance noise power $4kT\Delta fR_S$. Using the generic noise factor equation from equation 8, the noise factor of the amplifier with emitter follower second stage is given by equation 15. The Noise Figure is the $\log_{10}$ of this ratio in dB.

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{I_{C1}R_S}{8V_T} + \frac{\gamma g_{mPFET}R_S}{4} + \frac{I_{C2}R_S^3}{2V_TR_F^2} + \frac{I_{C3}R_S^3}{2V_TR_F^2} \qquad\qquad \{15\}$$

21

Substituting $I_{C1}/V_T = g_{m1}$, $I_{C2}/V_T = g_{m2}$, $I_{C3}/V_T = g_{m3}$, and $g_{m2} = A*g_{m1}$, the noise factor simplifies to equation 16.

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{g_{m1}R_S}{8} + \frac{\gamma g_{mPFET}R_S}{4} + \frac{Ag_{m1}R_S^3}{2R_F^2} + \frac{g_{m3}R_S^3}{2R_F^2} \qquad \{16\}$$

Noting that $g_{m1} = g_{m3} = 1/R_S$ the noise factor further simplifies to equation 17.

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{1}{8} + \frac{\gamma g_{mPFET}R_S}{4} + \frac{(A+1)R_S^2}{2R_F^2} \qquad \{17\}$$

II.2.E.ii Second Stage with Summer/Amplifier

(a)   *(b)*
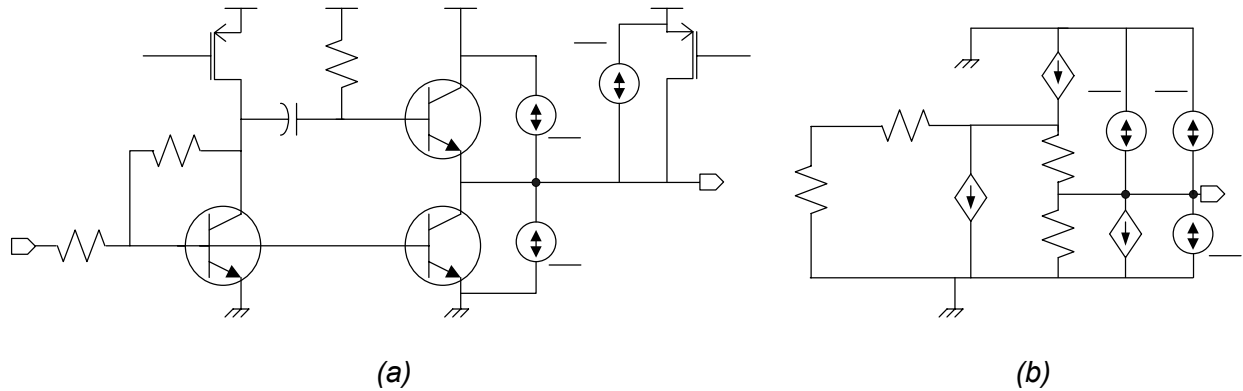
Figure 11. Noise Sources in Noise Canceling Second Stage Topology:

schematic (a) and modified small signal model (b)

Three additional noise sources are added to the first stage analysis in equations 5 and 7 when using the topology from Figure 9. They are the shot noises from Q_2 and Q_3 as well as the thermal noise from P_2 and are shown in Figure 11 (a). As in the case of the original second

stage topology, all output noise sources are in parallel and are thus referred to the input in the same manner.

Changing the noise current sources $\overline{I_{n\text{-}Q2}}^2$, $\overline{I_{n\text{-}Q3}}^2$ and $\overline{I_{n\text{-}P2}}^2$ to small signal current sources $i_{nss\text{-}Q2}$, $i_{nss\text{-}Q3}$ and $i_{nss\text{-}P2}$ the noise transfer function is equal to these small signal currents multiplied by the output impedance $1/g_{m3}$ (from equation 11). The output noise power is therefore the noise current source power multiplied by $1/g_{m3}{}^2$. To find the input referred noise voltage, this value is divided by the gain squared of the circuit, $\{-(g_{m1}R_F - 1) - g_{m2}/g_{m3}\}^2$, given in section II.2.D. Since g_{m1} is constrained to be $1/R_S$ and g_{m2}/g_{m3} equals A which in turn equals, $R_F/R_S + 1$, the gain squared is equal to, $(2*R_F/R_S)^2$. For full analysis see Appendix section A.V. The resulting input referred noise voltages are given in equations 18 (a), (b) and (c) for the shot noises from Q_2, Q_3 and P_2 respectively.

$$\overline{V_{i\text{-}Q_2}}^2 = \frac{qI_{C2}\Delta f R_S{}^2}{2g_{m3}{}^2 R_F{}^2} \qquad \overline{V_{i\text{-}Q_3}}^2 = \frac{qI_{C3}\Delta f R_S{}^2}{2g_{m3}{}^2 R_F{}^2} \qquad \overline{V_{i\text{-}P_2}}^2 = \frac{kT\gamma g_{mP_2}\Delta f R_S{}^2}{g_{m3}{}^2 R_F{}^2} \qquad \{18\}$$

(a)   (b)   (c)

As the noise from transistors Q_1 and P_1 has been canceled (see discussion in II.2.C), the noise factor of the circuit is governed by feedback resistor R_F, transistors Q_2, Q_3, and P_2. The input referred noise voltage of R_F is given by equation 5 and will not be repeated here. The Noise factor after dividing by the source impedance noise power value $4kT\Delta f R_S$ is given by equation 19. The Noise Figure is the $\log_{10}$ of this ratio in dB.

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{I_{C2} R_S}{8 V_T g_{m3}^2 R_F^2} + \frac{I_{C3} R_S}{8 V_T g_{m3}^2 R_F^2} + \frac{\gamma g_{mP2} R_S}{4 g_{m3}^2 R_F^2} \qquad \{19\}$$

Substituting $I_{C2}/V_T = g_{m2}$ and $I_{C3}/V_T = g_{m3}$, as well as noting that $g_{m3} = 1/R_S$, the noise factor simplifies to equation 20.

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{g_{m2} R_S^3}{8 R_F^2} + \frac{R_S^2}{8 R_F^2} + \frac{\gamma g_{mP2} R_S^3}{4 R_F^2} \qquad \{20\}$$

Simplifying further by setting $g_{m2} = A^* g_{m1}$ and noting that $g_{m1} = 1/R_S$ we have equation 21.

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{(A+1) R_S^2}{8 R_F^2} + \frac{\gamma g_{mP2} R_S^3}{4 R_F^2} \qquad \{21\}$$

Looking at this expression, some intuition may be gained as to how to minimize the noise contribution from this circuit. Since it is assumed that $R_F \gg R_S$ (needed for gain) the first term is negligible. The next term may be minimized by increasing R_F. This will come at the expense of power consumption as a larger R_F will require a larger g_{m2} (more current through transistor Q_2) in order to keep the noise canceling conditions. This reasoning also applies to the third term, where an increase in R_F will also decrease the noise contribution. Finally, in order to minimize the third term g_{mP2} may be decreased at the cost of linearity (as explained in section II.2.B with respect to P_{Bias}.

II.2.E.iii Comparison of the Two Second Stage Noise Factors

From section II.2.E.i the noise factor of the emitter follower with current source load stage is:

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{(A+1)R_S^2}{2R_F^2} + \frac{\gamma g_{mP1} R_S}{4} + \frac{1}{8}$$

From section II.2.E.ii the noise factor of the summer/amplifier is:

$$N.F. = 1 + \frac{R_S}{R_F} + \frac{(A+1)R_S^2}{8R_F^2} + \frac{\gamma g_{mP2} R_S^3}{4R_F^2}$$

The first two terms are present in both equations and can ignored for this analysis. The third term is four times less for the summer/amplifier second stage than for the emitter follower second stage. This is due to there being twice the gain at the output for the summer/amplifier as there is for the emitter follower alone. The fourth term, the contribution from the current sources is also significantly less for the summer/amplifier. Since P_1 and P_2 will have the same V_{GS} and P_2 is sized A-1 times larger than P_1, g_{mp2} will be approximately A times larger (assuming $A >> 1$) than g_{mp1}. Simplifying, the contribution from the summer/amplifier will be R_F/R_S smaller than the emitter follower. This can be seen numerically from the analysis below.

$$\frac{\gamma g_{mP_2} R_S^3}{4R_F^2} \longrightarrow \frac{A\gamma g_{mP_1} R_S^3}{4R_F^2} \longrightarrow \frac{R_F}{R_S} \frac{\gamma g_{mP_1} R_S^3}{4R_F^2} \longrightarrow \frac{\gamma g_{mP_1}}{4} \frac{R_S^2}{R_F}$$

Finally, there is a 1/8 term in the emitter follower equation that does not have a counterpart in the summer/amplifier equation. Thus, the emitter follower stage has more noise and the summer/amplifier that implements the noise canceling is a better choice for the output stage.

II.3 Transistor Tradeoffs

It is interesting to note that most transistor specifications are related to the emitter current density J_C as opposed to just the emitter DC current [9]. This is especially true for both the noise figure (NF) and unity current gain frequency (f_T). It is therefore unfortunate that the J_C for maximum f_T is much larger than that for the optimal noise. A tradeoff must be made between these two quantities which determines the maximum frequency of operation and noise figure of the wideband amplifier. Figure 12 shows a hypothetical example of such a tradeoff, where the values are not given due to their highly process dependant nature and confidentiality that the fabrication plant requires. The values can be obtained by looking at pages 100-106 of [10] for the 6HP process and page 19 of [11] for the Jazz process.
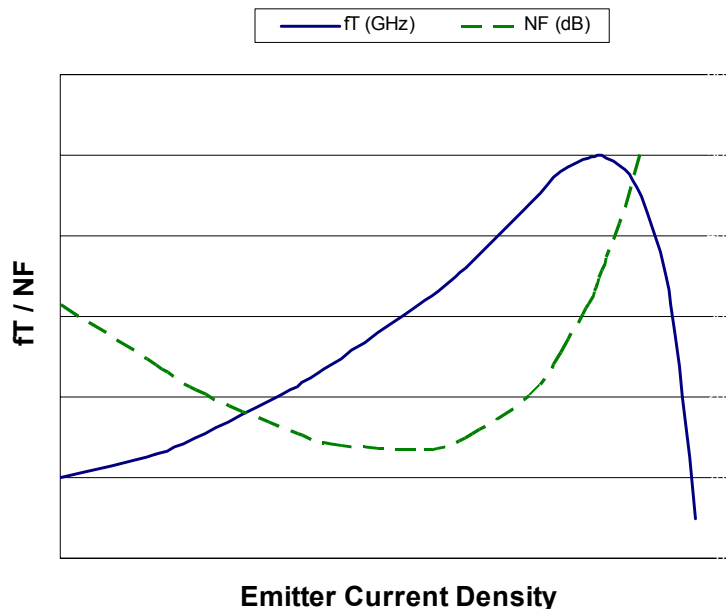
Figure 12. NF & f_T vs. J_C for a hypothetical transistor in a SiGe process

Other quantities affecting the circuit performance and related to the emitter current density are the transconductance g_m and current gain β. The transconductance is nominally equal to the

collector current I_C divided by the thermal voltage V_T. At large values of J_C the transconductance no longer behaves linearly and increasing I_C only causes a slight increase in g_m (from pages 76-96 of [9]). The same is true for the β value of the transistor, where larger J_C values result in a decreased current gain. Since this region of large J_C is also where the transistor f_T may be at its peak one must be careful when solely looking for high frequency operation.

II.4 High Frequency Design Issues
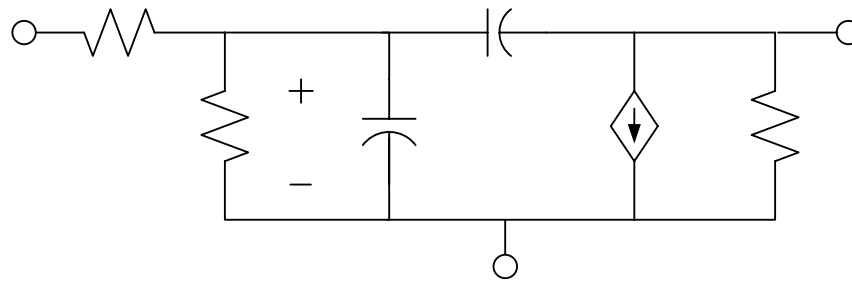
Figure 13. NPN Transistor High Frequency Model

So far in the analysis only low frequency circuit models have been used. This is because the amplifier is being designed to operate within its passband, or region where the gain has a flat frequency response. In this region the parasitic capacitance impedance is large compared to any parallel resistance. Figure 13 shows the parasitic capacitors of the SiGe NPN transistors. C_μ will be ignored in this analysis due to its low value and the fact that the Miller effect is greatly lessened because of the low gain values present in the circuit. C_π results from the added capacitances from the base diffusion & base-emitter junction and is the primary high frequency component of interest. It can be computed from equation 22 (a), the relation of unity gain frequency f_T and transconductance g_m to C_π. The effective impedance Z_π is given by equation

27

22(b) and is equal to $r_\pi \| C_\pi$. It is evident that as frequency increases the $sC_\pi r_\pi$ term in the

denominator increases as well, resulting in a lower effective impedance.

$$C_\pi = \frac{g_m}{2\pi f_T} \qquad Z_\pi = r_\pi \| \frac{1}{sC_\pi} = \frac{\dfrac{r_\pi}{sC_\pi}}{r_\pi + \dfrac{1}{sC_\pi}} = \frac{r_\pi}{sC_\pi r_\pi + 1} \qquad \{22\}$$

(a) (b)

Previously in this thesis it has been assumed that r_π is much larger than parasitic resistor r_b.

When the impedance Z_π decreases due to frequency it results in less voltage drop v_π. This will

cause less induced current to flow, effectively decreasing the transconductance of the amplifier.

This drop in transconductance is given by equation 23 where Z_π is given in equation 22 (b). This

affects both the high frequency gain (bandwidth) and input/output matching as these quantities

are directly related to the transconductance (see Section II.2).

$$g_{m-eff} = g_m \frac{Z_\pi}{Z_\pi + r_b} \qquad \{23\}$$

II.5 NeoCircuit® for Automated Design Synthesis

In order to get the maximum performance from the amplifier, the values for the transistor emitter

lengths, passive sizing and PFET gate lengths and widths should be tweaked for the

application. This is due to second and third-order effects that are very hard to solve at the hand

analysis level. NeoCircuit, an automated simulation tool, was used to quickly meet multiple

specifications while minimizing area and power. NeoCircuit works by running the same

simulations that a designer who is tweaking values themselves would run. NeoCircuit can run

hundreds of these simulations in a row, sweeping design variables and attempting to meet goals

along the way. This is all automated, and the values which result in peak circuit performance

can be found in much less time than if the designer was changing values themselves.

For this circuit, the design variables (see Figure 14 (a)) included all possible device sizes as well

as the bias currents. The *A* parameter was also part of the analysis and set the size of the

feedback resistor as well as the number of transistors in parallel for Q_2. Goals included the input

and output matches, gain, bandwidth and noise. Because of the need to operate at multiple

frequencies, goals were created at each of the frequencies of interest (1.2 GHz and 2.1 GHz for

the IBM fabrication run) and can be seen in the lower section of Figure 14 (b). To help

understand the screenshot, the first goal is for the input match (S11) at 1.2 GHz. The goal is set

to be less than -12 dB. Power was set to be minimized such that gain and noise would barely

meet specification.

(a)   (b)

Figure 14. Neocircuit Screenshots for Variables (a) & Goals (b)

29

Neocircuit was also used when translating the amplifier design from the IBM process to the Jazz process. A device file was created that described the Jazz components and what could be changed in each instance (for example the capacitor length and width). This step only needs to be done once for any process and the file may be shared between users. Next, a schematic was created that contained the architecture of the wideband amplifier. Neocircuit was then run with nearly identical variables and goals. A caveat of the Jazz process was that the transistor emitter width could not be changed through a variable as different widths required different simulation models. Thus, NeoCircuit was run independently for a few emitter widths ranging from 2μm up to 14μm. The size that was able to meet all goals at the lowest power level was chosen as the final design.

III. Layout, Extraction & Testing

III.1 Circuit Layout

Two fabrication runs were made in two different processes for this same topology. The first run was a 47 GHz f_T 6 Metal Process from IBM while the second was a 60 GHz f_T, 4 Metal Process from Jazz Semiconductor. The IBM run employed an *A* value of 7 while the Jazz run employed an *A* value of 11. In order to cancel the noise effectively, matching between the transistors was essential. This was accomplished by setting a fixed transistor length and setting the transistors in a matrix (3x3 for the IBM run, 4x4 for the Jazz run). This worked out as a transistor for Q_1, a transistor for Q_3 and either seven or eleven for Q_2. This regular pattern, as can be seen in the

lower left corner of the layouts in Figure 15, will help ensure matching. The Jazz run also includes three dummy transistors to complete the 4x4 matrix. Current matching in the bias network is also important in the noise canceling, and as can seen on the right side of the layout from figures 15(a) and (b), a regular pattern is used for the PFETS as well.
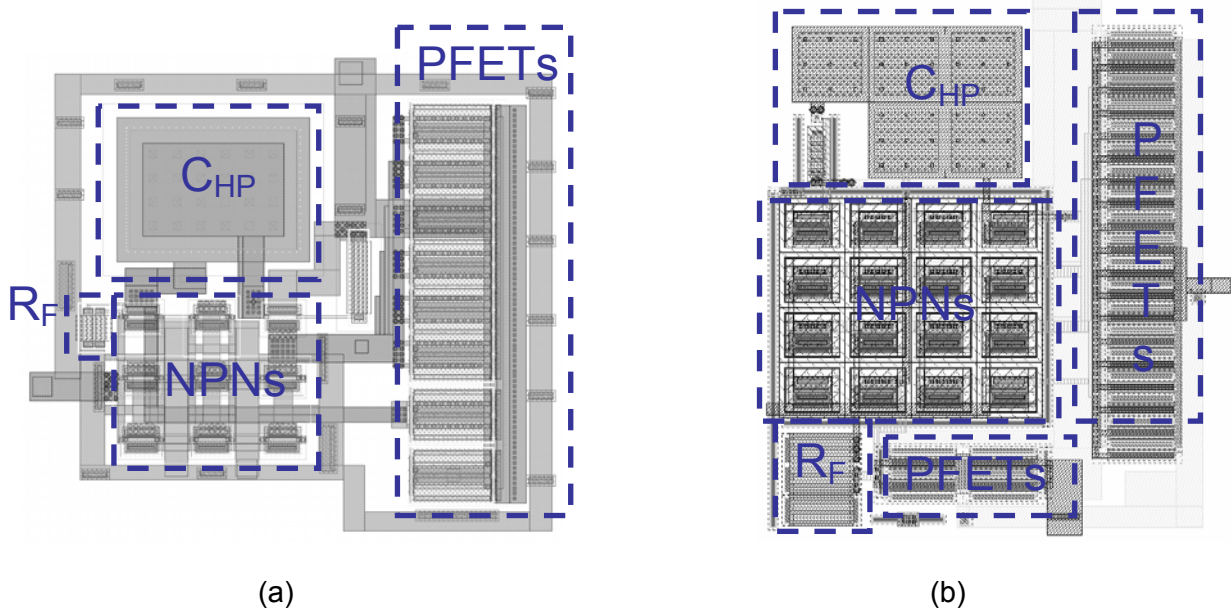

<center>(a)</center>

<center>(b)</center>

Figure 15. Layout of IBM run (a) & Jazz Run (b).

Area is 75μm x 80μm for (a) and 70μm x 85μm for (b)

Other issues to note about the layout include the use of substrate contacts surrounding all active components as well as a deep trench, available in the IBM process, surrounding all components as well as the entire circuit itself. This helps isolate the devices and reduce coupling through the substrate.

III.2 Testing Layout

In order to be able to test the circuit there must be a way to put a signal in and measure the amplified signal out. The circuit also needs to be powered and its bias point set. Classical test and measurement techniques include bonding from the chip to an outside package or brass board, using probes to provide the aforementioned signals, or some combination of the two.

At RF frequencies the wavelengths of the signals approach the length of the physical wires connecting the test equipment to the circuit. The use of either unshielded probes or bond wires for the high frequency signals will result in coupled noise from the environment and poor matching due to the parasitic inductances. The solution to this issue is the use of high frequency rated coaxial cables paired with shielded probes called Ground-Signal-Ground (GSG) probes [12]. The parasitic losses associated with this setup will be well-characterized due to the shielding, and may be calibrated out when testing (see section III.4).

Two approaches were used for the DC power and biasing needs. Bondpads for the IBM run (Figure 16(a)) and DC probes for the Jazz run (Figure 16(b)). For the first approach a PCB board was constructed (see section III.3) with decoupling capacitors to ground in order to minimize the parasitic inductance of the cable that leads from the equipment to the PCB. This is a better solution than a standard probe, which has huge amounts of parasitic inductance due to the lack of decoupling capacitors. The second approach used a probe with five connections with on-probe decoupling capacitors to minimize the effect of parasitic inductance during testing. The five pads can be seen at the top of Figure 16(b) with a 100μm pitch. Though there are only three DC connections to be made, the remaining two are shorted to ground such that there is less parasitic inductance.
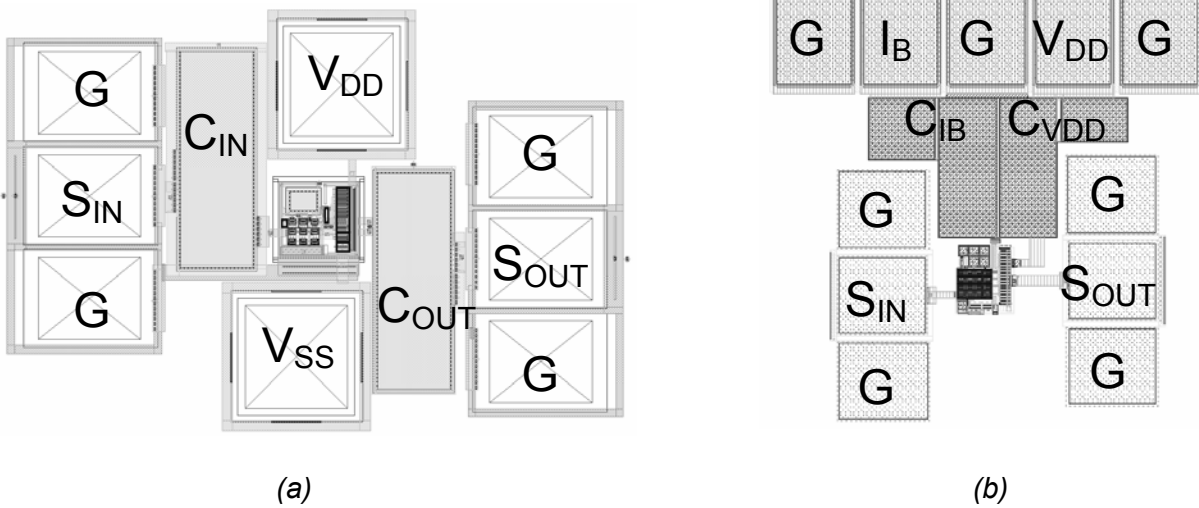
32

(a)   *(b)*

Figure 16. Full Layout with pads of IBM run (a) & Jazz Run (b)

The area is 600μm x 400μm for (a) and 450μm x 500μm for (b)

The input and output signals must be AC coupled to allow the LNA to set its own DC bias point. Either capacitors must be placed in series with the input and output connection or the test equipment must be AC coupled. In the IBM run this was accomplished by placing 22 pF DC blocking capacitors (labeled C_{IN} and C_{OUT} on Figure 16 (a)) on-chip. The impact of this is discussed in section IV.1. For the Jazz run, bypass capacitors are used off-chip, connecting between the cable and the test equipment. The only on-chip capacitors used are C_{IB} (15 pF) and C_{VDD} (16 pF), decoupling capacitors for the DC signals seen in Figure 16 (b). These should be made as large as possible to create a low impedance path to ground for signals that are meant to be DC (bias current and power supply in the scope of this circuit).

The fabricated LNA from the IBM fabrication run can be seen in Figure 17. The details of the circuit are obscured because there is metal connected to ground covering the entire circuit. This was included in the in order to protect the circuit from the post-processing that is required to

release MEMS devices elsewhere on the chip. Though the metal will add capacitance to all

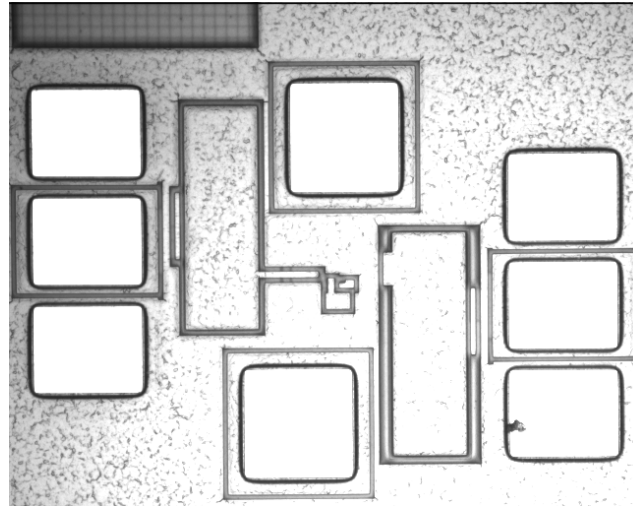nodes in the circuit, without it all the active devices would be etched away.

Figure 17. Micrograph of LNA experiment from IBM fabrication.

Transistors can not be seen due to metal top cover

III.3 Board Design

The board design for the bonded IBM case is shown in Figure 18. It is meant to provide

capacitance between the DC signals wired to J1 (voltage supply) and J3 (current bias) and

ground. There are five capacitors on both the power supply and bias current supply due to the

different self-resonant frequencies of different sized capacitors. As the capacitance increases,

so does the parasitic inductance across the two metal planes. The self-resonant frequency is

given by equation 24, from which it may be concluded that large capacitors have low self-

resonant frequencies.

$$2\pi f = \frac{1}{\sqrt{L_{PARASITIC} * C_{NOM}}} \qquad \{24\}$$

Therefore, the board will ensure that there will be sufficient capacitance regardless of the frequency of the noise. Connections to the board are made through a ribbon cable that attaches to the header JP1. Finally, the chip sits on a metal groundplane which is tied to the chip ground from multiple places on-chip.
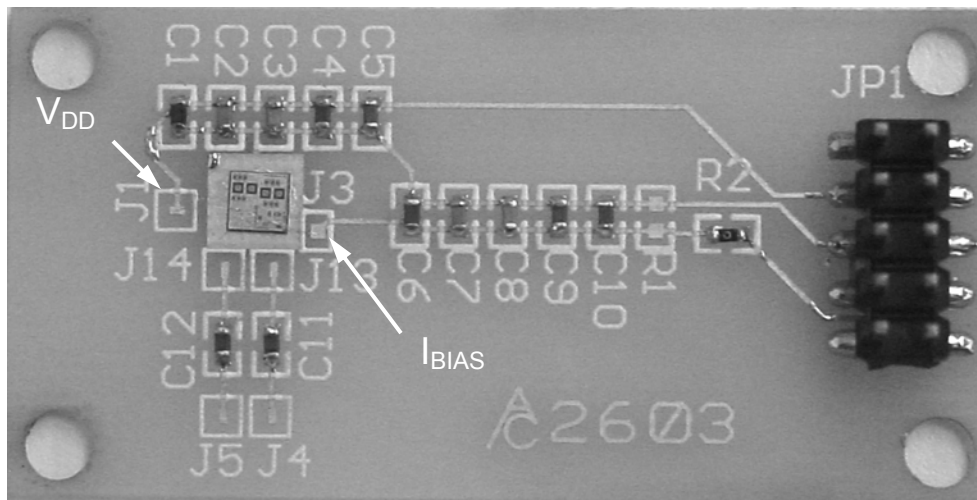

Figure 18. Board Design with Chip Pasted on

The chip was attached onto the groundplane with silver paste and then the DC signals were bonded. The total bond length from the voltage supply or bias current supply pads on-chip to the package was about 6mm. Ground was bonded from four pads on-chip to the groundplane. These wires were approximately 1mm in length. If bondwire inductance is assumed to be 1nH/mm, there is 6nH between both of the supplies and their on-chip pins, as well as 250pH between ground and the PCB groundplane. The purpose of R1 and R2 are to enable two types of current biasing. With a zero ohm resistor in R2 and nothing connected across R1 the bias current may be set off-chip through the ribbon cable. With a resistor across R1 and the zero

ohm resistor removed from R2 the current is set directly on-board and reduces the noise coupling on the bias line that could be incurred through the ribbon cable. The board has a gold top metal for all traces and bonding pads in order to guarantee that the gold wires will bond to the PCB. Furthermore there is nothing on the backside such that it can be placed directly onto the vacuum chuck of the Cascade Microtech Probestation.

III.4 Testing Simulation Setup

In order for simulation data to match testing data all components that will not be calibrated must be modeled. For the scope of the IBM run and board setup, the signal input and output can be calibrated down to the pad level using the network analyzer and WinCal® software. It is also possible (though not done in the IBM run) to calibrate the test equipment all the way to the chip level by placing dummy pads and traces elsewhere on the chip. Using these dummy shapes the Network Analyzer can then remove these parasitics and a measure of actual circuit performance may be obtained. If the test equipment or test setup used does not allow for de-embedding of the cable and probe they must be modeled as transmission lines as part of the system simulation.

The RF input and output are not the only connections that must be modeled. The DC connections, especially in the case of bonding, must be placed in the simulation model as well. Bondwire or probe parasitic inductance will have a huge impact on circuit performance (see section IV.1) and there is no way to calibrate the test equipment to include these. Because of this fact, the designer should minimize the effect of these test bed parasitics by including very large decoupling capacitors on-chip.

IV. Results

IV.1 Extraction & Test Bed Parasitics

In order to model the impact of test-bed parasitics on performance, simulation results from the IBM design were analyzed at four points in the layout process: the LNA by itself (L), the LNA including GSGs and bondpads (L+P), the LNA including GSGs, bondpads and the input/output bypass capacitors (L+P+C), and the LNA including GSGs, bondpads, the input/output bypass capacitors and the bondwire inductances (L+P+C+B). Also included is a hypothetical simulation assuming use of the Eyepass five probe for the DC connections (L+P+C+E). Simulation of the extracted layouts capturing the non-idealities are shown in Table 1 below. All results are taken at 2.1 GHz. Analysis of these results can be found in section V.1 and V.2.

	L	L + P	L + P + C	L + P + C + B	L + P + C + E
S11	-13.34 dB	-11.12 dB	-9.21 dB	-12.15 dB	-10.19 dB
S21	15.0 dB	14.25 dB	13.85 dB	12.41 dB	13.66 dB
S22	-14.51 dB	-13.67 dB	-10.04 dB	-15.64 dB	-10.71 dB
S12	-28.53 dB	-28.58 dB	-28.87 dB	-25.81 dB	-27.5 dB
Noise Figure	2.56 dB	2.85 dB	3.09 dB	3.81 dB	3.20 dB
3 dB BW	4.6 GHz	4.2 GHz	3.7 GHz	3.2 GHz	3.5 GHz
ICP 1dB	-15.89 dBm	-16.57 dBm	-17.95 dBm	-14.71 dBm	-16.89 dBm
IIP3	-6.4 dBm	-8.2 dBm	-9.1 dBm	-5.7 dBm	-8.1 dBm

Table 1. Simulation of circuit including layout (L) parasitics, pad (P) parasitics, dc blocking capacitor (C) parasitics, bondwire (B) parasitics and Eyepass Probe (E) parasitics

ICP represents the input compression point, while IIP3 represents the input-referred third order modulation point. Simulation measurements were made using the SpectreRF simulator and Cadence design tools.

IV.2 Experimental Results

	IBM 6HP (measured)	Jazz (extraction)	[1]	[5]
Figure of Merit	0.213	0.212	0.163	0.178
S21	14.9 dB	17.9 dB	13.7 dB	12 dB
S11	-11.36 dB	-10.5 dB	-8 dB	-10 dB
S22	-13.73 dB	-7.8 dB	-12 dB	-9 dB
S12	-22.07 dB	-25.6 dB	-36 dB	Not Given
N.F.	4.4 dB	2.9 dB	2.4 dB	2.8 dB
3 dB BW	2.8 GHz	2.6 GHz	1.6 GHz	15 GHz
ICP 1dB	-15.27 dBm	-13.7 dBm	-9 dBm	-7.6 dBm
IIP3	-8.7 dBm	-1.9 dBm	0 dBm	1.9 dBm
Area (ckt)	80 x 75 μm^2	85 x 70 μm^2	300 x 250 μm^2	> 150 x 150 μm^2
Power	15.9 mW	29 mW	35 mW	24 mW
Technology	IBM 6HP	Jazz 60 GHz f_T	0.25μm CMOS	80 GHz f_T SiGe

Table 2. Results from Testing & Other Designs. Jazz extraction includes all on-chip parasitics as well as off-chip probe parasitics.

Results from testing of the IBM fabrication run are presented in Table 2, along with those from other wideband LNA designs. The numbers represent the worst case value of each specification within the passband of each amplifier except for the gain (S21) which is taken as the maximum value. This is due to the fact that the passband is set by the frequency where the gain equals this maximum value subtracted by 3 dB. The Figure of Merit is given by *Gain / (Noise * Power)* and is used in other low noise papers such as [13].

The following graphs show various metrics versus frequency from extraction of the entire experiment for the IBM fabrication run (LNA plus pads, capacitors and bondwires) as well as from physical testing. S parameters and Power Compression were measured on an Agilent E8364A Network Analyzer that was calibrated with WinCal® software and an impedance standard substrate. Noise Figure was measured using an Agilent E4440A Spectrum Analyzer with Noise Figure Personality and an Agilent 346C Noise Source. Cable and probe losses were included in the Noise Figure measurement using the Noise Figure personality on the Spectrum Analyzer. Full test setups are included in the Appendix, section VIII.

The following graphs of gain (S21) and noise figure below include both extracted results with package parasitics (bondwires) as well as without. This difference will be discussed in section V.1.
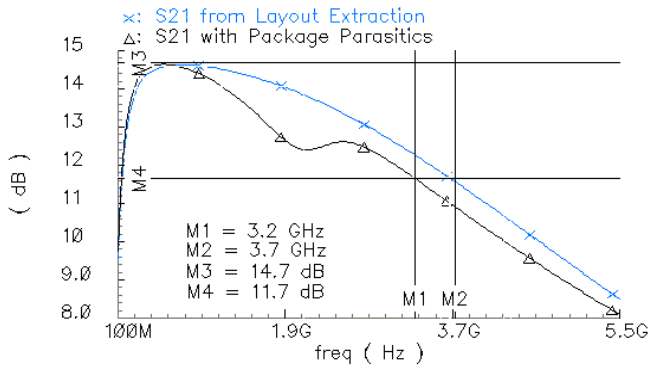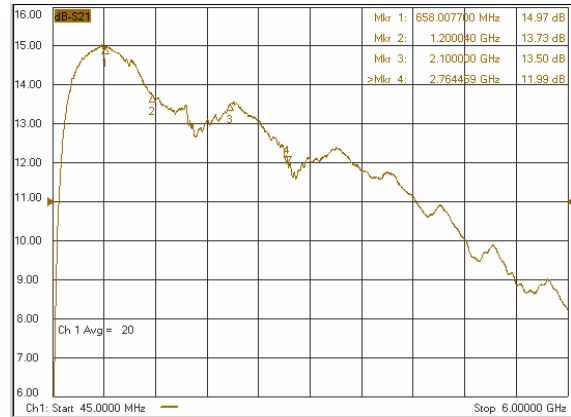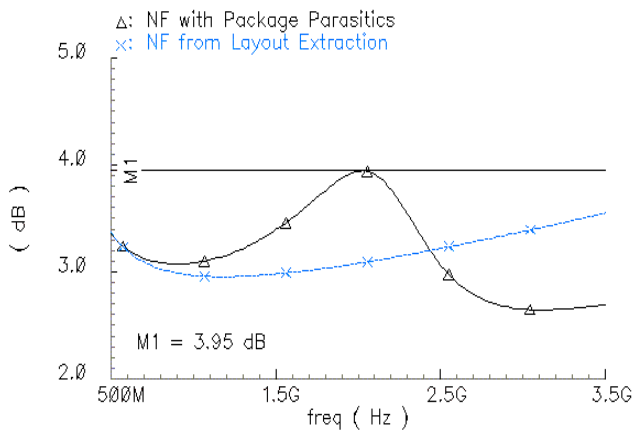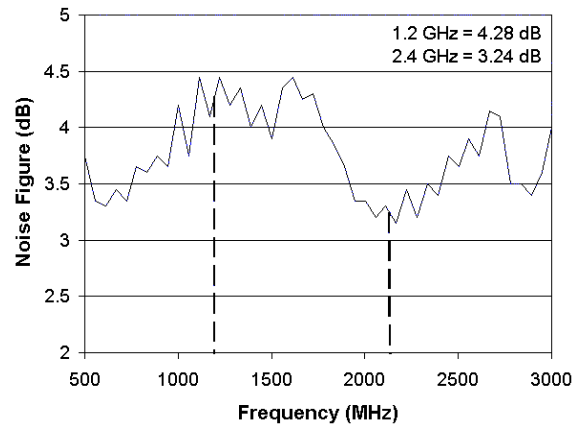
(a)   *(b)*

Figure 19. S21 Extractions (a) & Testing (b) The slight peak at 2.1 GHz is due to shunt peaking from the power supply bondwire inductance.


(a)   *(b)*

Figure 20. Noise Figure Extractions (a) & Testing (b). Spectrum Analyzer testing results are graphed using Microsoft Excel®.

The following graphs compare the rest of the S parameters between a simulation that includes test-bed parasitics and the measurements from the network analyzer. Simulation data closely correlated to measurement data, with differences discussed in section V.1.
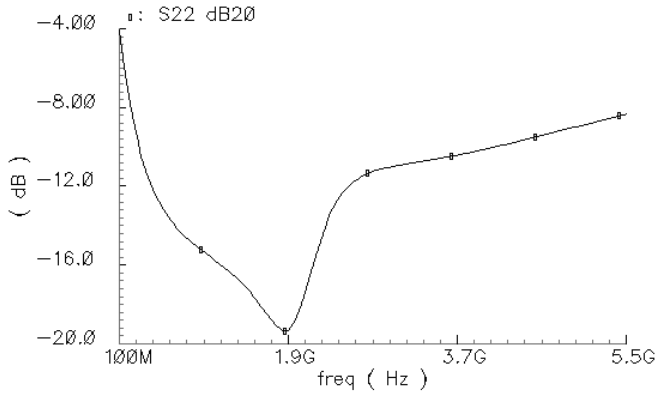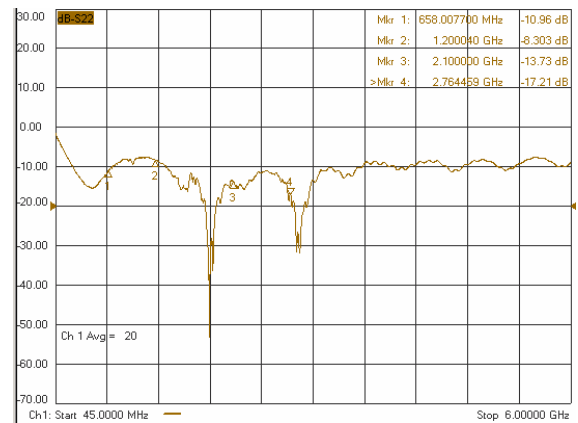
40
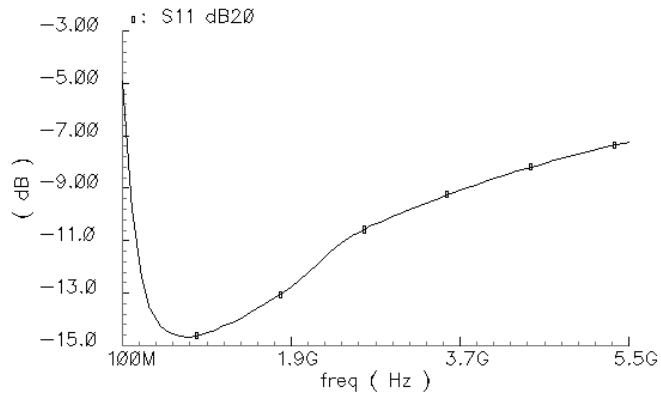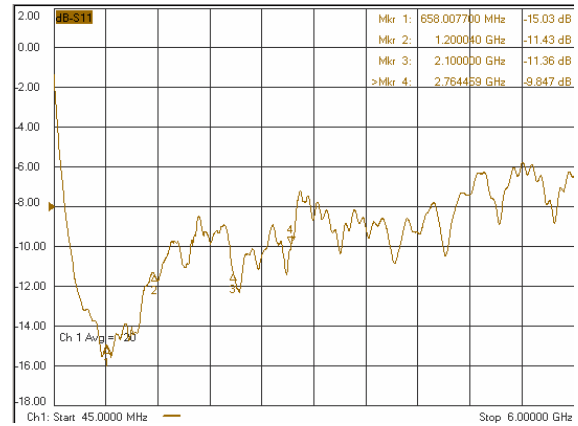
(a)   *(b)*
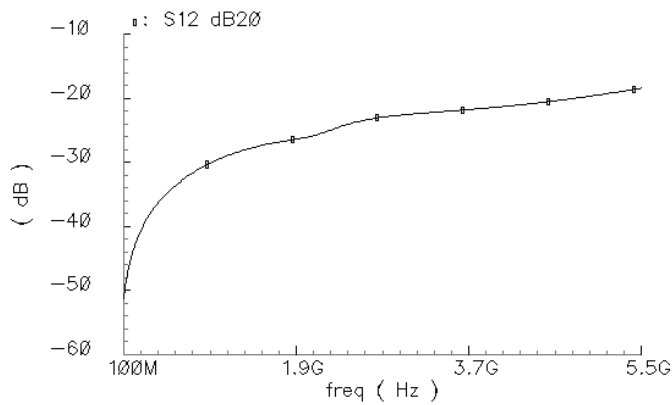
Figure 21. S11 Extraction of L + P + C + B (a) & Testing (b)
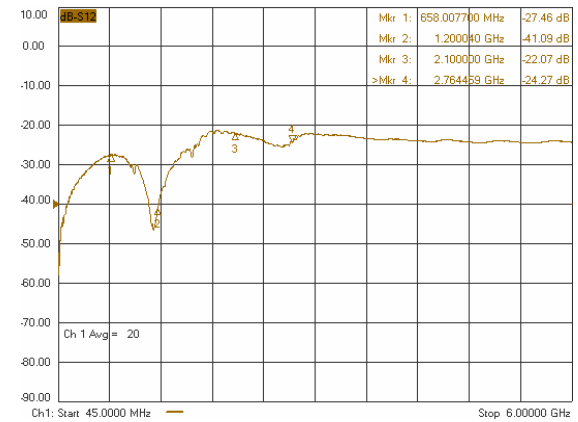

(a)   *(b)*

Figure 22. S22 Extraction of L + P + C + B (a) & Testing (b)

(a)   *(b)*

Figure 23. S12 Extraction of L + P + C + B (a) & Testing (b)

41

The following graphs show the linearity metrics versus input power for extraction (L + P + C + B) and testing. Power compression was measured with a network analyzer power sweep. IIP3 measurements were taken by using two Agilent E8251A Signal Generators, a Mini-Circuits ZN2PD2 power combiner and the E4440A Spectrum Analyzer. For the IIP3 measurement signals of the same amplitude but of slightly different frequencies generated using the signal generators and summed by the Mini-Circuits combiner drove the RF input. Measuring and extrapolating the intermodulated amplitude versus the signal amplitude across a span of input amplitudes enabled an accurate IIP3 measurement. For more details on the IIP3 measurement setup please see Appendix section VII.3. Both metrics showed slightly poorer performance compared to other wideband designs (from Table 2) due to tradeoffs with noise performance (see section II.2.B).
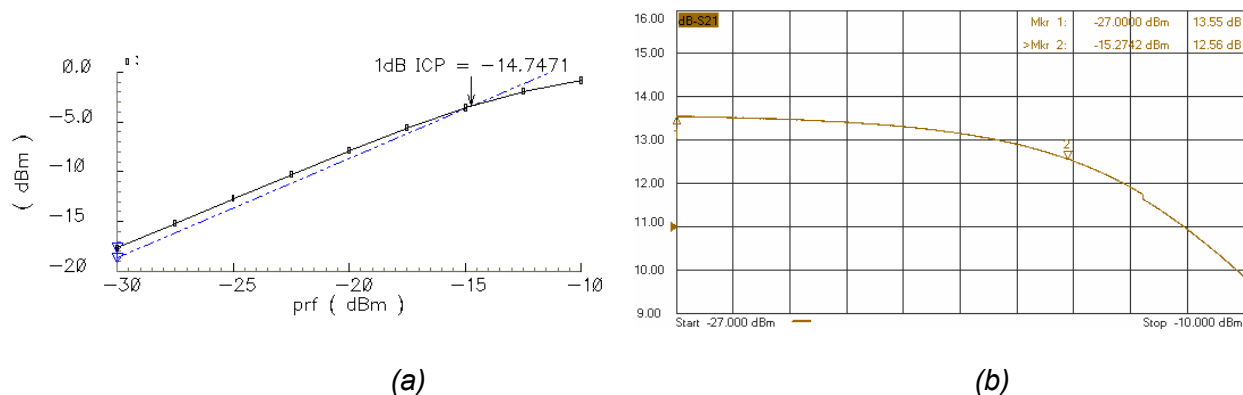

(a)   *(b)*

Figure 24. 1 dB Input Compression Point Extraction of L + P + C + B (a) & Testing (b)

(a)   (b)
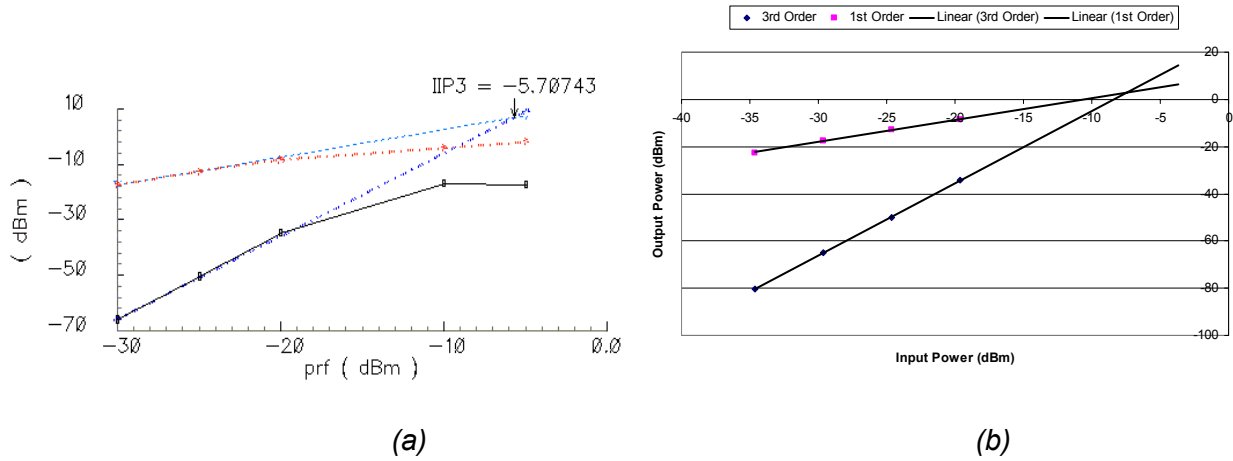
Figure 25. IIP3 Point Extraction of L + P + C + B (a) & Testing (b). Extrapolation was completed

using Microsoft Excel® and results from Spectrum Analyzer

The following graph shows an plot of gain and noise vs. frequency for the extracted Jazz

design. No experimental results are shown because the chip was still being fabricated at the

time of writing of this thesis.

Figure 26. Gain and Noise of Jazz Design vs. Frequency. Simulation included all

chip parasitics as well as probe parasitics

V. Assessment of Results

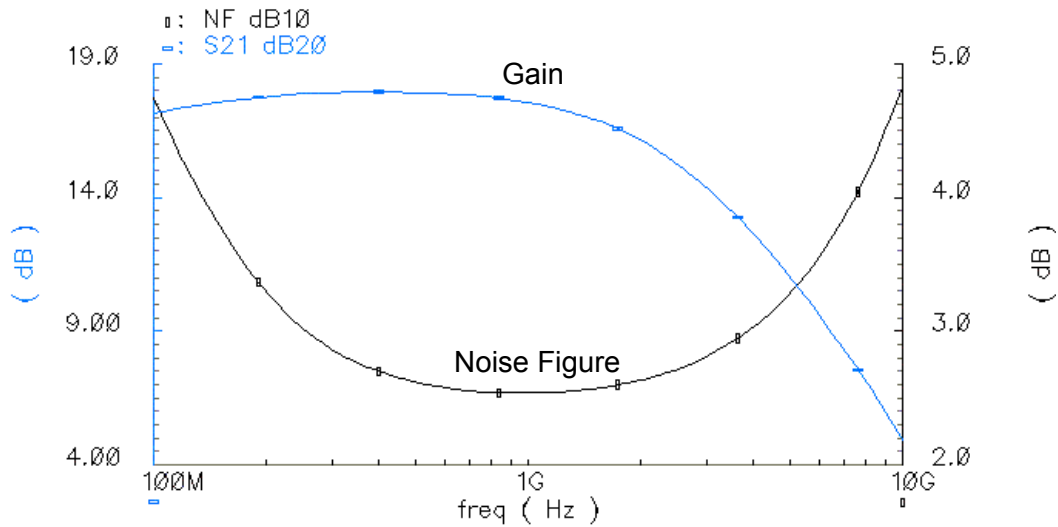The comparison in Table 1 shows three parasitic sources and their effects on the simulated data for the amplifier: the signal pads, the bypass capacitors and the bondwires. Because there is no way to get around using GSG pads for testing, methods for minimizing the effect of the other two parasitics will be discussed. They have been implemented in the Jazz layout (Figure 10.b) and an extracted simulation with the improved parasitics is shown in Figure 26 above.

V.1 Capacitive Effects

The dc blocking capacitors C_{IN} and C_{OUT} shown in figure 27 were used to allow self-biasing of the amplifier (see section II.2 for more details). They affect the circuit in two ways. Firstly, they prevent impedance matching at lower frequencies due to their series impedance with respect to the signal. This impedance is equal to $1/j\omega C$, and thus becomes less of a problem at higher frequencies where the capacitors act like short circuits. The parasitics, however, become more of a problem at these higher frequencies. The parasitic capacitance arises from the bottom plate of both capacitors to the substrate and is modeled by $C_{P\text{-}IN}$ and $C_{P\text{-}OUT}$. They are therefore located in parallel to the input and output impedances of the LNA. At higher frequencies the impedance from the parasitic capacitance lowers the overall impedance and provides a poorer match to both the source and the output. These issues reduce the overall bandwidth of the LNA and may be resolved in two ways. The designer may choose to place test structures containing a GSG pad and the dc blocking capacitor tied to nothing such that the parasitic capacitance may be de-embedded during testing (see section III.4). Alternatively the designer may chose to place dc blocking capacitors off-chip. These off-chip capacitors (which have minimal parasitic

capacitance and are available in large sizes for better low frequency matching) would connect
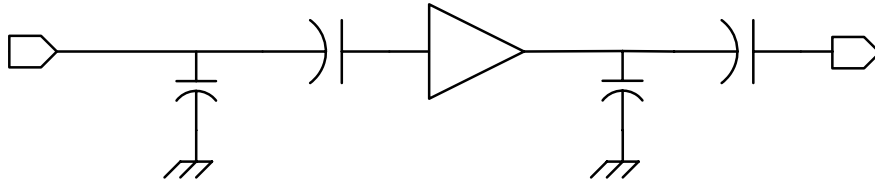
between the probe cable and test equipment.

Figure 27. Input and Output Capacitors & Parasitics
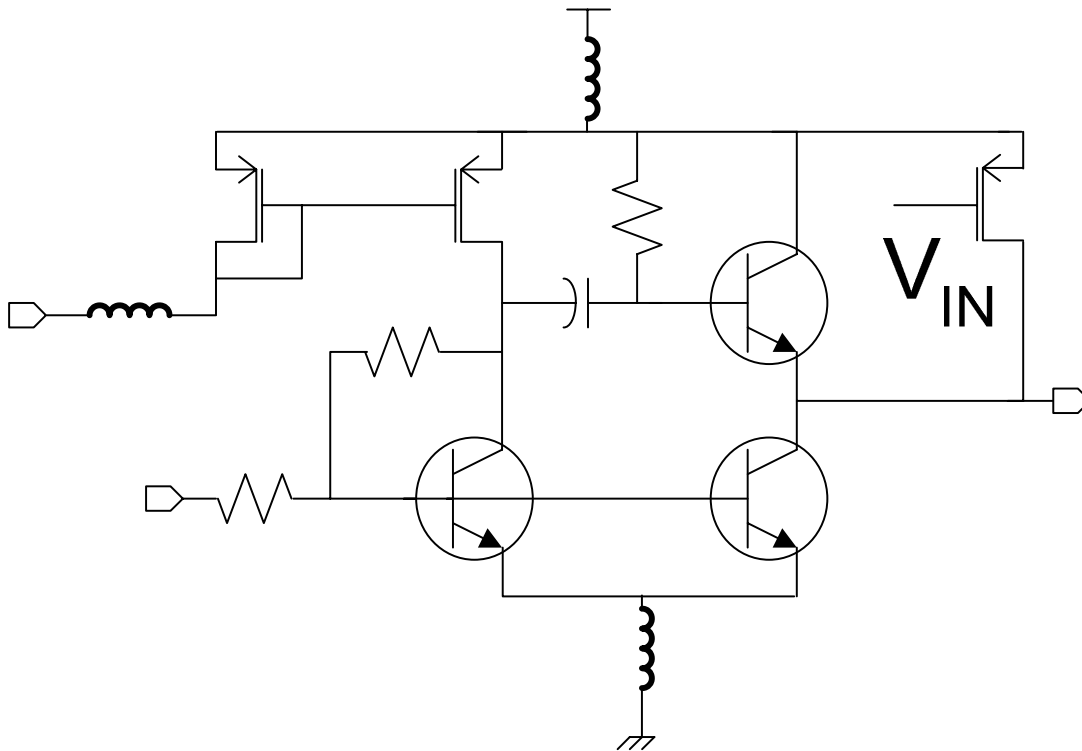
V.2 Bondwire Effects

Figure 28. Bondwire Inductances in the circuit

The various bondwire inductances are shown in Figure 28. They each contribute differently to the circuit, and will be explained separately. The ground bondwire inductance will have the greatest effect in the circuit both decreasing the bandwidth as well as increasing the noise of the circuit. It has been shown that the effective transconductance of a common emitter amplifier with emitter degeneration (the bondwire impedance acts as this degeneration) is given by equation 25 from page 193 of [14]:

$$g_{m,eff} = \frac{g_m}{1 + g_m Z_{emitter}} \qquad \{25\}$$

where $Z_{emitter}$ is equal to the impedance of L_{GND}, or $j\omega L_{GND}$. Thus, as frequency increases the impedance increases, lowering the transconductance of the transistors Q_1 and Q_2. This decreases the gain as can seen in Figure 19. L_{GND} will also increase the noise seen at the input of the circuit. Though the bondwire itself does not generate thermal noise (except for the small resistance value which is ignored in this analysis), noise currents flowing through the impedance will give rise to a noisy voltage (from page 248 of [14]). This noise voltage will be shifted to the input of the circuit due to the fact that the voltage gain from base to emitter is nearly unity.

The power supply bondwire inductance L_{VDD} as well as the bias current inductance L_{IB} will also increase the noise figure of the circuit, but not to the extent that the ground bondwire does. As in the ground bondwire case, a noise current flows through the power supply and current bias parasitic inductances and will generate a noise voltage on the bias lines. This voltage will be referred to the input first by becoming a noise current through the transconductance of P_1. This noise current is like the noise current from P_1 discussed in Section II.2.B and thus is referred as an input voltage through R_S. The overall equation is given in equation 26 below.

$$\overline{V_{ni}^{2}} = \overline{V_{n-Bias}^{2}} * g_{m-P1}^{2} * R_S^{2} \qquad \{26\}$$

46

Since g_{m-P1} has been minimized for noise considerations in section II.2.B this gain is very small and does not add excess noise. It should be noted that the contribution from L_{VDD} is much greater than that from L_{IB}. This is due to the fact that the current through L_{IB} is 'A' + 2 times smaller than that through L_{VDD}.

The power supply inductor L_{VDD}, while not contributing much to the overall noise figure of the circuit can affect the bandwidth of the circuit due to shunt peaking. Figure 29 (a) shows a high frequency schematic of the bondwire inductance L_{VDD} and pad capacitance C_L.

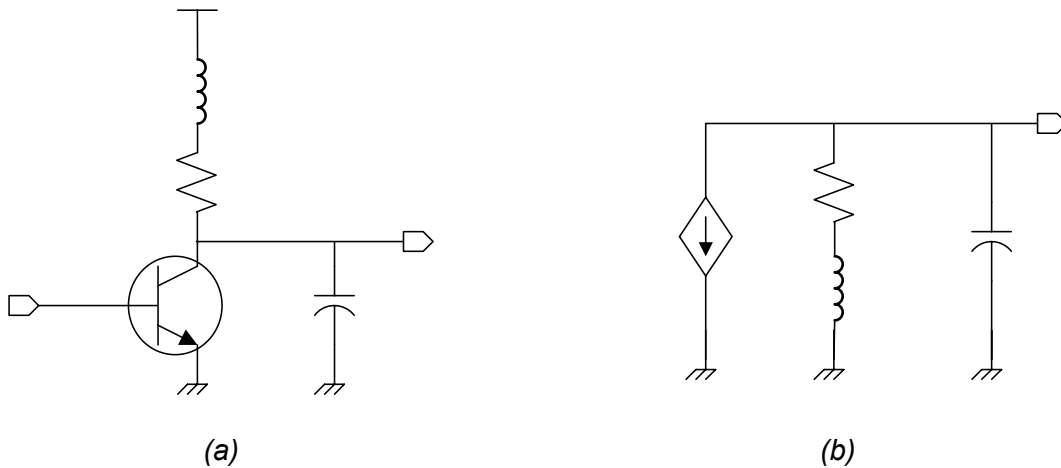(a)   (b)

Figure 29. Shunt Peaking at the Output schematic (a) and small-signal representation (b)

The small-signal representation is given in figure 29 (b). At low frequencies the output resistance is merely $1/g_{m3}$. As frequency increases, the impedance Z_L ($1/j\omega C_L$) begins to decrease, therefore decreasing the total output impedance and decreasing the gain. However, Z_{VDD} ($j\omega L_{VDD}$) begins to increase in impedance, introducing a zero into the system. This increase in impedance helps to cancel the decreasing impedance of Z_L and maintain the same output impedance at high frequencies. The magnitude of this net impedance is given by equation 27, taken from page 180 of [14].

$$|Z(j\omega)| = \frac{1}{g_{m3}} \sqrt{\frac{(\omega L_{VDD} g_{m3})^2 + 1}{(1 - \omega^2 L_{VDD} C_L)^2 + \left(\frac{\omega C_L}{g_{m3}}\right)^2}}$$ {27}

The inductance therefore both introduces a pole and a zero into the system. This can be exploited for an extra boost in bandwidth with a sharp roll off after the peak. This will only occur if the inductance value resonates with the capacitance at a frequency within the pass band. For the scope of the IBM design, this resonance occurs at 2.1 GHz right on the edge of the passband and can be seen in Figure 29 (b).

Once all parasitics are taken into account the LNA shows nearly identical performance between extraction and testing. Slight differences in the bandwidth and noise figure can be attributed to not being able to measure the exact bondwire inductances due to variations in bond length, chip distance to the PCB bondpads, as well as the arc of the bondwire itself.

VI. Conclusion

A design methodology for SiGe BiCMOS RF circuit design in the context of a wideband LNA has been demonstrated in this paper. The design process mimics that of the standard analog design, but with much closer attention to transistor selection and test board parasitics. Beginning with specification selection, RF issues such as impedance matching and low noise figure drove the topology choice to one with shunt resistive feedback with active noise cancellation. Circuit design followed that of standard analog circuits, with extra emphasis on the

non-linearities of the transistors at RF frequencies. NeoCircuit, a design synthesis tool, was used to generate a final design and layout was completed with sensitivity to interconnect parasitics & substrate coupling. Simulation models that included all test-bed parasitics were not created for the initial IBM design and on-chip measurements showed large deviations from simulation results. Regardless, these results showed a functional wideband LNA with a Figure of Merit (*Gain / [Noise * Power]*) greater than comparable designs [1, 2, 5], as well as a bandwidth of 2.8 GHz that was larger than a near identical RFCMOS design [1].

VII. Future Work

Future work with the noise canceling topology includes using more mature testing setups to measure the true performance of the amplifier as well as adapting the technology to higher f_T processes. Using a synthesis tool such as NeoCircuit enables this conversion to be quick and efficient. Another possible improvement may come from shunt peaking at the output using either on or off chip inductances for extended bandwidth. Consuming more power for lower noise and higher gain is also an improvement that may be implemented in this topology.

Other wideband topologies should also be examined and adapted to the SiGe process. SiGe has shown comparable performance to the near identical RFCMOS circuitry of [1], with better area and power efficiency. This type of comparison should be made against a GaAs design, such as in [4].

References

[1] F. Bruccoleri, E.A.M Klumperink and B. Nauta, "Noise Canceling in Wideband CMOS LNAs," *Proc. of ISSCC 2002*, Session 24, pp. 406-407.

[2] J. Janssens, J. Crols and M. Steyaert, "A 10mW Inductorless, Broadband CMOS LNA for 900MHz Wireless Communication," *IEEE Custom Integrated Circuits Conference*, pp. 75-78, May 1998.

[3] K.W. Kobayashi et al, "Sub-1.3 dB Noise Figure Direct Coupled MMIC LNAs using a high Current-Gain 1μm GaAs HBT Technology," *1997 IEEE GaAs IC Symposium Digest*, pp. 240 - 243, Oct. 1997.

[4] J.M Moniz, "Is SiGe the future of GaAs for RF applications?" *1997 IEEE GaAs IC Symposium Digest*, pp 229-231, Oct. 1997.

[5] H. Knapp, D. Zoshg, T. Meister, K. Aufinger, S. Boguth and L. Treitinger, "15 GHz Wideband Amplifier with 2.8 dB Noise Figure in SiGe Bipolar Technology," *2001 IEEE MTT-S Digest*, pp. 591-594.

[6] B. Razavi, *RF Microelectronics*, Prentice Hall Inc., Upper Saddle River, NJ, 1998.

[7] F. Bruccoleri, E.A.M Klumperink and B. Nauta, "Generating All Two-MOS-Transistor Amplifiers Leads to New Wide-Band LNAs," *IEEE Journal of Solid State Circuits*, Vol 36, No. 7, July 2001.

[8] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, New York, NY, 2001.

[9] O. Shana'a, I. Linscott, and L. Tyler, "Frequency-Scalable SiGe Bipolar RF Front-End Design" *IEEE Journal of Solid-State Circuits*, Vol 36, No. 6, June 2001.

[10] IBM Corp., *BiCMOS-6HP Model Reference Guide*, Chapter 6, Version: Nov. 15, 2001.

[11] Jazz Semiconductor, *Jazz SiGe60 Electrical Parameters*, Rev. 6.

[12] Cascade Microtech Inc. "Layout Rules for GHz Probing"
http://www.cmicro.com/pubs/Layout19.pdf.

[13] H. Ainspan et al., "A 6.25-GHz Low DC Power Low-Noise Amplifier in SiGe," *Proc. Of CSSC Conference*, 1997, pp177-180.

 [14] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, New York, NY, 2001.

Appendix

A.I Noise of Shunt Feedback Stage – Feedback Resistor
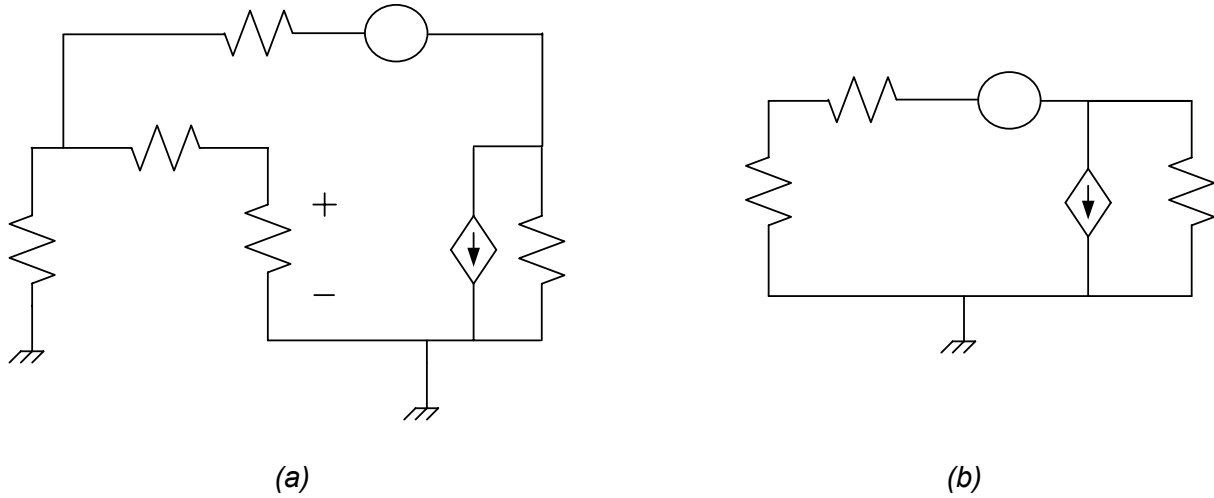

(a)   *(b)*

Figure A.1. Small Signal Circuit Model of Feedback Resistor R_F Noise Source used to find small signal transfer function from v_{nss-RF} to v_{OUT} (a). Since $r_{\pi 1} \gg r_{b1}$, r_{b1} is ignored and the parallel combination of R_S and $r_{\pi 1}$ is modeled by R_{base}'. Also, $r_o' = r_{o1} \| r_{oP1}$ (b).

$$R_F$$

Beginning with KCL at the output: $g_{m1}v_{IN} + \dfrac{v_{OUT}}{r_o'} + \dfrac{v_{OUT} - v_{nss-R_F}}{R_F + R_{base}'} = 0$

$$v_{IN}$$

In order to find v_{IN}, KCL at v_{IN} :

$$\frac{v_{IN}}{R_{base}'} = \frac{\left(v_{OUT} - v_{nss-R_F}\right) - v_{IN}}{R_F} \longrightarrow v_{IN}R_F\left(\frac{1}{R_{base}} + \frac{1}{R_F}\right) = v_{OUT} - v_{nss-R_F} \longrightarrow v_{IN} = \frac{v_{OUT} - v_{nss-RF}}{\dfrac{R_F}{R_{base}'} + 1}$$

$$R_S \qquad\qquad r_{b1} \qquad\qquad r_{\pi 1} \qquad\qquad v_{\pi 1}$$

Substituting back into the KCL at the output:

$$g_{m1}\frac{v_{OUT} - v_{nss-R_F}}{\dfrac{1}{R_{base}'}\left(R_F + R_{base}'\right)} + \frac{v_{OUT}}{r_o'} + \frac{v_{OUT} - v_{nss-R_F}}{R_F + R_{base}'} = 0$$

53

Assuming $r_\pi \gg R_S$, $R_{base}' \cong R_S$. Also, since g_{m1} is set to be $1/R_S$, the equation simplifies to:

$$\frac{2v_{OUT}}{R_F + R_S} + \frac{v_{OUT}}{r_o'} = \frac{2v_{nss-R_F}}{R_F + R_S}$$

Assuming $r_o' \gg R_F + R_S$, the equation simplifies further to $v_{out} = v_{nss-RF}$. Thus, $\overline{V_{no-RF}}^2 = \overline{V_{n-RF}}^2$

To refer this output noise power to the input, we divide by the gain, $-(g_{m1}R_F - 1)$ squared:

$$\overline{V_{ni-R_F}}^2 = \frac{\overline{V_{no-R_F}}^2}{\left(-g_{m1}R_F + 1\right)^2} = \frac{\overline{V_{n-R_F}}^2}{\left(-g_{m1}R_F + 1\right)^2}$$

A.II Noise of Shunt Feedback Stage – Transistors

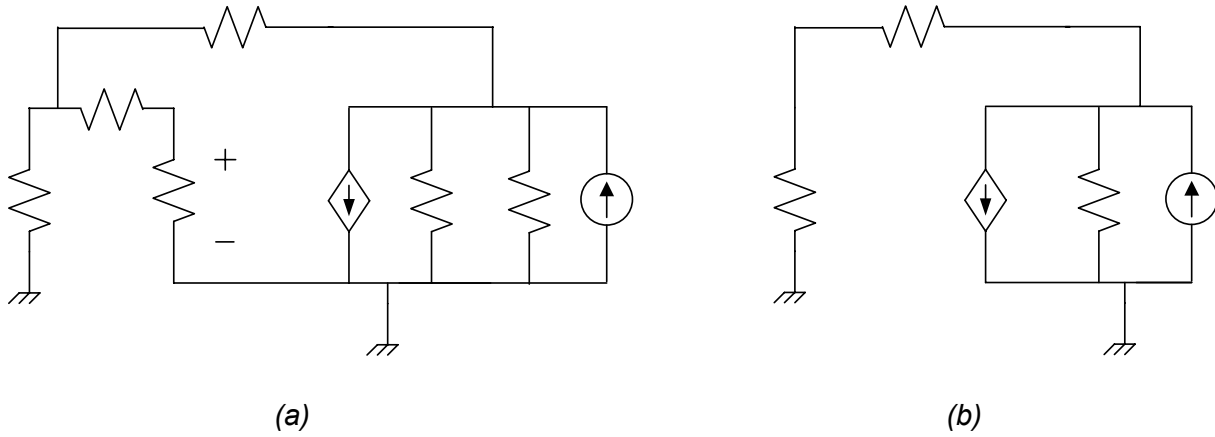*(a)*   *(b)*

Figure A.2. Small Signal Model of Transistor Noise Source used to find output noise transfer

function (a). Since $r_b \ll r_\pi$, redrawn circuit is shown (b), with $R_{base}' = R_S \| r_\pi$ and $r_o' = r_{o-Q1} \| r_{o-P1}$

The small-signal transistor noise sources, i_{nss-Q1} and i_{nss-P1}, are located in parallel to each other and thus the analysis to find the transfer function from the noise source to the output voltage is identical. Hereafter i_{nss} will represent a generic small signal noise current source from the output node to AC ground that can represent either of the transistors. KCL at the output node of A.2(b):

$$i_{nss} = \frac{v_{OUT}}{r_o' \| (R_F + R_{base}')} + g_m v_{IN}$$

To find v_{IN} in terms of v_{OUT}, a voltage divider equation is used: $v_{IN} = v_{OUT} * R_{base}' / (R_F + R_{base}')$. Substituting back into the previous equation:

$$i_{nss} = \frac{v_{OUT}}{r_o' \| (R_F + R_{base}')} + g_m v_{OUT} \frac{R_{base}'}{R_F + R_{base}'} \quad \longrightarrow \quad v_{OUT} = i_{nss} \frac{1}{\dfrac{1}{r_o' \| (R_F + R_{base}')} + \dfrac{g_m R_{base}'}{R_F + R_{base}'}}$$

Since $R_S \ll r_\pi$, $R_{base}' \cong R_S = 1/g_m$. Also, since $R_S + R_F \ll r_o'$, the parallel combination simplifies to just $R_S + R_F$. Substituting these principles back into the previous equation:

$$v_{OUT} = i_{nss} \frac{1}{\dfrac{1}{R_F + R_S} + \dfrac{1}{R_F + R_S}} \quad \longrightarrow \quad v_{OUT} = i_{nss} \frac{R_F + R_S}{2}$$

Thus, $\overline{V_{no-Q_1}}^2 = \overline{V_{no-P_1}}^2 = \overline{I_n}^2 \dfrac{(R_F + R_S)^2}{4}$. Referring this to the input by dividing by the gain sqaured:

$$\overline{V_{ni-Q_1}}^2 = \overline{V_{ni-P_1}}^2 = \frac{\overline{V_{no}}^2}{(-g_{m1} R_F + 1)^2} = \overline{I_n}^2 \frac{(R_F + R_S)^2}{4(-g_{m1} R_F + 1)^2}$$

A.III Noise of Emitter Follower Second Stage – Transistors

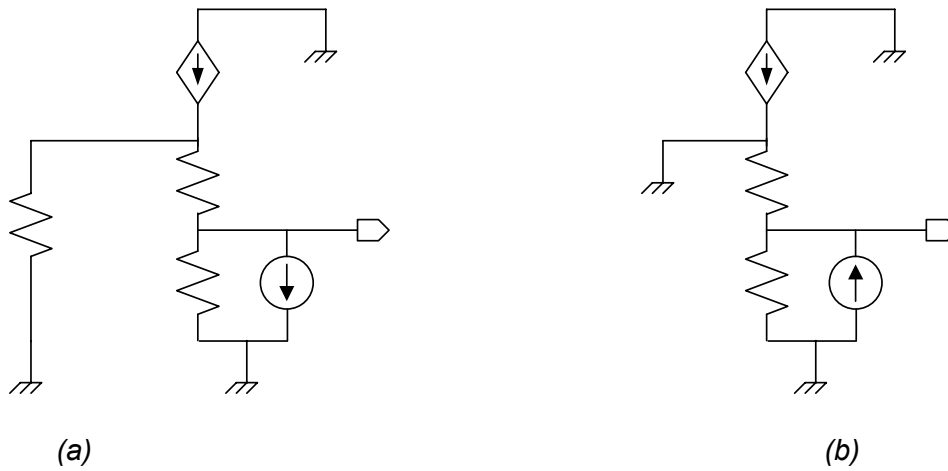(a)   (b)

Figure A.3 Small Signal Model of Transistor Noise Source used to find output noise transfer

function for either transistor shot noise of Q_2 or Q_3. $R_{o\text{-}S1}$ is the output resistance of the

first stage, equal to $(R_F+R_S)/2$ (a). Reflecting this impedance into the emitter, the circuit

shown in (b) is drawn, where $r_e' = r_{e3} + R_{o\text{-}S1} / (\beta+1)$.

The small-signal transistor noise sources, $i_{nss\text{-}Q2}$ and $i_{nss\text{-}Q3}$, are located in parallel to each other and thus the analysis to find the transfer function from the noise source to the output voltage is identical. Hereafter i_{nss} will represent a small signal noise current source from the output node V_{OUT1} to AC ground that can represent either of the transistors. KCL at the output node of Figure A.3(b):

$R_{O\text{-}S1}$

r_{e3}

$$i_{nss} = \frac{v_{OUT}}{r_{o3} \| r_{o2}} + \frac{v_{OUT}}{r_e'} \qquad \longrightarrow \qquad v_{OUT} = i_{nss} \frac{1}{\dfrac{1}{r_{o3} \| r_{o2}} + \dfrac{1}{r_e'}}$$

$r_{o3} \| r_{o2}$

Since R_{o-S1} is equal to $(R_F + R_S)/2$ this quantity is not very large (~200 Ω) and when divided by β it is negligible compared with r_{e3}. Also, since $r_{o3} \| r_{o2} >> r_{e3}$ the denominator becomes $1/r_{e3}$ and the final transfer function is: $v_{OUT} = i_n{}^*r_{e3} = i_n{}^*\alpha_3/g_{m3}$. Since α_3 is approximately equal to one for large β, the final transfer function is $v_{OUT} = i_n{}^*1/g_{m3}$.

Thus, $\overline{V_{no-Q_2}}^2 = \overline{V_{no-Q_3}}^2 = \overline{I_n}^2 \dfrac{1}{g_{m3}^2}$. Referring this to the input by dividing by the gain squared:

$$\overline{V_{ni-Q_2}}^2 = \overline{V_{ni-Q_3}}^2 = \frac{\overline{V_{no}}^2}{\left(-g_{m1}R_F + 1\right)^2} = \overline{I_n}^2 \frac{1}{g_{m3}^2\left(-g_{m1}R_F + 1\right)^2}$$

To find the noise factor, all the input referred noise sources are summed. Using the equation above for the input referred noise of Q_2 and Q_3, equation 5 for R_F and equation 6 for Q_1 and P_1 the noise factor is (expanding on the generic noise factor equation from equation 8):

$$\frac{4kT\Delta f R_S + \dfrac{\overline{V_{n-R_F}}^2}{(-g_{m1}R_F + 1)^2} + \dfrac{\overline{I_{n-Q_1}}^2(R_F + R_S)^2}{4(-g_{m1}R_F + 1)^2} + \dfrac{\overline{I_{n-P_1}}^2(R_F + R_S)^2}{4(-g_{m1}R_F + 1)^2} + \dfrac{\overline{I_{n-Q_2}}^2}{g_{m3}^2(-g_{m1}R_F + 1)^2} + \dfrac{\overline{I_{n-Q_3}}^2}{g_{m3}^2(-g_{m1}R_F + 1)^2}}{4kT\Delta f R_S}$$

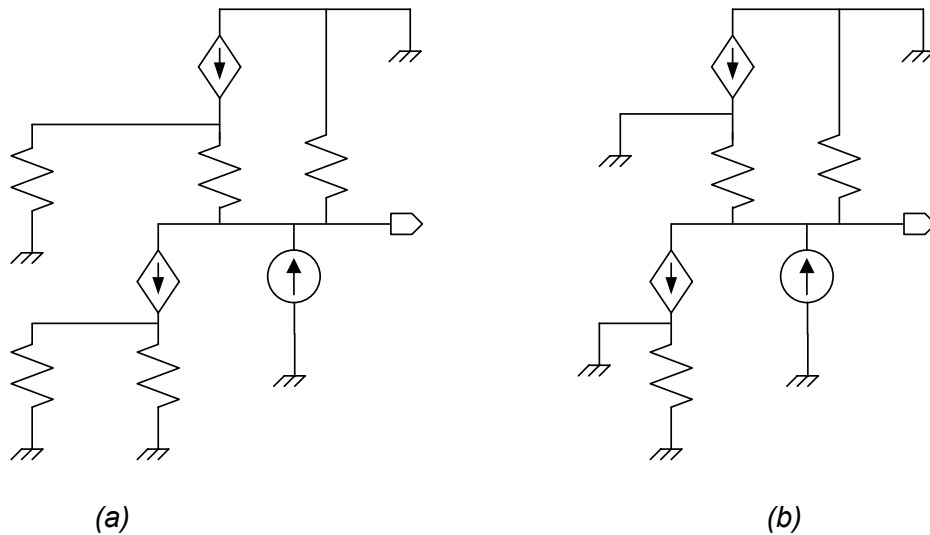## A.IV Noise of Summer/Amplifier Second Stage – Transistors

(a)   *(b)*

Figure A.4 Small Signal Model of Transistor Noise Source used to find output noise transfer

function for either transistor shot noise of Q_2 or Q_3. $R_{o\text{-}S1}$ is the output resistance of the

first stage, equal to $(R_F+R_S)/2$ (a). Reflecting this impedance into the emitter of Q_3 and

reflecting the source impedance R_S into the emitter of Q_2, the circuit shown in (b) is drawn,

where $r_{e3}' = r_{e3} + R_{o\text{-}S1} / (\beta+1)$, $r_{e2}' = r_{e2}' + R_S / (\beta+1)$ and $r_o' = r_{o2} \,||\, r_{o3} \,||\, r_{oP2}$

The small-signal transistor noise sources, $i_{nss\text{-}Q2}$, $i_{nss\text{-}Q3}$ and $i_{nss\text{-}Q4}$ are located in parallel to each

other and thus the analysis to find the transfer function from the noise source to the output

voltage is identical. Hereafter i_{nss} will represent a generic small signal noise current source from

the output node to AC ground that can represent any of the transistor small signal noise

sources. KCL at the output node of Figure A.4(b):

$$i_{nss} = \frac{v_{OUT}}{r_o'} + \frac{v_{OUT}}{r_{e3}'} + \alpha_2 i_{e2}$$

Since i_{e2} is equal to zero, $r_{e3}' \cong r_{e3}$ from section A.3, $r_o' \gg r_{e3}$ and α_3 is approximately equal to one, the transfer function becomes:

$$i_{nss} = v_{OUT}\left(\frac{1}{r_o'} + \frac{1}{r_{e3}}\right) \quad \longrightarrow \quad v_{OUT} = i_{nss} * r_{e3} \longrightarrow \quad v_{OUT} = i_{nss}\frac{1}{g_{m3}}$$

Thus, $\overline{V_{no-Q_2}}^2 = \overline{V_{no-Q_3}}^2 = \overline{V_{no-P_2}}^2 = \overline{I_n}^2\frac{1}{g_{m3}^2}$. Referring this to the input by dividing by the gain squared:

$$\overline{V_{ni-Q_2}}^2 = \overline{V_{ni-Q_3}}^2 = \overline{V_{ni-P_2}}^2 = \frac{\overline{V_{no}}^2}{\left((-g_{m1}R_F + 1) - \frac{g_{m2}}{g_{m3}}\right)^2} = \overline{I_n}^2\frac{1}{g_{m3}^2\left((-g_{m1}R_F + 1) - \frac{g_{m2}}{g_{m3}}\right)^2}$$

To find the noise factor, all the input referred noise sources are summed. Using the equation above for the input referred noise of Q_2 and Q_3, and equation 5 for R_F the noise factor is shown below (expanding on the generic noise factor equation from equation 8). Note the noise from Q_1 and P_1 has been canceled.

$$\frac{4kT\Delta f R_S + \dfrac{\overline{V_{n-R_F}}^2}{(-g_{m1}R_F + 1)^2} + \dfrac{\overline{I_{n-Q_2}}^2}{g_{m3}^2\left((-g_{m1}R_F + 1) - \frac{g_{m2}}{g_{m3}}\right)^2} + \dfrac{\overline{I_{n-Q_3}}^2}{g_{m3}^2\left((-g_{m1}R_F + 1) - \frac{g_{m2}}{g_{m3}}\right)^2} + \dfrac{\overline{I_{n-P_2}}^2}{g_{m3}^2\left((-g_{m1}R_F + 1) - \frac{g_{m2}}{g_{m3}}\right)^2}}{4kT\Delta f R_S}$$

A.V Checklist before Fabrication

1. Before layout, test plan developed and simulations run with model of signal path from Agilent signal source to Agilent measurement equipment as well as bias lines from circuit to power supply.

2. Layout done taking care to place active devices in regular patterns, with substrate contacts and deep trench isolation around them if possible. Dummy cells are also important if matching or exact sizing is needed.

3. Bondpads placed with at least 200μm pitch. If circuit is not being post-processed, 120μm bondpads are suggested. 200μm pads if it will be.

4. Probes to be used with RF positioners (GSG, GSGSG, Multiple contact DC probe {EyePass}) may only be placed to the West, East and North in Circuit. Bondpads should be placed such that they do not cross the path of a GSG.

5. On-Chip decoupling capacitors to ground for all bias lines.

6. Multiple ground contacts on chip.

7. Simulation with extracted circuit and testing models completed and results ok

A.VI PCB Board

1. Multiple capacitor sizes on each bias line (see section III.3)

2. No solder mask so all traces are accessible. Gold plating suggested (easier bonding)

3. Before bonding, solder all components on and wash bondpads with Isopropyl alcohol, then rinse with water. Allow to dry to ensure clean bonding surface.

4. Using one side of the board (no bottom routing) is preferable such that the board can be placed directly on a vacuum chuck because of its smooth bottom surface.

5. Use silver paste, not epoxy. Place as little paste as possible so it doesn't glob.

A.VII   Making Measurements

1. GSG Loss Measurement

A.   Connect a 3.5mm cable (Agilent #11500F) between the PSG and PSA

B.   Sweep frequency and record the power level in the PSA

C.   Connect the GSGs on a THRU pad (signal can travel from one to another), a 3.5mm cable from the PSG to the input GSG cable and the output GSG to the PSA as in Figure A.5.

D.   Sweep frequency and record the power level in the PSA. The difference between this measurement and measurement from B is the loss through both GSGs. Divide by two to obtain the loss through one GSG.
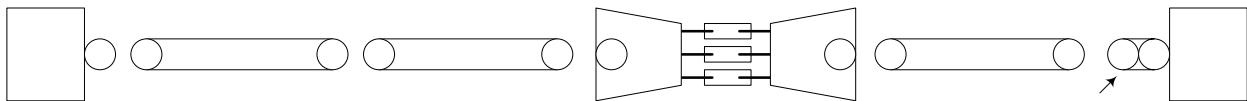

Figure A.5 Loss Measurement Setup

2. Noise Figure

A.   Set the PSA to use the Noise Figure Personality, connect the noise source to the PSA input directly & complete the ENR table.

B.   Input the cable/probe losses from section A.VII.1 at various frequencies into the Loss Compensation table for both 'Before DUT' and 'After DUT'.

C.   Set the Frequency Range, number of points, averaging & then calibrate

D.   Connect the noise source to input of circuit, and the PSA to the output (Figure A.6). The noise will be measured and displayed using the Noise Figure personality. It can be saved as a graph or table of values.

3. **IIP3**

    A. Connect everything as in Figure A.6 below and connect OUT to the PSA

    B. Set the amplitudes of the PSGs to be equal, their frequencies to be very close together (depending on the communications standard this can be any number from 1 MHz to 20 MHz) and measure the amplitudes of the two tones through the spectrum analyzer at various input power levels (Note that the PSG amplitudes should always be identical while sweeping). When connected to the circuit, the actual input power at the input will be these values plus the loss of one GSG cable (taken from A.VII.1).
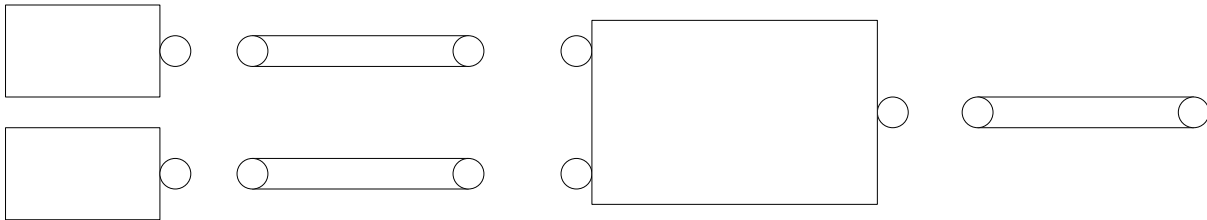
Figure A.6 IIP3 Testing Setup

    C. Connect OUT to one of the GSG cables and place the GSG probe on the input of the Device Under Test (DUT). Connect the other GSG cable to the PSA and the GSG probe to the output of the circuit.

    D. Measure the output on the spectrum analyzer again. There should be four peaks as shown in Figure A.7. The middle two are the input tones while the outside two are the third order modulated tones. Record the amplitudes of both sets of tones while sweeping the power level for at least three data points (remember to keep the two PSGs at the same power level). Two low of an input power and the third order modulation will be lower than the noise

floor. Too high of a power and the circuit may be in a non-linear region.

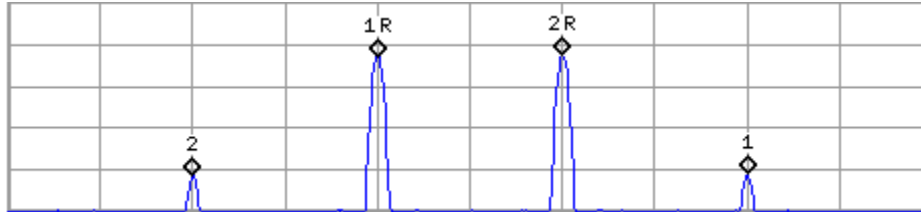Sweeping from -40 dBm to -25 dBm will usually be a good range.

Figure A.7 IIP3 Measurement on Spectrum Analyzer

E. Plot the amplitude of the actual circuit input power vs. third order tone and first order tone. The value of the X axis (actual circuit input power) at the intersection point of the two curves is the IIP3 value. For more details see the numerical example below in Table A.1 of a hypothetical 10 dB gain amplifier where there is 1dB of loss through each GSG cable + probe and 3 dB of loss through the setup of Figure A.6. All numbers are in dBm. The plot of 'Actual Circuit Input Power' vs. 1st & 3rd Order magnitudes can be seen in Figure A.8 where the IIP3 value is -16.5 dBm.

PSG Amplitude	Step B Amplitude	Actual Circuit Input Power	Step D 1st Order	Step D 3rd Order
-25	-28	-29	-20	-45
-30	-33	-34	-25	-60
-35	-38	-39	-30	-75
-40	-43	-44	-35	-90

Table A.1 IIP3 measurements of hypothetical amplifier with 10 dB gain, using test setup with

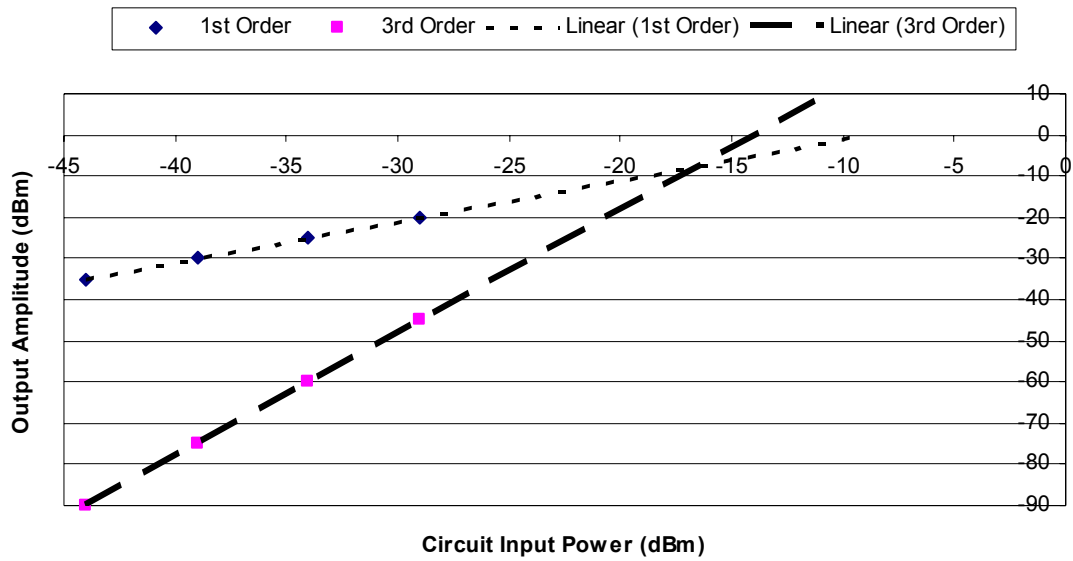*3 dB loss through combiner and 1 dB through each GSG cable*

Figure A.8 Hypothetical IIP3 Calculation from Table A.1 showing a value of 16.5 dBm

A.VIII   Cascade Microtech Probestation Test Setups

1. Network Analyzer (S-Parameters, 1dB Compression Point)

A. Agilent 3.5mm (f) to 2.92 mm (m) adaptors (Part # 11904-60004) are already attached to the Network Analyzer. Connect the input GSG cable directly to Port 1 and the output GSG cable directly to port 2 using a 3.5mm Torque Wrench (0.9 N-m, Agilent Part # 8710-1765)
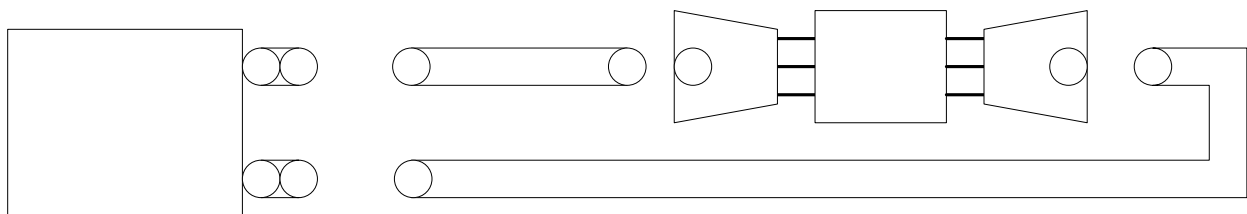

Figure A.9 Network Analyzer Test Setup

2. Spectrum Analyzer (Noise Figure)

    A. Connect the +28 V Output from the rear of the Spectrum Analyzer to the 346B Noise Source via a BNC cable. The other side of the 346B is an RF connection that gets connected to the input GSG cable, and therefore to the input of the DUT.

    B. Connect the output GSG cable to a SMA to SMA adapter (Agilent Part # 1250-1159). Connect the other side of the adapter to the Spectrum Analyzer RF input. Use the SMA torque wrench (0.56 N-m, Agilent Part # 8710-1582) when tightening this piece.
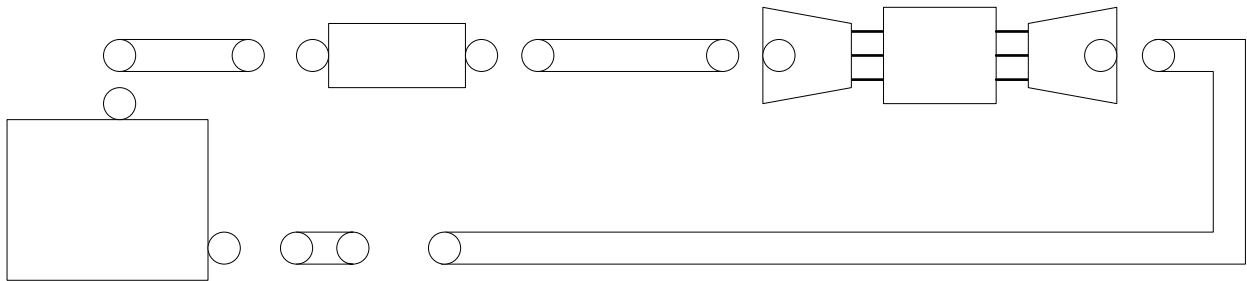

Figure A.10 Spectrum Analyzer Noise Figure Personality Test Setup

A.IX   CDS Directory Structure

1. **IBM 6HP – SRC_Phase2**

    A. DiffAmp – Differential Amplifier to amplify mixer output

    B. DiffAmp_tb – Testbench for Differential Amplifier

    C. LNA_Mixer_expr – Full experiment with LNA connected to Mixer (+pads)

    D. MixerAmp – Pre-Amp and Differential Amplifier connected in series

    E. MixerAmp_expr – Full experiment to test MixerAmp (+pads)

    F. MixerAmp_tb – Testbench for MixerAmp

    G. Mixer_expr – Two experiments in one: Just the mixer connected to pads &

      The mixer connected to MixerAmp, then to pads.

    H. PreAmp – Pre-Amplifier used at mixer output

    I. PreAmp_tb – Testbench for Pre-Amplifier

    J. Wideband_LNA – Wideband LNA only

    K. Wideband_LNA_expr – Full LNA experiment including bypass caps + pads

    L. Wideband_LNA_expr_tb – Full model of measurement setup (section III.4)

    M. Wideband_LNA_fill –layout of LNA with top-metal fill (section III.2)

    N. Wideband_LNA_tb – Testbench for LNA alone

2. **Jazz – jz60_002**

    A. FE_Wideband_LNA – Wideband LNA only, including top cover

    B. FE_Wideband_LNA_expr – Full LNA experiment including pads

    C. FE_Wideband_LNA_expr_tb – Full model of measurement setup (sect. III.4)

    D. FE_Wideband_LNA_tb – Testbench for LNA alone