Design and Simulation of A CMOS-MEMS Accelerometer

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1. INTRODUCTION

With the development of MicroElectroMechanicalSystems (MEMS), inertial instruments have seen significant progress over the past decades. The advantages of low-cost, low-power, small size, batch fabrication makes MEMS-based inertial sensors have a wide range of applications in automotive, consumer, computer, and navigation markets. As the most mature MEMS-based inertial sensor application, current MEMS accelerometers have the highest degree of integration, with sensing elements and electronic interface circuitry on a single chip [1, 2, 3].

In a conventional polysilicon surface micromachining process[4], microaccelerometers are made from custom processes combining polysilicon surface micromachining and electronic circuits processes. Microstructures are separated from electronics by around 100μm due to process limitations, which wastes significant amount of silicon area. Parasitic capacitance between the structural layer to the substrate can be around 50 pF for a typical inertial sensor design. Interconnection between microstructures and electronics is implemented by the polysilicon layer or by diffusion with large resistance and parasitic capacitance to substrate, which result in large wiring noise and signal attenuation. Extra micromachining process steps usually involve performance and yield compromises, and are incompatible with standard IC technology.

The accelerometer described in this report is designed with the CMOS-MEMS technology developed at Carnegie Mellon[5]. The process flow, shown in Figure 1.1, incorporates microstructures with the Hewlett-Packard 0.5μm three-metal n-well CMOS process. After the foundry CMOS processing, two steps of dry etches, with the top metal layer as etch resistant mask, are performed to create microstructures. An anisotropic reactive ion etch (RIE) with CHF_3/O_2 is first performed to etch away exposed oxides, and form microstructural sidewalls. This step is followed by a more isotropic RIE with SF_6/O_2 to etch bulk silicon and release the microstructures from substrate. Dry etches eliminate sticking problems associated with competing wet-etch release processes.

Comparatively, CMOS-MEMS technology has many advantages over polysilicon surface micromachining processes. Compatibility with conventional CMOS technology enables fast, repeatable, reliable, and economical fabrication of MEMS devices integrated with conventional CMOS. Microstructures can be integrated as close as 12 μm from on-chip electronics limited by the silicon undercuts. Since the mask metal layer is defined by lithography in the CMOS process, the minimum microstructure feature size is 1.5μm and scales with CMOS technology. Structural layers are released with a gap of about 20 μm above

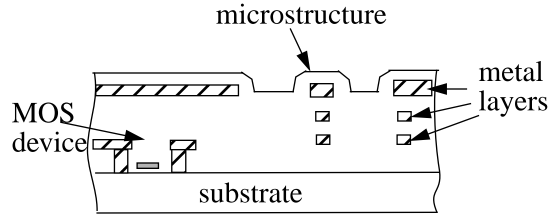


Figure 1.1(a) after foundry CMOS process

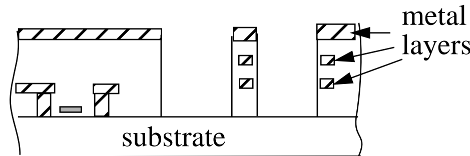


Figure 1.1(b) after dielectric etching

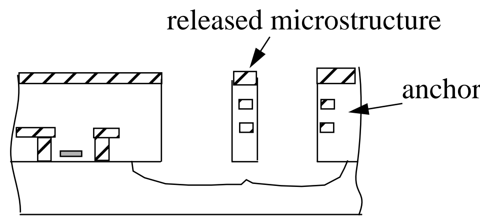


Figure 1.1(c) after bulk silicon etching

Figure 1.1: CMOS-MEMS process flow.

the substrate, providing a much smaller parasitic capacitance to the substrate. Aluminum interconnect eliminates thermal noise caused by wiring resistance. Multiple conductors can be built into structural layers, which allow novel and flexible design, such as fully differential capacitive sensors, self-actuating springs and gimbaled gyroscope designs[12]. Such designs can not be implemented in homogeneous conducting structural layers such as those in polysilicon technology.

In this report, design issues are addressed with the emphasis on exploiting advantages and benefits provided by CMOS-MEMS technology, and overcoming potential difficulties.

In Chapter 2, the design of the sensing element is presented. There are many novel features in this design, which take advantage of the CMOS-MEMS technology, including a fully differential capacitive sensing interface, and common centroid topology. To address the curling problem associated with the composite structural layers, a rigid frame is included to match curl of rotator fingers and stator fingers to first order. The rigid frame also reduces the parasitic capacitance by suspending signal paths far above the substrate. All major characteristics of the sensing element design are covered including Brownian noise, sensi-

tivity, resonant frequency, damping factor, electrical spring softening, gap capacitors, capacitive bridge interface, and electrostatic force feedback actuators. Finite-element analysis with Abaqus[16] is also presented.

Chapter 3 focuses on the design of the electronic interface circuits. A fully differential interface is presented. Front-end circuitry consisting of buffers and preamplifiers enables isolation of the sensing nodes, preamplification of the signal and provides design flexibility for the later stages. In the demodulator and preamplifier design, switched-capacitor techniques are used with correlated double sampling to remove offset and errors. A fully differential wide-swing folded-cascode amplifier with dynamic common-mode feedback is designed. Noise contributions are calculated thoroughly from different sources.

Chapter 4 details the simulation of the accelerometer system using Hspice[14]. Approaches combining mechanical and electrical simulation are developed to predict the performance of the complex system.

Chapter 5 describes tests methods and experimental results of two fabricated accelerometers. Major parameters of the sensor are measured. Experimental results point out some design issues such as spring design and needs of offset trimming circuitry.

Chapter 6 concludes the overall work and outlines the directions of future work.

Acknowledgments

I am grateful to my advisor, Professor Gary Fedder, for his guidance, encouragement and support throughout this project. I have grown academically as well as personally during the course of this interaction. I thank Professor Rick Carley for his guidance on circuit design and for reviewing the manuscript. I also thank Suresh Santhanam for releasing the devices and thank my fellow students at Carnegie Mellon: Steve Eagle, Mike Kranz, Hasnain Lakdawala, Mike Lu, Jan Vandemeer, Yong Zhou, Xu Zhu, for helpful discussions. Finally I will heartily thank my wife Connie for her love and her full support for me all the time.

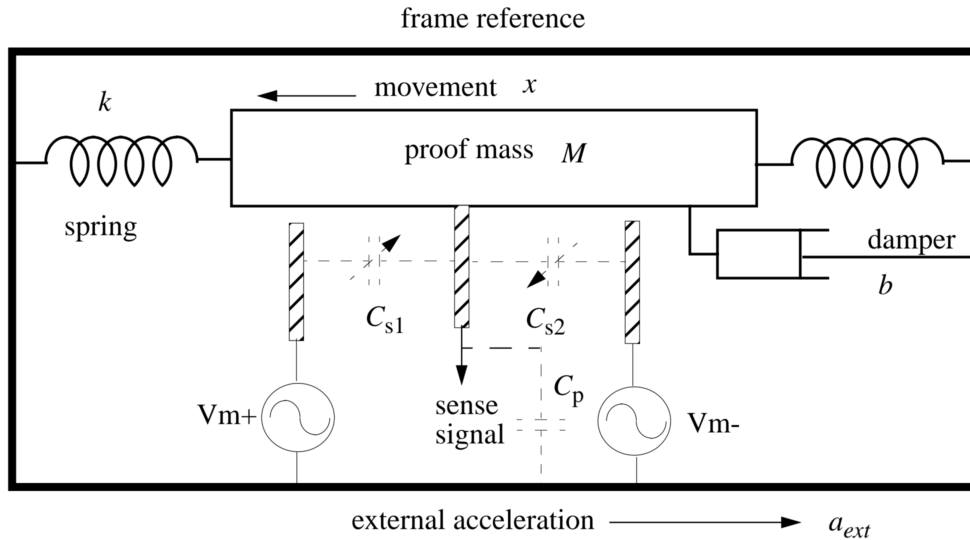


Figure 2.1: Schematic of a capacitive accelerometer.

2. SENSING ELEMENT DESIGN

2.1 Overview

A simplified schematic of a capacitive microaccelerometer is shown in Figure 2.1. The central part of the accelerometer is a suspended micromechanical proofmass, which acts as the sensing element. When an external acceleration is applied, the proofmass will move with respect to the moving frame of reference. The acceleration is inferred from the displacement of the proofmass which can be measured by several means. For the capacitive sensing approach, the displacement is detected by measuring the capacitance change between the proofmass and adjacent fixed electrodes. Low parasitic capacitance achieved from monolithic integration are the key to maximizing the performance with this technique.

The most commonly used capacitive sense interface is a single-ended half-bridge interface shown in Figure 2.2(a)[1]. Change in capacitance can be measured by driving the ends of the bridge and taking the central node as the output. Fully differential interfaces are always preferred to their single-ended counterparts because of better power supply rejection and first-order cancellation of substrate coupling. In previous work, differential capacitive sense interfaces have been implemented with polysilicon surface micromachining processes. In some designs displacement is sensed with a capacitive half-bridge by modulating the central node (i.e., the proofmass) and connecting the two fixed ends to a differential position sense interface (Figure 2.2(b))[3]. Since there is only one modulation node instead of two differential ones,

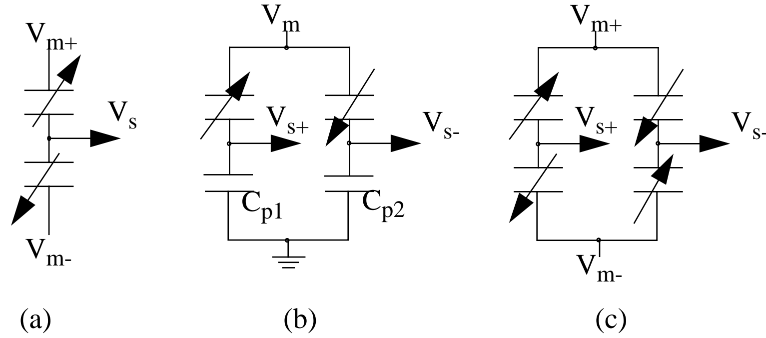


Figure 2.2: Different schemes of capacitive interfaces

a significant common-mode signal will appear at the input nodes of the differential interface. This scheme requires special input common-mode feedback (CMFB) circuitry to improve input common-mode rejection ratio (CMRR) and dynamic range, however, at the expense of noise and bandwidth[6]. Mismatch between two parasitic capacitors (C_{p1}, C_{p2}) results in output offset which can be a great source of drift over environmental variations, such temperature and aging.

A fully differential full-bridge capacitive sense interface, shown in Figure 2.2(c), is described in this chapter. Taking advantage of multiple conductors in the structural layer, this topology can approximately double the sensitivity of half-bridge topology with the same value of sensing capacitance. Since the interface is truly fully differential, very high CMRR can be achieved at the outputs. There is no need for extra circuitry for input CMFB at the inputs of sensing electronics. In the layout realization, common-centroid design can improve matching and further reduce offset.

A unique suspended rigid frame illustrated in Figure 2.7, is included in the sensing element design to provide several advantages, including minimized parasitic capacitance from the signal path to the substrate, and first order curl matching between the rotor fingers and the stator fingers as discussed in section 2.3.

To implement balanced force feedback and for self-test purposes, four electrostatic force actuators are placed on the corners of the sensor. Actuation fingers are separated and shielded from sensing fingers to simplify clock design and minimize possible feedthrough.

2.2 Mechanical Design and Analysis

The schematic shown in Figure 2.1 shows the mechanical parameters for the sensing element. The differential equation for the displacement x as a function of external acceleration is that of a second-order mass-spring-damper system:

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = ma_{ext} \tag{2.1}$$

where k is the spring constant, b is the damping coefficient, and a_{ext} is the external acceleration. In Laplace transform notation, the above equation converts to a second-order transfer function:

$$\frac{X(s)}{A(s)} = \frac{1}{s^2 + s\frac{b}{m} + \frac{k}{m}} = \frac{1}{s^2 + s\frac{\omega_r}{Q} + \omega_r^2} \tag{2.2}$$

where $\omega_r = \sqrt{k/m}$ is the resonant frequency and $Q = \omega_r m/b$ is the quality factor. At low frequency ($\omega << \omega_r$),

$$\frac{X}{A} \approx \frac{1}{\omega_r^2} \tag{2.3}$$

The sensitivity is inversely proportional to the square of the resonant frequency which means the lower the resonant frequency the higher the sensitivity. But actually, the lower limit of resonant frequency is bounded by many factors such as the mechanical shock resistance, the achievable lowest spring constant, the highest possible effective mass, and manufacturability.

2.2.1 Spring Design

An open-end folded-beam suspension is shown in Figure 2.3. One advantage of this topology is that the residual stress can be released and will not affect the spring constant. The same topology with more turns can provide a lower spring constant, and thus higher sensitivity. The spring constant of this structure, to the first order, is found to be:

$$k_y = Eh\left(\frac{w}{l}\right)^3/2 \tag{2.4}$$

where E is Young's modulus, h is the thickness, w is the width and l is the length of the spring structure.

To have stable sensor parameters, the spring constant must be well controlled. According to the

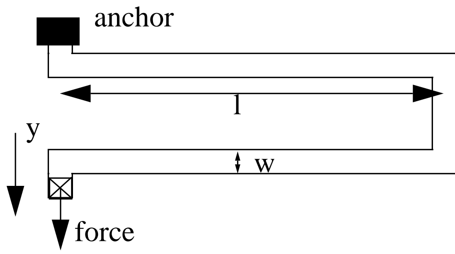


Figure 2.3: Open-end spring

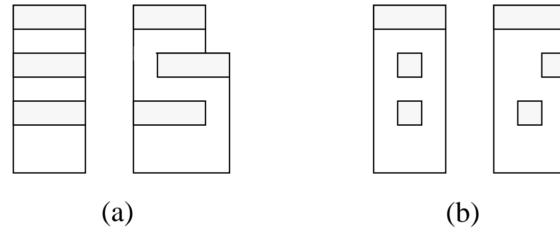


Figure 2.4: Effect of misalignment of metal layers

above formula, the spring constant is proportional to the third power of the width, which, therefore, is the key parameter to be controlled. The width is determined by the width of the widest metal layer. If the three metal layers in the beam have the same width, then any misalignment among them will cause variation of the beam width (Figure 2.4(a)). To eliminate dependence on misalignment, which can be around 0.1μm, widths of metal3 line are restricted to have 0.3μm overlap on both sides over the underlying metal1 and metal2 lines. With this restriction as a design rule, beam width is solely determined by the width of top metal3 line as shown in Figure 2.4(b). Even though beam width can be controlled in this way, the misalignment of metal layers can cause lateral bending of the beams, due to lateral residual stress gradient in the beam. In accelerometer design, lateral bending of beams can cause offset.

Figure 2.5 shows finite element analysis results of the resonant modes of a lateral accelerometer. The simulation is done with Abaqus[16]. The dimension of the sensor is 300μm by 400 μm, with a proofmass of 0.47μg. Two-turn open-end springs are used in the design. A rigid frame is also included in the model.

Another important factor that has to be taken into account for accurate spring constant estimation is

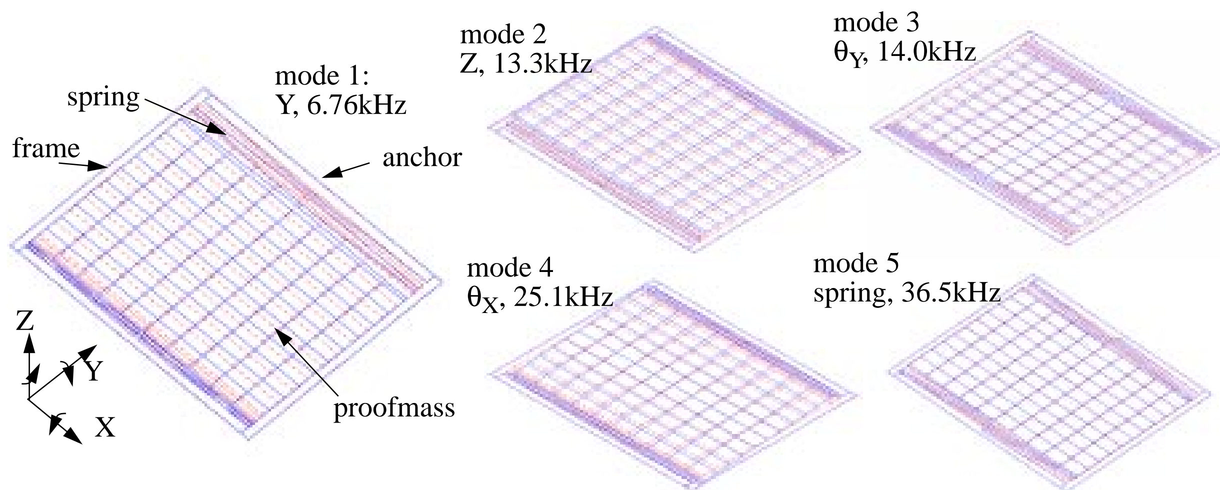


Figure 2.5: Finite element analysis results of the resonant modes of the sensor.

electrical spring softening caused by modulation voltages as will be discussed in section 2.5.

2.2.2 Damping and Quality Factor:

There are two categories of damping mechanisms with the design. Structural damping is caused by friction within composite structural layers. The second category is viscous air damping which, at atmospheric pressure, is several orders of magnitude higher than structural damping. Damping caused by air flow between the rotor and stator fingers, and at the edges of the proofmass is the major damping mechanism. Since the proofmass is relatively far above the substrate, Couette-flow damping, due to shear flow between parallel plates, is relatively small. For the lateral accelerometer, squeeze-film damping, which occurs when the air gap between two closely placed parallel surfaces changes, is not critical either. Hagen-Poiseuille flow[7] is assumed to model damping with narrow width gaps. The damping coefficient between a single comb finger gap is given by:

$$b = 7.2\mu l\left(\frac{t}{d}\right)^3 \qquad (2.5)$$

where μ is effective viscosity of air, t is finger thickness, d is finger gap, and l is finger length. At 760 torr and 20°C μ is 1.56e-5 kg/m.s. For the symmetric design in this report, with gap number of 28, the calculated damping coefficient is 2.7×10^{-6} kg/s, and the corresponding Q is 7, which is close to the measured Q of 8. Reducing the damping coefficient by changing the finger size or gap is at odds with increasing sensing sensitivity. Vacuum packaging can reduce damping and increase the quality factor significantly.

2.3 Vertical Stress Gradient Compensation with Curl Matching Technique

Due to the composite nature of the CMOS-MEMS structural layer, structures experience more vertical stress gradient than that seen in optimized polysilicon processes. The typical radius of curvature of the structural layer can be relatively small, around 4 mm, compared with a radius of curvature of 800 mm in a polysilicon surface MEMS technology[9].

With given radius of curvature and beam length, displacement of the beam tip caused by curl is,

$$h = R - R\cos\left(\frac{l}{R}\right) \qquad (2.6)$$

For example, for R=4mm, and l=200μm, the beam curls out-of-plane by 5μm, which is equal to the beam thickness of 5μm in CMOS-MEMS process.

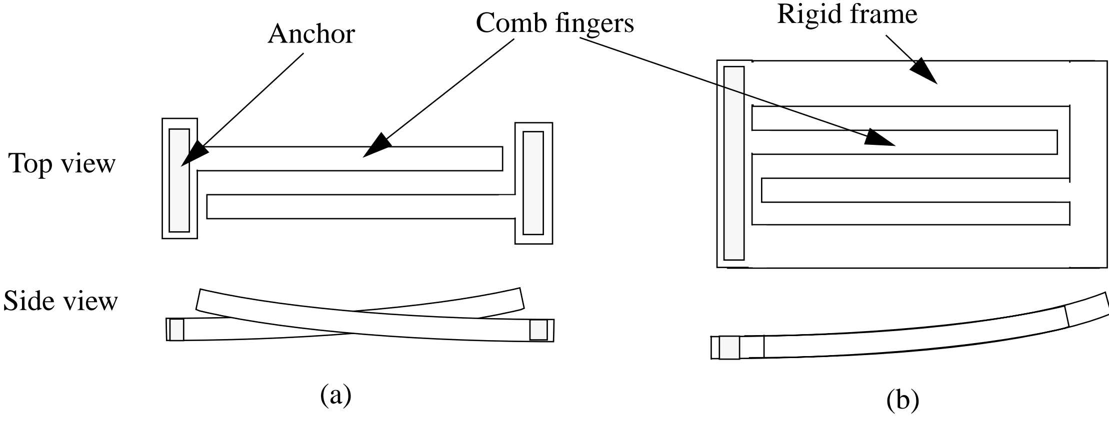


Figure 2.6: Curl matching of micro comb fingers

Figure 2.6(a) illustrates two interdigitated fingers anchored on the substrate at opposite ends. If the fingers are sufficiently long, then both fingers will curl out-of-plane. Similarly, in accelerometer design, both rotor fingers and stator fingers will curl out-of-plane and cross, reducing the effective sensing capacitance. Moreover, the mismatch can drift dramatically with environmental variations such as temperature and moisture, increasing the overall sensor drift. Unfortunately, alleviating the curling problem by limiting structure size will reduce effective mass and increase the Brownian noise floor. Thus a special technique targeting good curl matching is demanded. If the structure is modified as in Figure 2.6(b), making the finger on the right anchored on a frame curling in line with the left finger, then the interdigitated fingers will curl out-of-plane in line, and achieve good curl matching.

To achieve matching of curl to first order in the accelerometer, both the suspension springs and the stator fingers are anchored to a rigid frame instead of the substrate, as shown in Figure 2.7. The rigid frame, springs, proof-mass plate, rotor fingers and stator fingers are made from the same type of structural layer to match stress gradient. The side view of the device shows a good curl matching of the fabricated device (Figure 2.8).

A rigid frame also provides the benefit of low parasitic capacitance from the sensing nodes to the substrate, since the rigid frame is released from the substrate and has much less area compared to the proof mass. An additional benefit is the compatibility with micro-oven control. Since the rigid frame thermally isolates the sensing element from other parts on the chip, thermal gradient effects on the suspension springs are avoided.

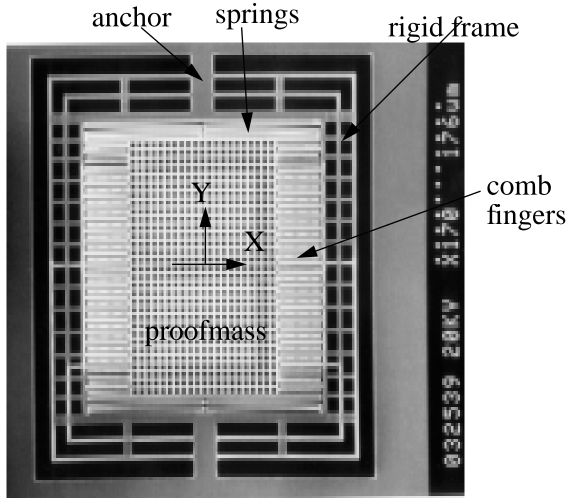


Figure 2.7: Top-view of the accelerometer

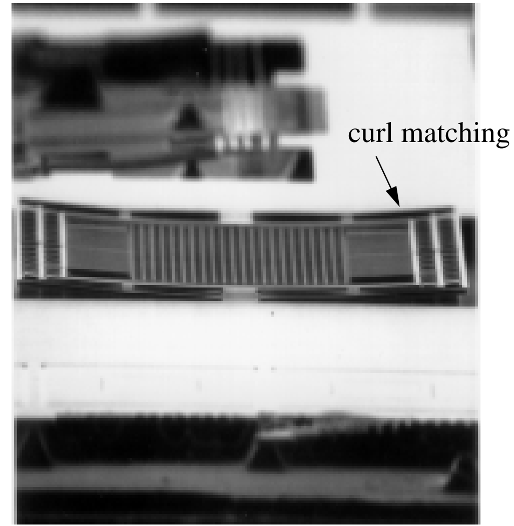


Figure 2.8: Side-view shows curl matching

The frame must be rigid compared with the compliance of the springs, otherwise the stator fingers may have displacement with respect to the input acceleration signal. As shown in Figure 2.7, the residual stress in the vertical beams of the frame is released by bending the horizontal beams very little in Y direction. There is no lateral buckling, which is proved by Abaqus simulation and fabricated devices.

2.4 Fully Differential Capacitive Bridge Interface

The capacitive bridge interface to the accelerometer has a novel design. It provides fully differential signals to the following electronics, with very good CMRR compared with previous work, eliminating the need for common-mode feedback circuits at the front end. A common-centroid design cancels the cross-axis and translational coupling to first order, and reduces offset among sensing capacitors.

Multiple conductors in the structural layer make this design topology realizable. With CMOS-MEMS technology, isolated interconnect can be routed within the proofmass, allowing much more flexible sensor design. High-impedance sensing nodes are connected to stationary fingers on the rigid frame, while low-impedance modulation nodes are connected to rotor fingers on the proofmass. Since the frame is released from the substrate, signal wires are short. This topology reduces parasitic capacitance to substrate and coupling from other signals like modulation signals and drive signals.

Schematics of these two designs are shown in Figure 2.9. The symmetric topology (Figure 2.9(a)) has the advantages of simplicity and less parasitic capacitance along with the disadvantage that a cross-axis acceleration signal generates a common-mode output. The common-centroid design (Figure 2.9(b)) has

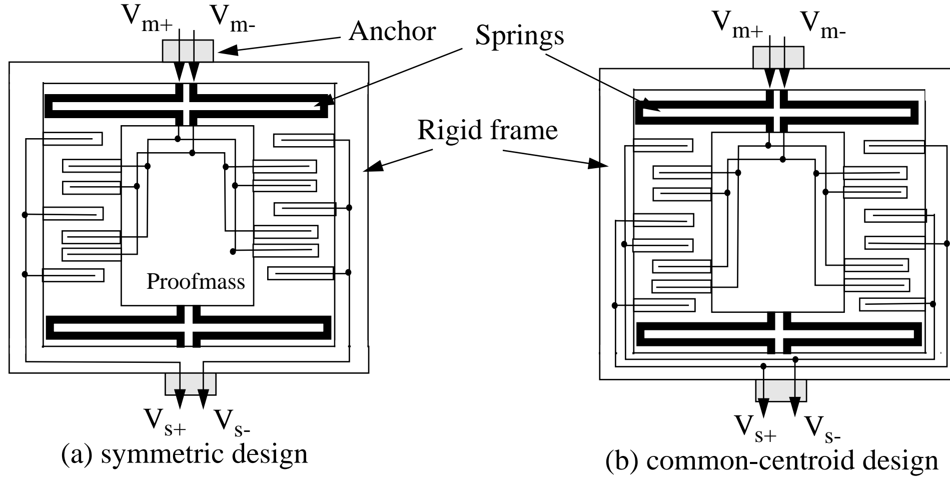


Figure 2.9: Schematics of two sensor designs

better cross-axis rejection ratio, but has greater parasitic capacitance due to longer wires and cross-overs for the sensing nodes.

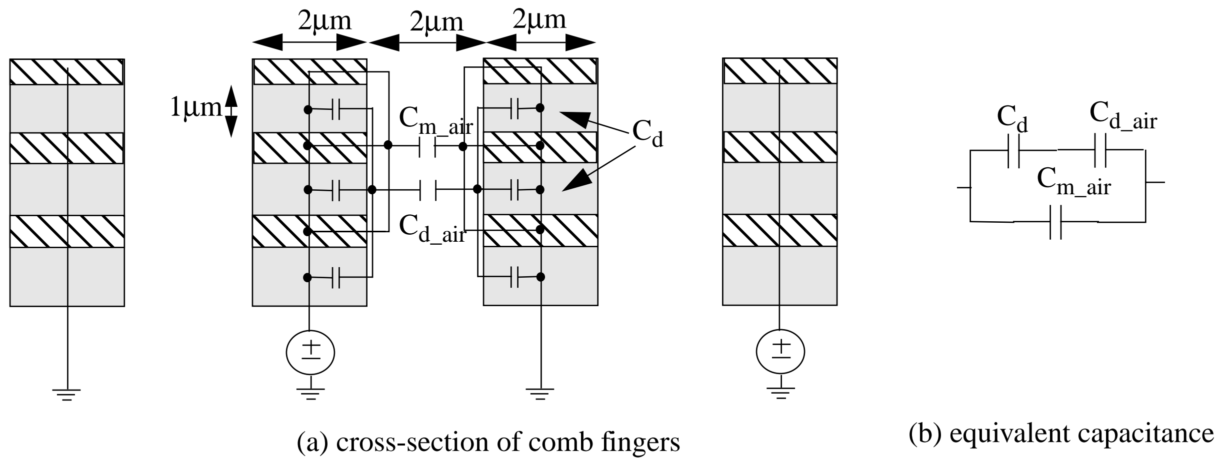
Low-impedance signals such as modulation voltages, and drive voltages are fed in from one side of the sensor through suspensions to the proofmass. High-impedance sensing signals are routed directly through the frame. This arrangement of the interconnection minimizes coupling to the critical sensing nodes.

2.4.1 Gap Capacitance of Composite Comb Fingers:

Gap capacitance of comb fingers in CMOS-MEMS technology is rather different from that in homogeneous polysilicon MEMS technology. However, since the dielectric material between metal layers has significantly larger dielectric coefficient (~4) than that of air, most of the comb voltage drops between the air gap. Therefore, to first-order, the capacitance model for CMOS-MEMS is similar to polysilicon MEMS. As shown in Figure 2.10, the total gap capacitance can be modeled as

$$C_{gap} = C_{m_air} + \frac{C_d \cdot C_{d_air}}{C_d + C_{d_air}} \approx C_{m_air} + C_{d_air} \tag{2.7}$$

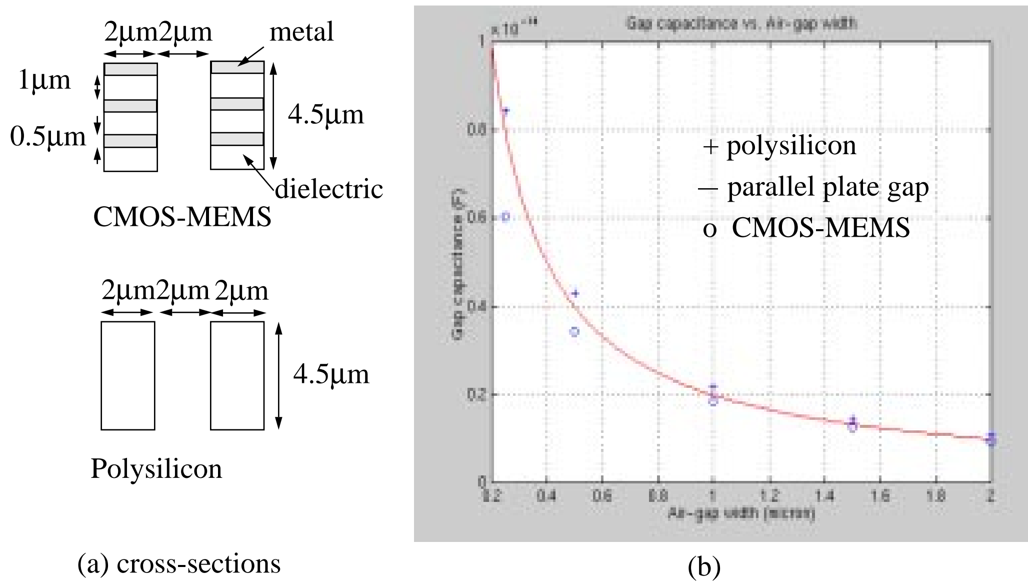
where C_{m_air} is the gap capacitance with metal sidewall, C_{d_air} is the gap capacitance with dielectric sidewall, and C_d is the dielectric capacitor. Considering the dimensions and different dielectric coefficients of the two types of capacitors, C_d is about an order of magnitude larger than C_{d_air}, so approximately the total gap capacitance is equal to the sum of C_{m_air} and C_{d_air}, which is close to the gap capacitance of homoge-



(a) cross-section of comb fingers

(b) equivalent capacitance

Figure 2.10: Gap capacitance of composite comb fingers



(a) cross-sections

(b)

Figure 2.11: Finite element analysis results of different types of gap capacitance.

neous comb fingers.

Capacitance per unit length can be more precisely determined by using electrostatic finite element analysis using Ansoft Maxwell [15]. Figure 2.11 shows the simulation results for CMOS-MEMS and polysilicon comb fingers with the same beam cross-sections, and compared with a simple parallel-plate approximation.

2.4.2 Capacitive bridge model:

For simulation purposes, an accurate capacitive bridge model is required which takes into consider-

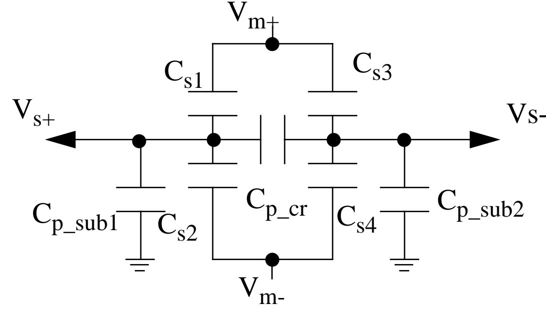


Figure 2.12: Capacitive interface model.

ation all the parasitics and couplings. Compared to previous work, the capacitive bridge is quite simple and close to ideal. Parasitics are small, and need for a ground-plane shield is eliminated. Resistance from interconnect is negligible. In Figure 2.12, the major parasitic capacitors are those between sensing signal paths and the substrate, C_{p_sub1} and C_{p_sub2}, and between two sensing paths, C_{p_cr}. The crosstalk capacitance, C_{p_cr} is increased in the common-centroid design because the two signal paths have to overlap. The effective total value of these parasitic capacitors is around 70fF, which is the same order as the total sensing capacitance. Parasitic capacitance of diodes and input transistors of buffers is relatively small, less than 5fF.

The output voltage of this model is given by:

$$V_{out} = V_{s+} - V_{s-} = V_m \left(\frac{C_{s1} - C_{s2}}{C_{s1} + C_{s2} + C_{p_sub1} + 2C_{p_cr}} - \frac{C_{s3} - C_{s4}}{C_{s3} + C_{s4} + C_{p_sub2} + 2C_{p_cr}} \right) \tag{2.8}$$

2.4.3 Sensor Sensitivity:

The sensitivity of the sensor is defined by the ratio of output voltage over input acceleration. We can divide this ratio into three terms which give more physical insight:

$$\frac{\Delta V}{A} = \frac{\Delta x}{A} \times \frac{\Delta C}{\Delta x} \times \frac{\Delta V}{\Delta C} = \frac{m}{k} \times \frac{C_s}{d} \times \frac{V_m}{C_s + C_p/2} = \frac{mV_m}{kd[1 + C_p/(2C_s)]} \tag{2.9}$$

An increase in sensitivity can be obtained by increasing effective mass, and modulation voltage, or by reducing spring constant, finger gap, and the ratio of parasitic capacitance and sensing capacitance. Since m, and d are limited by process technology, sensitivity is most effectively increased by adjusting k, and V_m. As discussed in section 2.2, spring constant k can be reduced by increasing the number of spring turns, however, a large number of turns tends to increase the cross-axis sensitivity, and reduce quality factor. V_m

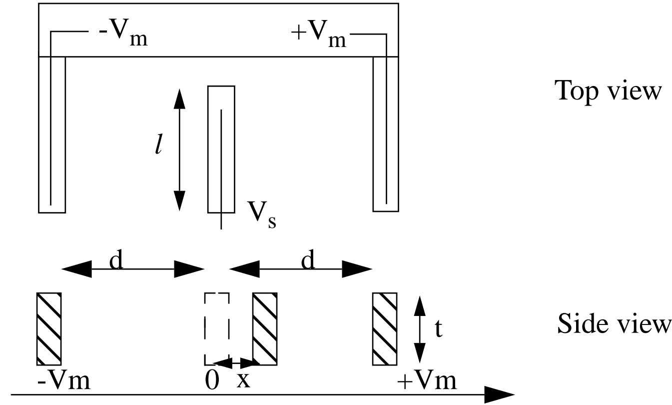


Figure 2.13: Modulation signals, V_m, generate electrostatic forces between comb fingers

is limited by electrostatic spring softening effect, which may cause instability, and is discussed in the next section.

2.5 Electrostatic Forcing

2.5.1 Electrical Spring Softening:

Modulation signals, present on the sensing capacitors, generate an electrostatic force on the proof-mass.

The force is given by:

$$F = -\frac{N\varepsilon l t V_m^2}{2(d+x)^2} + \frac{N\varepsilon l t V_m^2}{2(d-x)^2} \tag{2.10}$$

where N is the number of gaps, l is the length of fingers, t is the thickness, d is the gap, x is the displacement of rotor fingers, and V_m is the amplitude of modulation signals. The effective electrical spring constant is obtained by differentiating displacement x through the above equation:

$$k_e = \frac{\partial F}{\partial x} = -N\varepsilon l t V_m^2 \left(\frac{1}{(d+x)^3} + \frac{1}{(d-x)^3} \right) \tag{2.11}$$

As an example, given N=28, t=5µm, l=50µm, d=2µm, and a mechanical spring constant of 1N/m, Figure 2.14 shows the total effective spring constant vs. displacement x for V_m from 1V to 5V. When displacement is larger than a certain critical value, the value of the total spring constant becomes negative and the system will be unstable. For example, with V_m of 4V, a displacement of 1.0µm will create a negative spring constant and result in crashing of the fingers. At equilibrium, x=0, the effective electrical spring

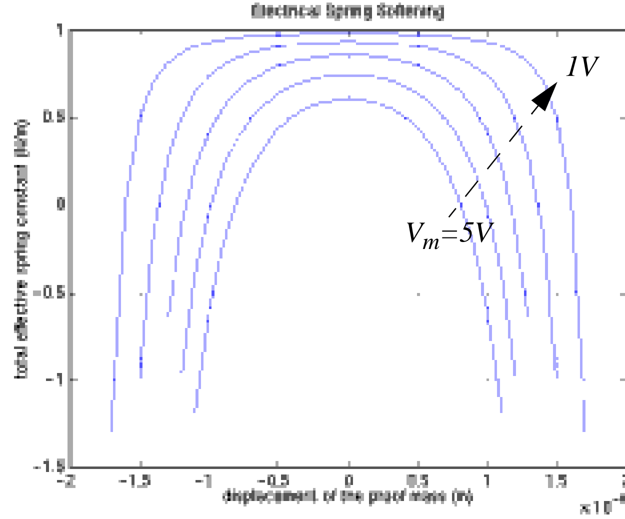


Figure 2.14: Plot of effective spring constant vs. comb-finger displacement illustrating electrical spring softening.

constant is:

$$k_e = -\frac{\partial F}{\partial x} = -2N\varepsilon l t V_m^{\;2}\left(\frac{1}{d^3}\right) \tag{2.12}$$

which is an appropriate approximation for the force balancing accelerometer since the proofmass position is nulled by the feedback. In the common-centroid design discussed in this report, with 1V modulation voltage, the effective electrical spring constant is $-1.5\text{x}10^{-2}$N/m, which is a significant fraction of the mechanical spring constant, 0.5N/m.

2.5.2 Electrostatic Force Feedback Drivers:

To implement force-balancing feedback and for design testability, four parallel comb-drive type electrostatic actuators are located at the four corners of the device. As shown in Figure 2.15, one of the rotor fingers is connected to the drive voltage signal, while all other fingers are grounded to shield the actuation signal from the sensing nodes. Since the stator fingers are close to the sensing nodes, it's desired to connect driving voltage to rotor fingers only. The electrostatic force for the comb-finger gap is given by:

$$F = \frac{CV^2}{2d} = N\frac{\varepsilon t l V^2}{2d^2} \tag{2.13}$$

where *d* is finger gap, and *C* is the capacitance of the comb-fingers. In the designs described in this report.

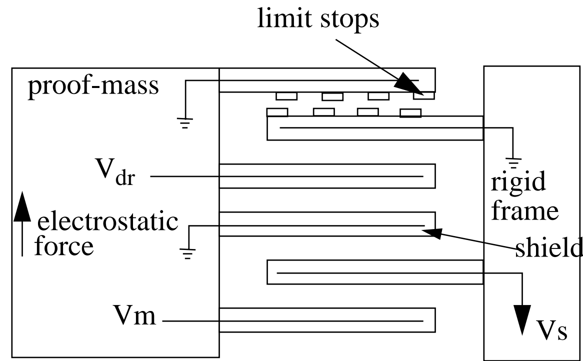


Figure 2.15: Electrostatic actuator with limit stops

The four actuators have 1.5fF gap capacitance each and can provide about ±4g driving acceleration with a driving voltage of 5V. To prevent shock effects during handling and testing, limit stops, which are grounded, are included in actuator design to prevent crashing. The distance between the tips on the limit stops is 0.9μm(3λ) less than the gaps between comb fingers, so limit stops will touch each other before other fingers. Since the minimum spacing between metal-3 lines (1.5μm/5λ) is used for finger gaps, this design actually violates the design rule. However, since the limit stops are grounded and micromachining process can prevent them from mechanically touching, this design works well in reality. The adjacent tips are shifted to each other to guarantee proper release.

3. ELECRICAL INTERFACE CIRCUITRY DESIGN

3.1 Introduction

An accelerometer infers acceleration by measuring displacement of a suspended proof-mass in response to an input acceleration. There are several methods for this transduction: piezoelectric sensing, piezoresistive sensing, electron tunneling, and capacitive sensing. The advantages of capacitive sensing include low noise, easy realization with conventional processes, and high sensitivity. For the polysilicon-based surface MEMS processes, a drawback of capacitive sensing is that the output can be seriously attenuated by the parasitic capacitance at the output node. But as stated in Chapter 1, for the CMOS-MEMS process, the parasitic capacitance is relatively small. In this chapter, a fully differential interface to the accelerometer is presented.

The system block diagram is shown in Figure 3.1. There are two ways to sense the capacitance change, one is through sensing charge and the other one is through sensing voltage. Voltage can be sensed by buffering the output nodes[8]; while charge can be sensed by connecting the output nodes to a charge integrator [6]. Voltage buffering is used here instead of charge integration. Buffers isolate the sensitive nodes from following electronics, especially dynamic switched-capacitor circuits, eliminating effects from switch noise, and reflect noise injections [6] to the sensing node. Since the parasitic capacitance is very small, there is no need for buffer driven shielding to increase sensitivity. Diodes can provide good dc bias at the high-impedance inputs of the buffers without considerable noise contribution. Buffers are followed by preamplifiers to boost signal levels. Large load capacitors associated with buffers and preamplifiers significantly reduce kT/C noise and switch noise. The amplified signal is then led into a switched-capacitor demodulator. Switched-capacitor circuits have advantages of good dynamic range, accuracy, parameter insensitivity and easy implementation in CMOS technology.

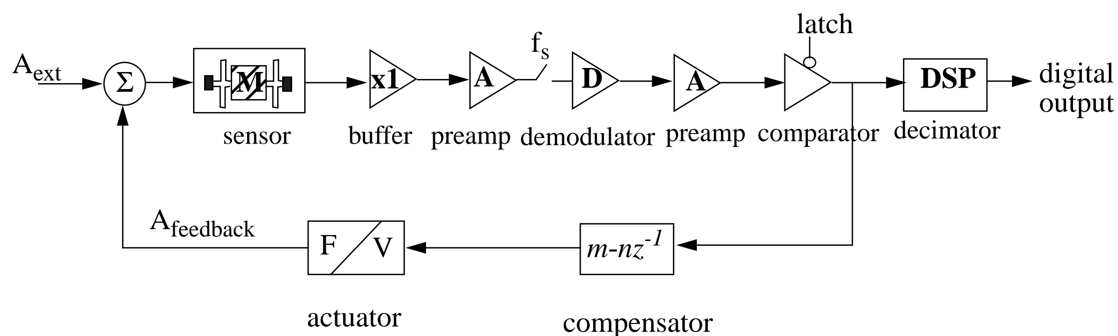
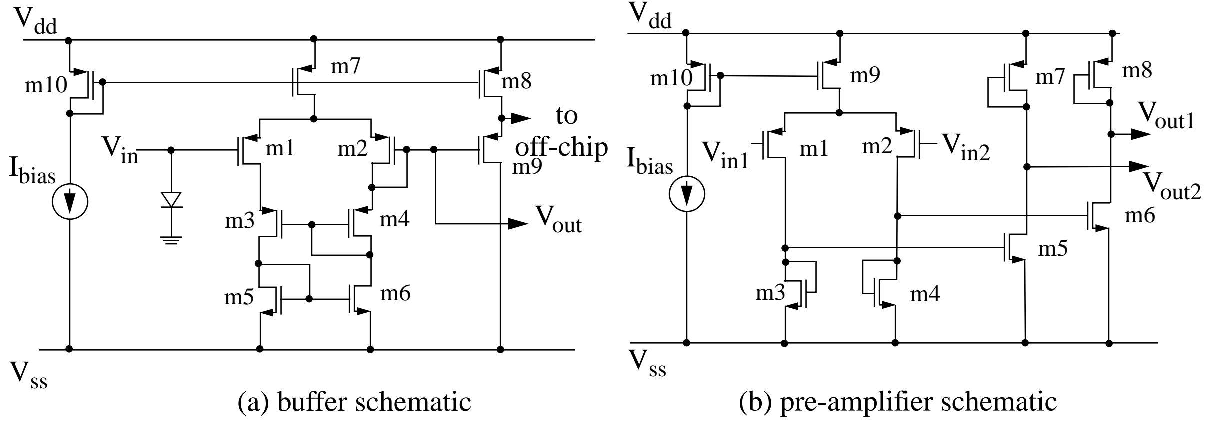


Figure 3.1: System block diagram of accelerometer



(a) buffer schematic (b) pre-amplifier schematic

Figure 3.2: Schematics of the front-end circuits

3.2 Front-end Circuits

The front-end electronics are composed of ac coupled buffers and preamplifiers. Typical mismatch of MOS devices can be very large, up to 10mV input offset. If stages are dc coupled, there will be significant offset accumulation and propagation, which will drastically reduce the dynamic range. To solve this problem, outputs of preceding stages are connected to the inputs of following stages through a large ac-coupling capacitor, and the inputs of following stages are dc biased by diodes. The coupling capacitors are chosen to be reasonably large (2pF) to minimize signal attenuation by the capacitive divider formed between the coupling capacitors and the input parasitic capacitors.

The schematic of the buffer is shown in Figure 3.2 [8]. Optimal buffer design requires a trade-off between minimization of input capacitance and minimization of thermal noise. Increasing transconductance of the input transistors will reduce thermal noise, but the transistor size must increase assuming constant $V_{gs\text{-}eff}$, which equals to (V_{gs}-V_t), and therefore increase the input capacitance. PMOS input transistor pairs are used to minimize body effect due to the n-well CMOS process. Cascoded transistors decouple the drains of input pairs from output nodes, and keep drain nodes tracking the input, thus minimize effective input capacitance. A $V_{gs\text{-}eff}$ of 0.25V, and a bias current I_{dc} of 100µA are used in design. Hspice simulation shows a -3dB bandwidth of 98MHz with 1pF load, and an effective input capacitance of 2.5fF.

Diodes are used to provide dc bias at input nodes. In the n-well CMOS process, the diode is implemented as shown in Figure 3.3. There are two types of connections used depending on which node is attached to the high-impedance node. As shown in Figure 3.3, the P-type connection has much less capac-

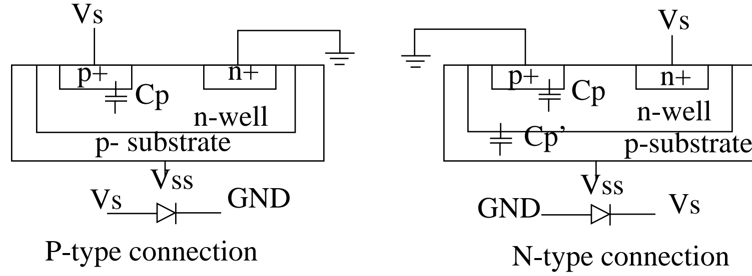


Figure 3.3: Two types of connections for diode in n-well process

itance than the N-type connections, since the latter has a much larger associated substrate junction capacitance. Therefore, high-impedance nodes are connected to the P-type side of the diodes in out circuits. There are other implementations of diodes, such as diode-connected MOS devices, however, they have larger gate capacitance and smaller leakage current.

The main trade-offs in preamplifier design are to achieve reasonable gain boost, minimize thermal noise, and limit bandwidth, while keeping reasonable settling time. Since the output signals of the preamplifiers are sampled for demodulation at the following stage, the preamplifier should also act as an anti-aliasing filter to minimize high-frequency noise aliasing to the signal band. Simple differential pairs with diode-connected load transistors have enough speed to achieve the settling requirement. A gain of about 10 is obtained for each gain stage. Since the signal dynamic range is relatively small, there is no need to use triode-connected loads to have less distortion. Since the pre-amplifier is working open-loop, and the dominant pole is determined by the large sampling capacitor on the output node, settling time can be estimated simply through the RC delay time at the output node. For a sampling frequency of 1MHz, a settling time of less than 100nS is required. Using 7τ as the settling time (settle to within 0.1%), the preamplifier must have a -3dB bandwidth of 12MHz, which requires an output impedance of 7kΩ for a sampling capacitor of 2pF. Hspice simulation shows a -3dB bandwidth of 16.5MHz with a 2pF load capacitor. Another requirement for the preamplifier is that the input capacitor be relatively small and stable, since it forms a capacitor divider with the ac coupling capacitors, and directly affects the gain. In the design, the effective input capacitance of the preamplifiers is about 200fF.

3.3 Demodulator Design

The demodulator schematic is shown in Figure 3.4, together with the clock waveforms. After preamplification, the signals are subsequently sampled for demodulation. At the capacitive bridge interface, the sensing signals are modulated to high frequency. Through demodulation, sensing signals are moved back to low frequency and low frequency noise, offsets and switch charge errors injected at the front-end circuits and demodulator stage are cancelled out.

Operation of the demodulator is shown in Figure 3.5. Since the acceleration signal bandwidth is much smaller than the modulation frequency, we can assume that the sensing signals have constant amplitudes within one modulation period and only change sign between first and latter half period, which is almost true given that the bandwidth of the acceleration signal usually is no greater than 1kHz. Offsets and low frequency noise associated with the position sensing interface, are referred to an error voltage, V_{error}, at the inputs of the demodulator. V_{error} remains constant between two adjacent samples, assuming sufficiently high modulation frequency, *i.e.* 1MHz for this design. A correlated double-sampling technique [10] is used to subtract out V_{error} with two sequential samplings.

For one modulation period, there are four phases, namely, Sample 1, Integrate 1, Sample 2, and Integrate 2. During the Sample 1 phase, V_{s+} and V_{error} are sampled to sampling capacitor C_{i1}, and V_{s-} is sampled to C_{i2}. At the same time, integration capacitors C_{f1} and C_{f2} are reset to zero charge, and hold capacitors C_h's are floating. During the Integrate 1 phase, the difference of charges on C_{i1} and C_{i2} are integrated to C_{f1} and C_{f2}, and the outputs are preamplified, sampled and held on hold capacitors. During the Sample 2 phase, $-V_{s+}$, V_{error} and $-V_{s-}$ are sampled. Since in the second half of the demodulation period, the hold capacitors are floating, charges obtained during the Integrate 1 phase are held. In the final Integrate 2 phase, $-V_{s+}$, V_{error}, $-V_{s-}$ are integrated and amplified. Since the error voltage remains constant, and sensing signals flip their signs, the subtraction cancels out the error voltage and amplifies the sensing signals, as shown in Figure 3.5 (d).

Referring to the waveforms in Figure 3.4, the switches $k_1$and k_2 use the ϕ_{1e} phase which turns off earlier than ϕ_1, and k_3 uses the ϕ_{1ed} phase which turns off slightly later than ϕ_{1e} but still ahead of ϕ_1. The purpose of doing this is to reduce switch charge injection errors and clock feedthrough. By turning off switches k_1 and k_2 slightly earlier, charge injection of other switches, k_4, k_5, k_6, k_7, and k_8 will not add to

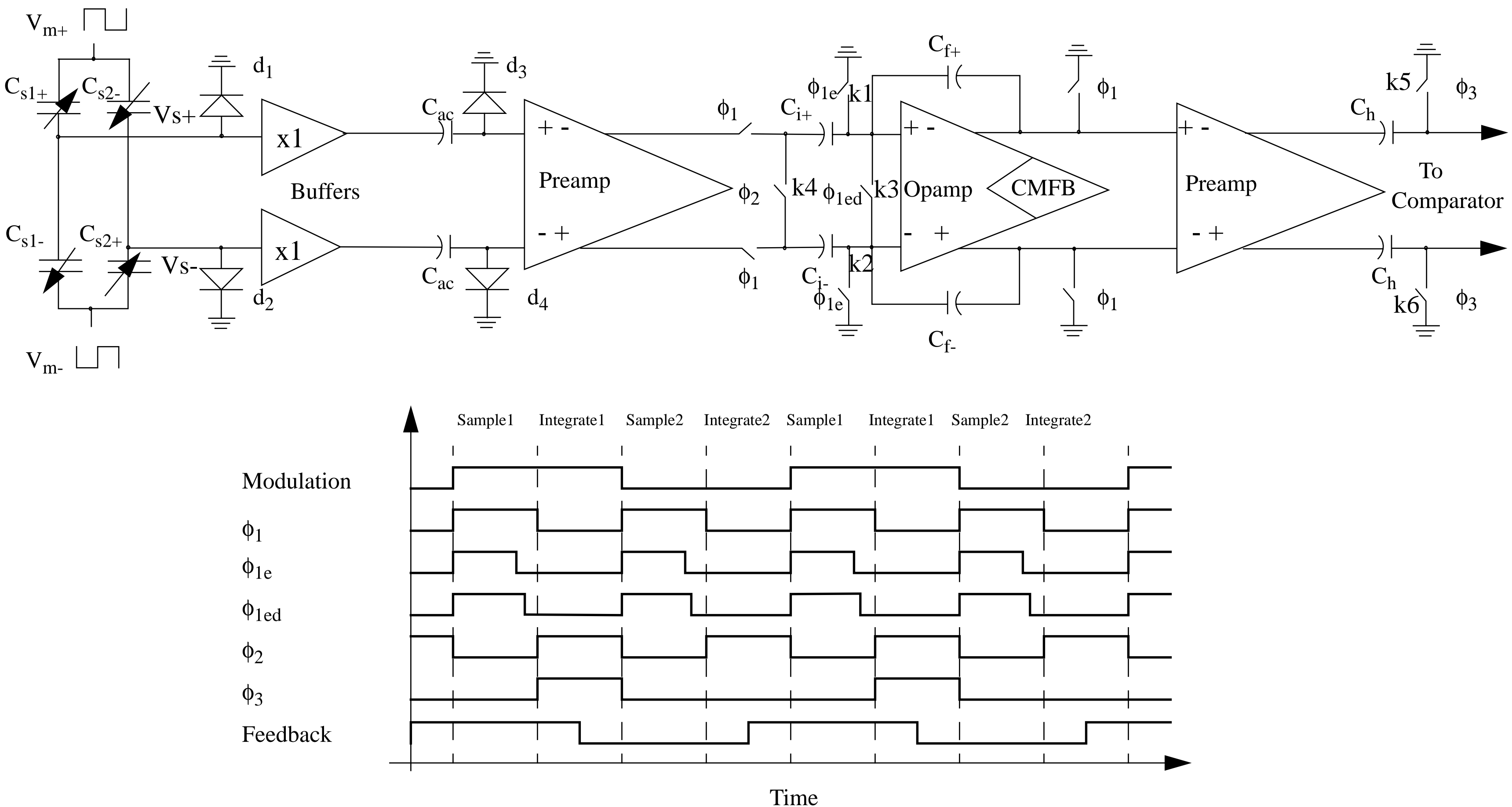
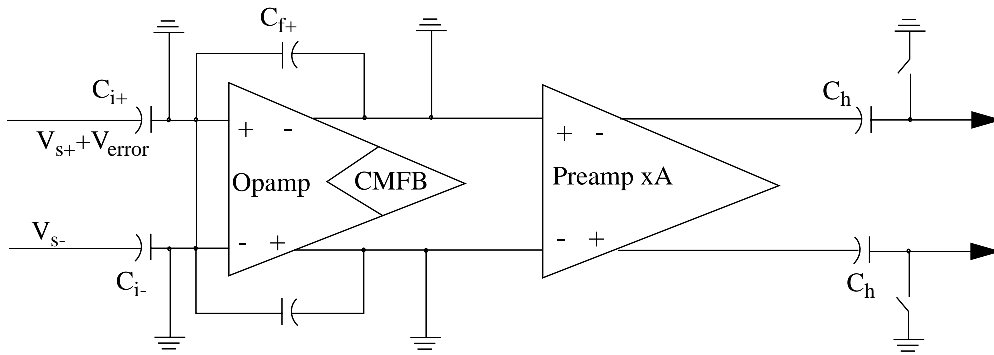
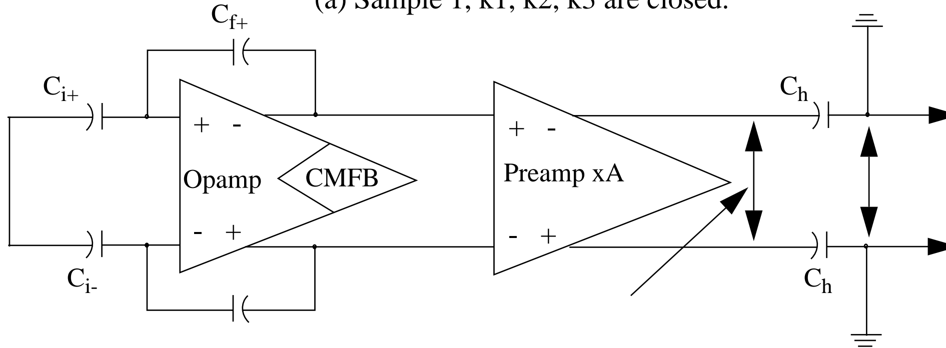


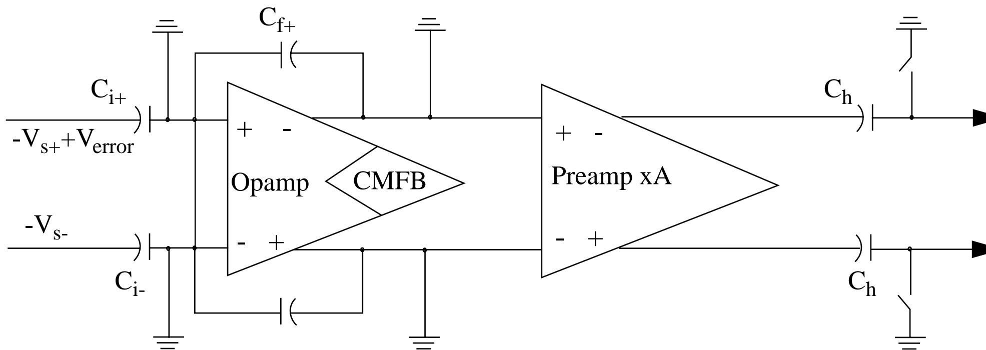
Figure 3.4: Schematic of the position sensing interface and clock waveforms.



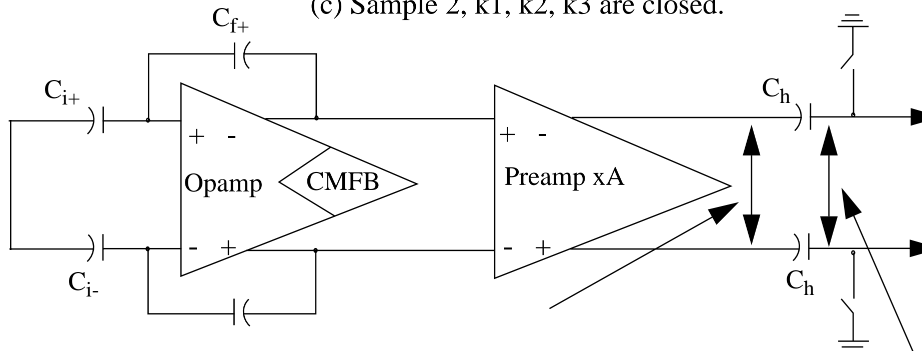
(a) Sample 1, k1, k2, k3 are closed.



(b) Integrate 1, k4, k5, k6 are closed.



(c) Sample 2, k1, k2, k3 are closed.



$$V_{out} = (V_{s-} - V_{s+}) \times \frac{2C_i}{C_f} A$$

(d) Integrate 2, k4 is closed.

Figure 3.5: Operation of the demodulator.

sampling and integrating capacitors since there is no charge loop. Only switch charges from k_1 and k_2 are still injected onto the input capacitors. If the switches are ideally matched, then charge injection is rejected as a common-mode signal. In practice, they have mismatches which will cause some offset. With clock phase ϕ_{1ed}, k_3 shorts k_1 and k_2 and equalizes the charge injected.

Maintaining good CMRR at the inputs of demodulation is crucial to obtaining good dynamic range. Due to process variations, the outputs of the front-end preamplifiers have a difference in output bias voltage. If switches are used between ground and the sampling nodes to perform integration, the bias voltage level can appear as a huge common-mode signal at inputs of demodulator, which adds design difficulties and reduces dynamic range. In this design, integration is performed by shorting the two differential sampling nodes through switch k_4, so that only the difference of charges corresponding to two input signals is integrated. In this way, common-mode input signals are greatly attenuated.

Integrating capacitors are reset by grounding inputs and outputs of the opamp, and there is no time that the feedback loops are disconnected. By doing this, output glitches due to disconnection of feedback loops during switch transitions are avoided at the cost of increasing power dissipation.

The schematic of the operational amplifier used in the demodulator is shown in Figure 3.6. The amplifier is a fully differential wide-swing folded-cascode design with dynamic common-mode feedback at the outputs. The folded-cascode amplifier has good stability and reasonable gain with a single gain stage. Hspice simulation shows a dc gain of 2800, with a open-loop -3dB bandwidth of 60kHz for a 2pF load capacitor. A wide-swing biasing circuit is required for the relatively small 3.3V rail-to-rail power supply. Switched-capacitor common-mode feedback circuitry, allowing wide output swing, is suitable for this design.

The pre-amplifier following the demodulator further boosts the signal level. At the last stage, a latched comparator digitizes the analog signal to a digital bit stream. Buffers are used to prevent *kickback* effects, which refers to the possible interference from the latch stage back to the driving stage. Positive feedback is used in the comparator to increase gain and ensure a digital output.

3.4 Noise Analysis

In the accelerometer system, there are several noise sources. In the mechanical domain, the sensor presents Brownian noise to the system; in the electrical domain, there are thermal noise, flicker noise gen-

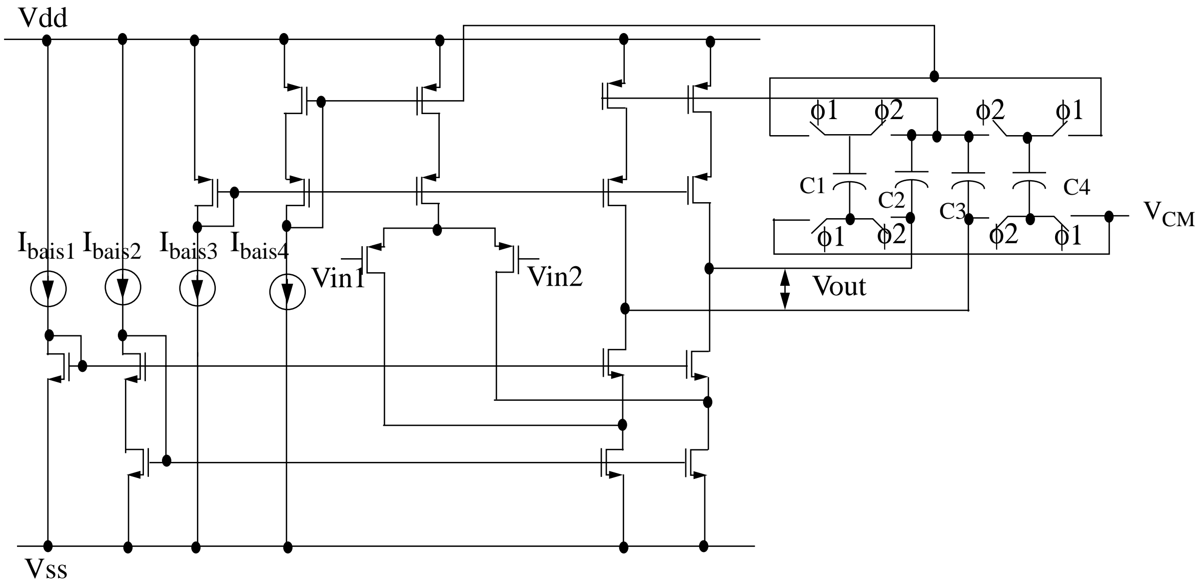


Figure 3.6: Schematic of the folded-cascode amplifier for the demodulator.

erated at various locations in addition to quantization noise if digital feedback is used. Quantification of all of the major noise sources is critical for minimizing the overall system noise floor.

When calculating noise, it is helpful to convert all noise sources to input-referred acceleration noise, and assume the system is noiseless. This approach will be carried on through this section.

3.4.1 Brownian Noise

Brownian noise is caused by random collision of air molecules with the sensor. For a damped suspended proofmass, the Brownian noise acceleration is [13]:

$$\sqrt{\frac{a^2}{\Delta f}} = \frac{\sqrt{4k_bTb}}{m} = \sqrt{\frac{4k_bT\omega_r}{mQ}} \qquad 3.\ 1$$

where k_b is Boltzman's constant(1.38×10^{-23}J/K). For example, if m=0.5μg, Q=5, ω_r=10kHz, the Brownian noise is 66μg/sqrt(Hz).

From the above equation, Brownian noise can be reduced by either increasing effective mass or reducing air damping, or equivalently increasing quality factor. The proofmass is limited by realizable film area which is mostly determined by acceptable radius of curvature and cost. Proper curl matching technique can be used to achieve a relative large film area even though the radius of curvature can be small. An alternative is to connect multiple sensing elements in parallel to get a larger effective mass. Reducing damping can be achieved by vacuum packaging.

3.4.2 Front-end Noise

For a system with several gain stages, the noise injected in the earliest stage will be the dominant noise contributor to the system. For this system, the front-end circuits are the dominant noise sources, while the noise contributed by subsequent stages are divided by the gain of front end stage, and are negligible. There are several different type of noise involved: thermal noise of MOS devices, flicker noise of MOS devices, and shot noise of biasing diodes. It should be noted, since the compact integration of MEMS devices with electronics provided by the CMOS-MEMS process, thermal noise of interconnect, which is usually a major noise source in polysilicon-based processes, is negligible for this design.

3.4.2.1 Thermal Noise of the MOS Devices

MOS devices generate thermal noise as normal resistors due to the effective channel resistance. It is given as:

$$\frac{V_n^2}{\Delta f} = \frac{8}{3}\frac{1}{g_m}kT \qquad 3.2$$

Since buffers only have unity gain, the thermal noise of the first preamplifier will directly contribute to the equivalent input noise. An alternative design will employ a buffer with some gain to reduce the noise contribution of the preamplifier stage. However an amplifier input needs to take increased input capacitance into consideration, since a typically sized input transistor (20μm/0.6μm) has an input capacitance of around 20fF which will result in a 3dB signal attenuation for the symmetric design discussed in this report. PMOS input transistor pairs have more thermal noise than their NMOS counterparts due to their lower transconductance for an equal gate area. The noise contributed by the input pairs dominates, since other MOS transistors in the buffer have smaller transconductance and their input referred noise contributions are proportional to the ratio of their transconductance over that of the input transistors.

When the outputs of the preamplifier are sampled for demodulation, wide-band thermal noise is also sampled and aliased to the signal band. Sampled noise can be calculated by integrating thermal noise power density over the preamplifier’s bandwidth as:

$$V_{n(rms)}^2 = \frac{V_n^2}{\Delta f} \times \frac{\pi}{2} f_{-3dB} = \frac{V_n^2}{\Delta f} \times \frac{1}{4R_{out}C_i} \qquad 3.3$$

where R_{out} is the output resistance of the preamplifier. The above equation demands that bandwidth should be made as narrow as possible. The lower bound of bandwidth is limited by the settling time requirement as stated in section 3.2. High-frequency thermal noise will be partially removed by digital low-pass filtering at the decimation stage.

Hspice simulation shows a wide-band noise floor of 5nV/sqrt(Hz) at the input nodes, taking the noises in the buffers and preamplifiers into account.

3.4.2.2 Diode Noises

Biasing diodes introduce both shot noise and flicker noise. As described in previous section, flicker noise is removed by modulation and demodulation. Diode shot noise is modeled as a wide-band noise current source and given by:

$$i_d^2 = 2qI_d\Delta f \qquad 3.4$$

where I_d is the current flowing through the diode. The dc leakage current of the diode is almost zero in this design, since diodes are covered by top metal layer, and there is no photo-generated leakage current. The equivalent noise voltage is [8]:

$$\frac{v_d^2}{\Delta f} = 2q\frac{C_j}{2\pi f(C_j + C_i + C_s)^2}v_{in} \qquad 3.5$$

which is proportional to *1/f* and the sensing signal magnitude. Assuming C_j is about 10 times less than the total capacitance and V_{in} is around 1mV, the noise power density due to diodes is about 4 orders of magnitude less than that contributed by MOS devices. From above analysis, we can see that biasing diode is not a major noise source in this design.

3.4.2.3 Electronic Noise vs. Mechanical Noise

Assuming the front-end electronics dominate the electronic noise, noise contribution of electronics can be compared with the mechanical Brownian noise of the sensor by referring all noise sources to an equivalent input acceleration noise. For a sensor with sensitivity of 2mV/g, and assuming 5nV/sqrt(Hz) input noise floor, a -3dB bandwidth of 20MHz at the outputs of the preamplifier where noise aliasing occurs, sampling frequency of 1MHz and a signal bandwidth of 1kHz, the equivalent input referred accel-

eration noise is 20µg/sqrt(Hz), which is smaller than the Brownian noise floor (50µg/sqrt(Hz)) in this design.

3.4.3 Quantization Noise

Quantization noise refers to the errors caused by digitizing analog signals to discrete digital signals. The noise power density is:

$$\frac{V_Q^2}{\Delta f} = \frac{\Delta^2}{12} \qquad 3.6$$

where Δ is the value of the least significant bit. In this design, quantization noise injected at the regenerative comparator can be attenuated by the second-order noise shaping of the loop. The sensing element acts as a second-order noise shaping element in the system. In a second-order sigma-delta system, quantization noise is attenuated by about 15dB/Octave. For a given oversampling ratio, assuming a 1kHz signal band width, 1MHz sampling frequency, and a gain of 1000 from the front-end to the input of the comparator, the quatization noise is attenuated by roughly -150dB, to 0.05nV/sqrt(Hz) input referred noise, and can be neglected.

4. SYSTEM SIMULATIONS

4.1 Introduction

System-level simulation combining mechanical and electrical elements is extremely important for MEMS design. More specifically, design of the accelerometer control system, especially an underdamped mechanical system with highly non-linear closed-loop dynamics, requires accurate simulation of both the MEMS devices and the interfacing analog/digital electronics. In this chapter, the simulation is done with Hspice.

4.2 Hspice Simulation

Hspice [14] is a standard electrical domain simulation tool with certain behavioral simulation capacities. Electronic circuitry can be simulated very accurately within Hspice. Mechanical elements need to be precharacterized with finite-element analysis tools such as Abaqus to get essential parameters like resonant frequency, quality factor, effective mass and spring constant. With a known Laplace transfer function, a system model of the sensor can be implemented with behavioral models within Hspice. The Hspice block diagram of the accelerometer system is shown in Figure 4.1. The capacitive interface is realized with voltage controlled capacitor model provided by Hspice. All signals including force, acceleration, and displacements are referred to voltage signals. The pulse stream from the comparator output is low-pass filtered by a 0.5dB-ripple 5th-order Chebyshev low-pass filter, and then a Fast Fourier Transform (FFT) is performed to see the spectrum of the output. This approach can accurately simulate electronics and can be relatively fast.

Figure 4.2 shows the simulation results of the step response of an accelerometer. The sensor has a

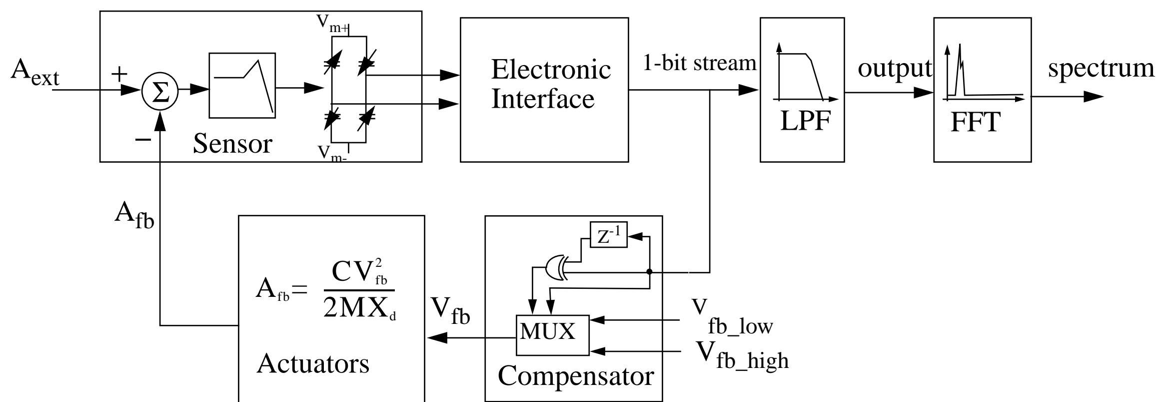


Figure 4.1: Hspice model of an accelerometer system

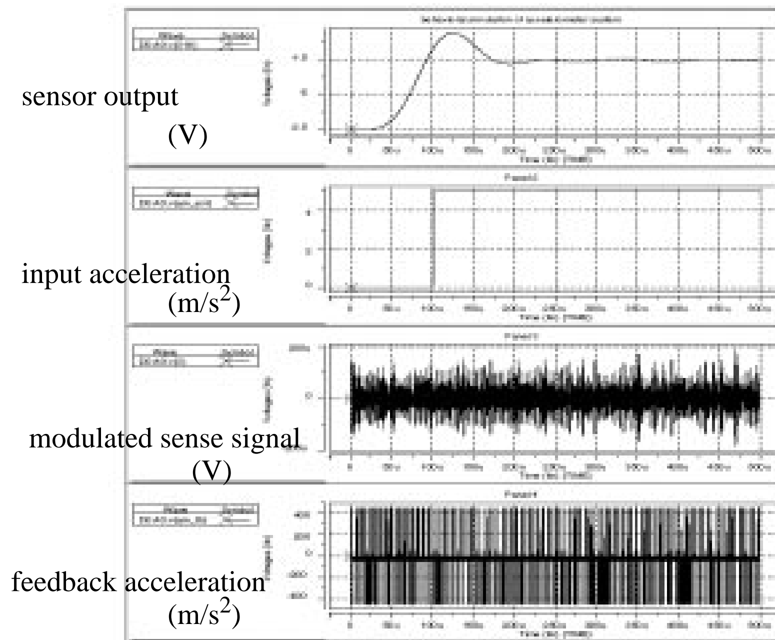


Figure 4.2: Step response of the accelerometer

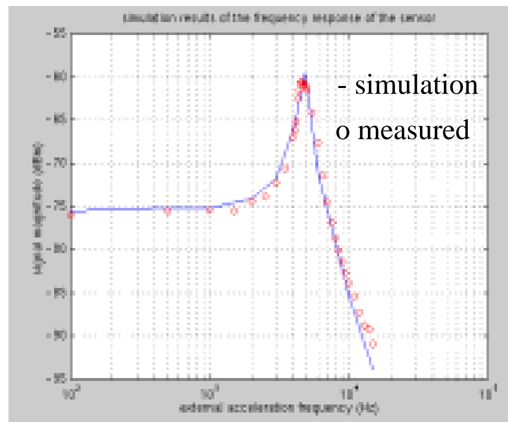


Figure 4.3: Simulation results of the frequency responds compared with experimental results.

proofmass of 0.5µg, resonant frequency 8kHz, and Q of 3. V_{fb_low} is 3V and V_{fb_high} is 15V. It's found that for Q of 3, compensation is necessary for stable operation. Compensation is done by using '$m\text{-}(m\text{-}1)Z^{-1}$', and larger *m* means deeper compensation. For Q=10, simulation shows that a *m* of 4 is needed.

Since only open-loop testing has been done, open-loop simulations were performed to compare with the experimental results. Figure 4.3 shows the simulated frequency response of the sensor compared with measured results. The original simulation data were attenuated to take the impedance matching issues in experiments into account.

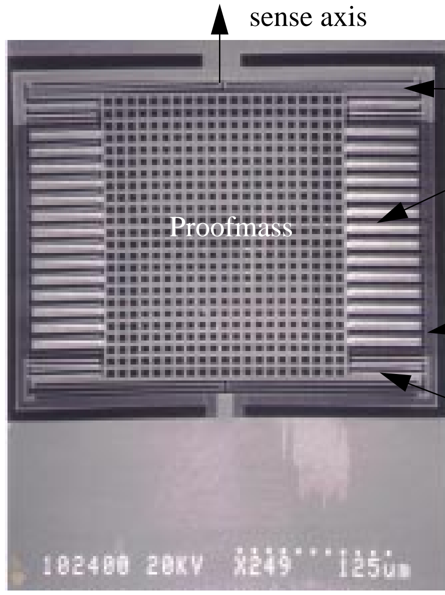


Figure 5.1: SEM of the first-generation symmetric lateral accelerometer.

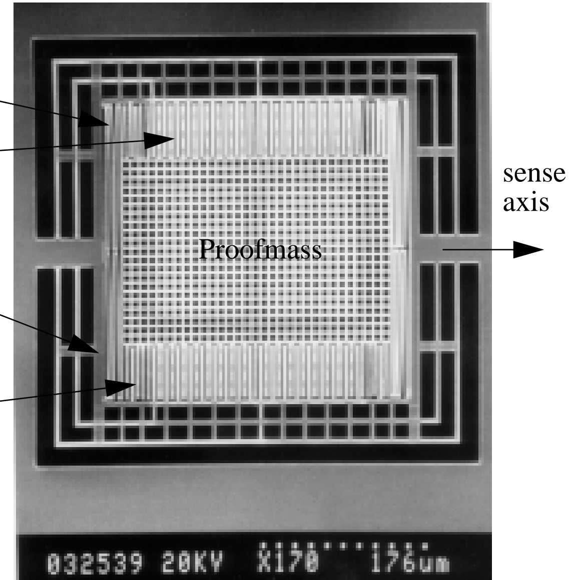


Figure 5.2: SEM of the second-generation common-centroid lateral accelerometer.

5. EXPERIMENTAL RESULTS

5.1 Introduction

Preliminary experiments have been done with two different designs of the lateral accelerometer. Accelerometer characteristics, such as sensor sensitivities, frequency response, and parasitic capacitance, were measured. Initial calibration of the sensor was also performed by rotating the device at different angles to the earth's gravitational field.

Two versions of lateral accelerometers have been designed and fabricated. Figure 5.1 shows the SEM of the first-generation device which is referred as the symmetric lateral accelerometer. Open-ended springs with one turn are used in this design. Vias on the fingers result in large lateral curl and offset. The second-generation device, shown in Figure 5.2, uses a common-centroid design and springs with two turns. Comb fingers are designed to be wider to reduce lateral bending. Vias are removed from the fingers. Figure 5.3 shows the layout of the accelerometer system. Electronics are covered by the planerized top-metal layer, and can not be seen in the SEM's.

5.2 Experimental Results

Experiments have been done mainly through self-tests by using the on-chip electrostatic force actua-

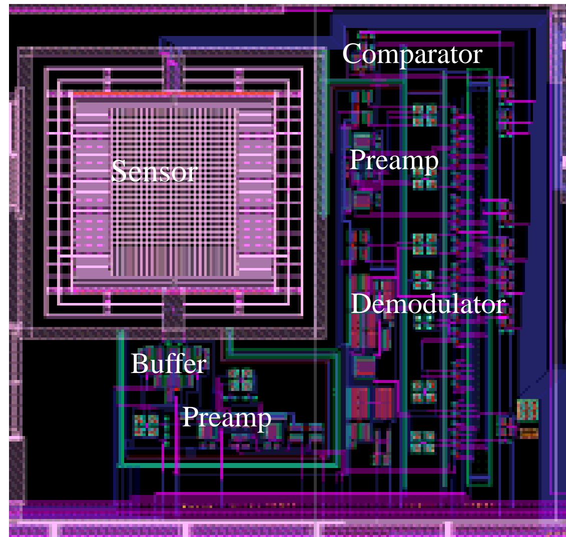


Figure 5.3: Layout of the second-generation accelerometer system

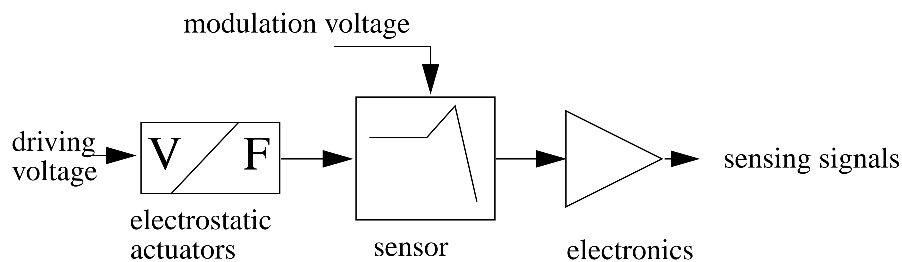


Figure 5.3: Schematic of self-test setup

tors as shown in Figure 5.3. Calibration by changing sensor's orientation to the earth gravity is performed and the results are used to convert driving voltages to corresponding forces.

Modulation voltages and clocks are generated externally with discrete IC's in a way similar to [8].

The experiments of the first-generation accelerometer were performed on a probe station. Table 1 lists major parameters of the device. Only the ratio of parasitic capacitance and sensing capacitance can be measured, and the estimated value is calculated assuming a total sensing capacitance of 60fF. Parasitic capacitance and mismatch of sensing capacitance is measured in a way as shown in Figure 5.4. The capacitance ratios are derived from the ratios of driving signals and buffer output signals. By driving one end of the capacitor divider and grounding the other end, mismatch between two sensing capacitors can be measured. Buffer gain is assumed to be one, since the frequency of the signal is much lower than the -3dB frequency of the buffer.

Table 1: Major parameters of the accelerometer

Device parameter	Symmetric design	Common-centroid design
Dimension	350µm * 250µm	400µm * 300 µm
Proof-mass	0.36µg	0.45µg
Spring constant	1.0N/m	0.5N/m
Resonant frequency	8.5kHz	5.0kHz
Quality factor	8	7
Total sense capacitance (design)	4* 15fF	4*20fF
Total sense capacitance (test)	4*15fF	4*6.5fF
Parasitic capacitance	2*37fF	2*60fF
Capacitor mismatch	19%	15%
Sensor offset	70g	40g
Sensor sensitivity (V_m=1V)	1.5mV/g	1.2mV/g
Sensitivity at preamp outputs	N/A	80mV/g

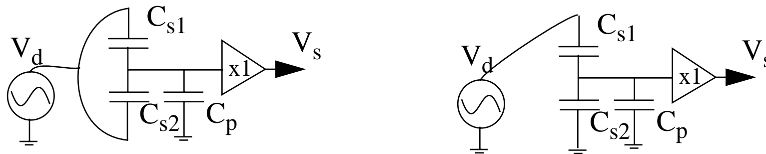


Figure 5.4: Setup for testing of parasitic capacitance

The common-centroid accelerometer is bonded and packaged in a ceramic DIP package. Major parameters are also listed in Table 1. The table shows that this design, surprisingly, has lower sensitivity than the symmetric design. The reason is that the residual stress gradients cause the two-turn springs to bend down, making the proofmass lower than the rigid frame, and significantly reduces the effective sensing capacitance. Figure 5.5 shows a close-up view of the fingers. The rotor fingers are notably lower than

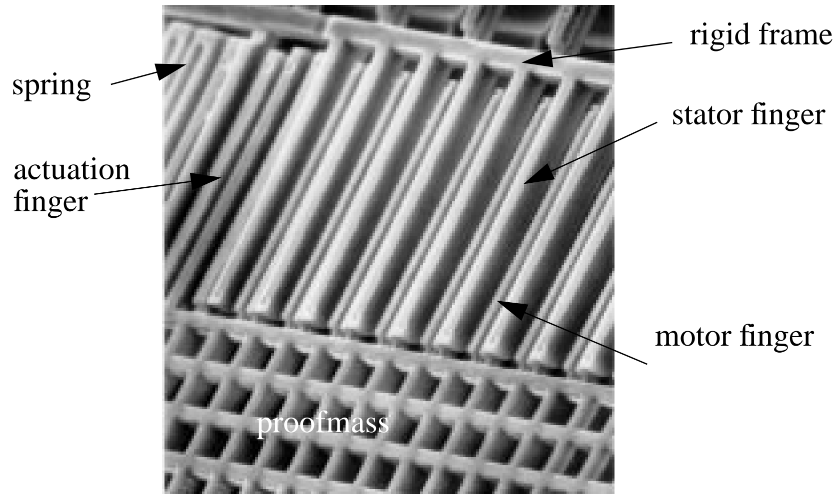


Figure 5.5: Motor fingers are noticeablly lower than stator fingers.

the stator fingers. The offset of this design is improved slightly over the symmetric design. Figure 5.2 shows that the comb fingers have much less lateral bending than those in Figure 5.1. However, the two-turn springs have large lateral curling which is one of the major sources of offset. The sensor outputs have an offset of about 25mV, which saturates the preamplifier. In experiments, the offset is cancelled by applying a DC voltage of about 24V to two electrostatic actuators on one side of the sensor. Self-test is then performed by applying driving voltages to the other two actuators.

Figure 5.6 shows the preamplifier output signals vs. the orientation angles of the device in the earth's gravitation field. The orientation angles were measured with a protractor, resulting in significant testing errors. Refined calibration needs to be done after getting a precision dividing head. Cross-axis calibrations are also performed, but output signals are too small to be measured.

Dynamic testing is done by applying a sinusoidal driving signal to the electrostatic actuators. The output of the preamplifier is connected to a spectrum analyzer. By varying the frequency of driving signal, and measuring the peak amplitude of the modulated signal, the frequency response is obtained as shown in Figure 5.7. The quality factor is about 8. The spectrum of the modulated signal at 100Hz is shown in Figure 5.8. The magnitude of the driving acceleration is approximately equivalent to 4g.

The magnitude of the peak for driving force shown in Figure 5.8 are much smaller than the real values, since the output impedance of the preamplifier doesn't match the spectrum analyzer's 50Ω input impedance. It has been observed that a 100mV peak-to-peak voltage at the output of the same preamplifier appears as a corresponding pulse of -74dBm on the spectrum analyzer. The pulse appearing at the center

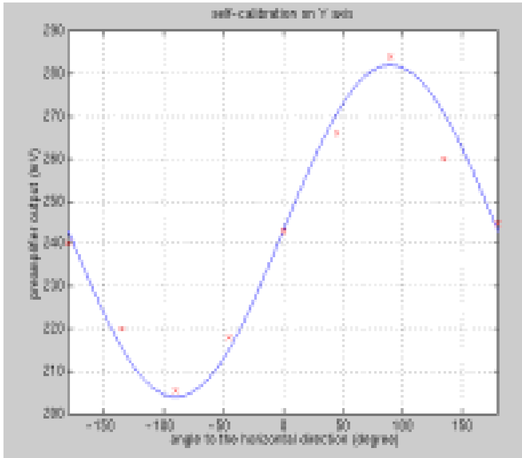


Figure 5.6: Sensor preamplifier output vs. orientation with respect to gravity.

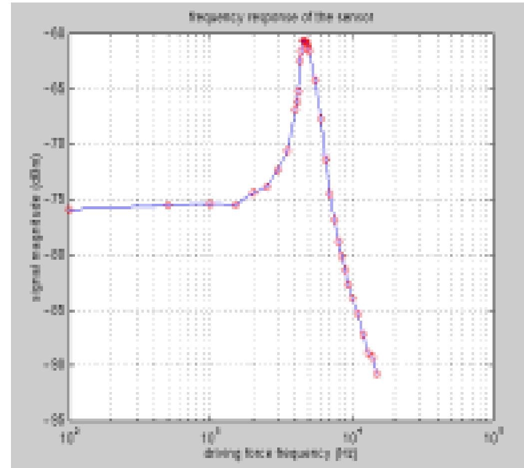


Figure 5.7: Frequency response of the sensor due to self-test exitation of ~4g amplitude.

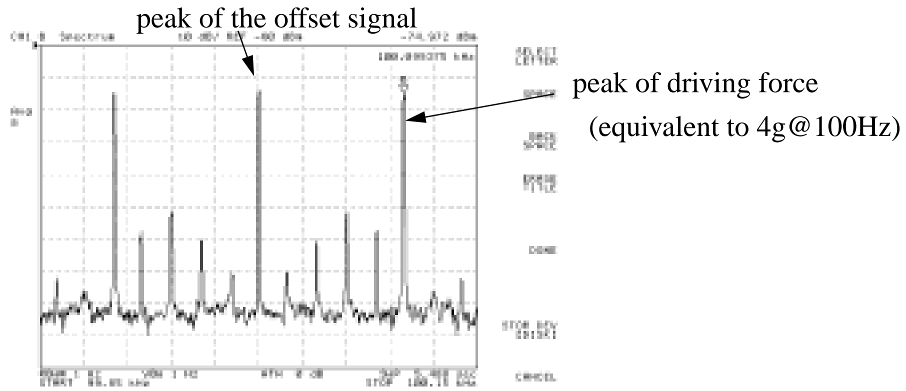


Figure 5.8: Spectrum of amplitude-modulated signal.

modulation frequency (100kHz) is the offset signal which is not completely cancelled out.

Other parts of the accelerometer are currently under-testing.

6. CONCLUSIONS

Fully differential CMOS-MEMS accelerometers are designed, and fabricated. Vertical stress gradient in the composite structural layers are compensated to first order with a curl matching technique. Issues in sensor design, such as composite gap capacitance, common-centroid layout, proper routing of interconnections and design of electrostatic actuators are discussed. Low frequency noise, offset, and switch charge errors injected in the electronic interface can be rejected with the fully differential position sensing interface. Simulation and analysis shows that for this design, the Brownian noise dominates the overall noise floor. Behavioral models of the mechanical sensor allow simulation of the entire electro-mechanical system.

Initial testing results show good performance in terms of sensor sensitivity. Functional sensor and front-end circuits are demonstrated, showing a promising future for CMOS-MEMS technology in applications of inertial sensors.

Further closed-loop testing of the device is needed. The initial experimental results show large offset at the sensor outputs, which requires improved sensor design to the overcome the lateral bending problem associated with composite microstructures and underscores the need for the offset trimming circuitry. For this design, offset trimming can be done at the sampling nodes of the demodulator. The gain of the preamplifiers should be reduced to avoid saturation at the front-end.

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