Topology Trade-offs in the Synthesis of Chip-based Electrophoretic Separation Systems

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ABSTRACT

Complex topologies result from the desire to create compact micro scale electrophoretic devices. Knowledge of how topology affects chip performance is necessary to develop feasible and efficient designs. In this paper, we investigate how topology affects system performance when the available chip area is constrained.

Keywords: Electrophoresis, Design, Microfluidics

1 Introduction

The ability to fabricate increasingly complex micro scale devices has lead to the development of several promising new technologies. Lab on a chip technology or micro total analysis systems (μ-TAS) are an important result of this technological advance. μ-TAS devices incorporate several chemical analysis and processing operations onto a single microchip. These devices have many benefits including, portability, reagent economy, high speed, ease of automation, and disposability. μ-TAS devices are most relevant to emerging fields in the life sciences such as genomics and proteomics, which require high speed analytical methods. There are also many applications for μ-TAS in the pharmaceutical industry for uses in combinatorial chemistry for drug discovery or point of care clinical analysis [1].

μ-TAS devices can be thought of as being composed of the same unit operations as their macro-scale counterparts; however, the phenomena involved in μ-TAS devices are complicated by geometry and non-standard operating regimes. In general, a μ-TAS device will be composed of some combination of micro-mixers/splits, micro-reactors, and micro-separators. Of these unit operations, micro-separators, specifically micro electrophoresis encompasses a large area of research into μ-TAS devices. Micro scale electrophoresis is a very valuable technique for the separation of bio-molecules, combining the possibility of high resolution and throughput in a compact design [2]. In this paper, the effect of compact channel topology on the design of micro scale electrophoretic systems will be discussed.

2 Scope of Work

Currently, designers of micro-electrophoretic systems use one of two different design methodologies. In the first approach, designers iteratively fabricate and test a multitude of different design schemes based on heuristic rules and understanding [2]. The second approach is based on developing piecewise phenomenological models for specific components of micro-electrophoretic systems [3]–[5]. As of yet, there are no formal methodologies for the design of micro-electrophoretic devices, but practical designs are expanding. Both of the above mentioned design methodologies are acceptable for the design and analysis of simple electrophoretic channel topologies, where geometry and initial conditions are pre-specified. However, the confined area of a microchip often requires complex channel topologies. Also, it is frequently desirable to investigate a large number of channel geometries and operating conditions in order to identify superior designs. Because of these inherent complexities, the current methodologies which rely on experimental and PDE models of electrophoretic systems quickly become intractable for use in design and optimization.

In this paper, a strategy for comparing the performance of serpentine and spiral channel topologies will be presented. Special attention will be given to the evaluation of device performance versus chip area used. It will be shown that the appropriate selection of channel topology has a significant impact on the design and ultimate performance of micro scale electrophoretic separation systems. The core of this strategy involves the creation of a micro-electrophoretic simulation engine, the creation of layout algorithms for channel topology generation, and a methodology for the selection of superior solutions from a set of candidate designs. This approach is capable of efficiently investigating a large number of feasible designs in a very short period of time. An efficient and accurate strategy for the design of micro-electrophoretic devices is crucial to achieve the enormous potential these devices have to offer.

3 Background and Terminology

Electrophoretic separation occurs because of the differential transport of charged species in the presence of an electric field. As an analyte mixture travels through an electrophoretic channel, the species within the mixture separate into bands according to their electrophoretic mobilities. All the while this separation is occurring, the species bands are broadening or dispersing due to factors such as; diffusion, geometry, Joule Heating, adsorption, and electro migration [6]. The quantity that represents the ratio of the distance between the means of two adjacent bands to the amount they have dispersed is termed resolution. Resolution characterizes separation effectiveness. Another important quantity is the minimal distance between the edges of two adjacent bands as seen by a detector. This specification coupled with a desired resolution defines the maximum amount of allowable dispersion for two adjacent bands.

A primary cause of dispersion in microchip based electrophoresis results from geometrically induced dispersion. When compact designs are desired, geometric dispersion results from the addition of turns to the design. Turns are necessary to fit the desired separation length onto a confined area. The amount of turn induced dispersion is dependent on the radius of curvature and the flow regime of species within the turn [3], [5]. Turn induced dispersion results from differences in the velocity and electric fields that particles within the band experience from the inner radius to the outer radius of a turn. Skewed bands in straight channel sections also exhibit different dispersive behavior than plug shaped bands. This is due to the larger surface area of skewed bands. In serpentine topologies, a complimentary set of turns has the potential to remove turn induced dispersion for appropriate operating conditions. The simulation engine presented in this paper is capable of predicting band dispersion and shape resulting from complex topologies and operating conditions.

4 Simulation Engine and Layout Algorithms

The concept behind the channel simulation engine is that any channel system can be decomposed into a set of component pieces or sections. Each of these sections contains an algebraic model combined with logic that captures how bands travel and disperse within that section. The underpinning phenomenological understanding that was used to develop these models was taken from the literature and from colleagues [3]–[5], [7]. At present, we divide channel systems into straight sections, turns, injectors and detectors. New section models will be implemented as research progresses.

An electrophoretic channel system can be simulated by piecing the channel sections together to produce the desired channel topology. The simulation takes in species and buffer properties and returns band variance, shape and separation time for a given topology. The simulation engine is highly flexible and versatile. Section models can be easily tested and compared. Any number of analytes and any type of buffer can be specified. A vast assortment of channel topologies can be constructed from the section models available. Figure 1 shows how information is passed within the straight section model.

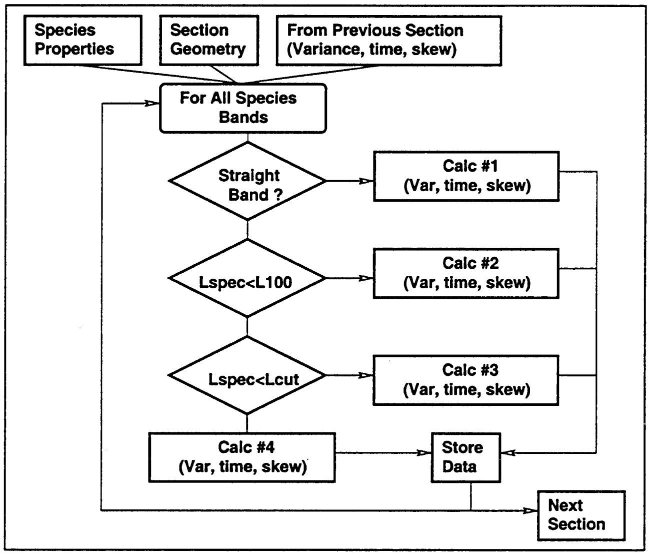

Figure 1: Flowchart for straight section model.

It is important to note that depending on the incoming band shape, the model will behave differently. This is because a skewed band disperses differently than a plug shaped band. As a skewed band travels along the channel, it slowly diffuses back to a plug like band shape. Figure 2 shows how information is passed in the turn model.

The important feature of this model is that it is capable of accurately predicting the effect of a turn on a skewed band. This feature must be captured accurately in order to demonstrate the skew canceling effect that complimentary turns have for certain operating conditions. For any band entering a turn, the band may: (1) become skewed, (2) become less skewed, (3) become more skewed (4) not be perceptibly skewed. The resulting band shape depends on the specified operating conditions and geometry of the system.

The simulator has been verified against a numerical PDE model as well as experimental data from the literature [8], [9]. For a broad range of operating conditions, the simulator produced results that were within 10% of the finite element solution for dispersion. In all cases, the simulator produced results in only seconds, while the finite element simulation took on the order of hours.

Since the simulator is capable of analyzing particular designs in only seconds, we are able to conduct parametric investigations of numerous designs in a short period of time. Currently we have developed algorithms that sequentially place channel sections according to geomet-

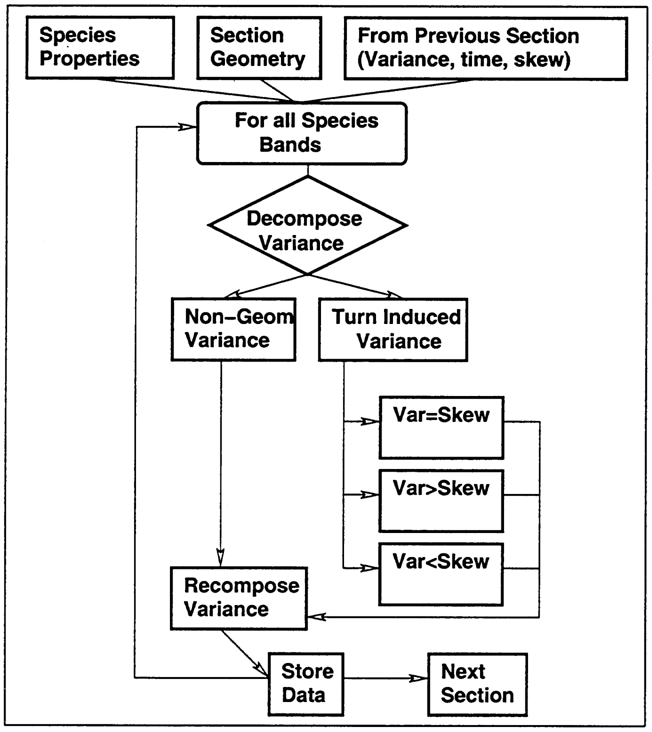

Figure 2: Flowchart for turn section model.

ric considerations. The two channel placement/packing algorithms used are for serpentine channel topologies and for spiral channel topologies. The performance of each topology can be compared for a variety of operating conditions and system geometries. Figure 3 shows how channel sections are added to a given chip for each topology.

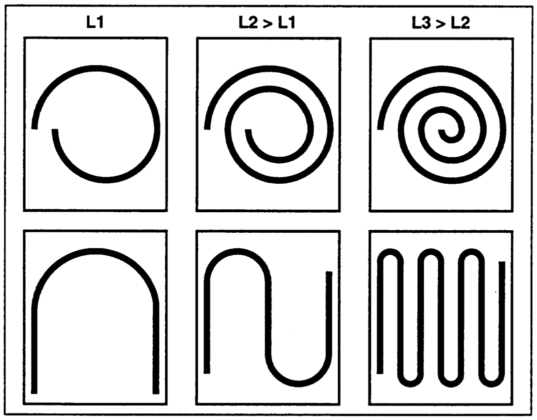

Figure 3: Length Positioning/Packing Algorithm.

As the specified length becomes longer and longer, more sections are added until no more sections will fit within the defined chip area. Figure 4 shows how separation performance changes for serpentine and spiral topologies. In this case, the spiral topology is better for much of the realistic design space. This is because, for less convective flow regimes, spiral topologies approach the dispersive behavior of straight channels.

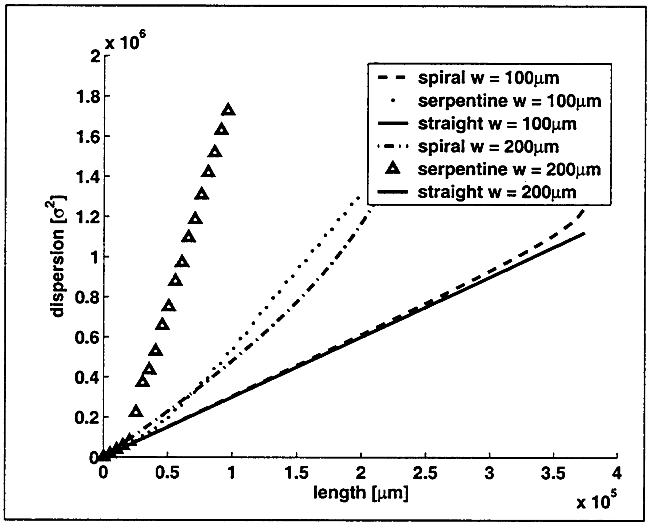

Figure 4: Dispersion vs. Length for Spiral and Serpentine Topologies (Taylor Flow) *Specs: Area* $=1cm^2$, $E = .005V/\mu m$, *substance: dichlorofluorescein.*

In Figure 5 the serpentine topology is shown to out perform the spiral topology. In this case the flow is convective. The benefits conferred by complimentary turns are most noticeable for serpentine topologies during convective flow.

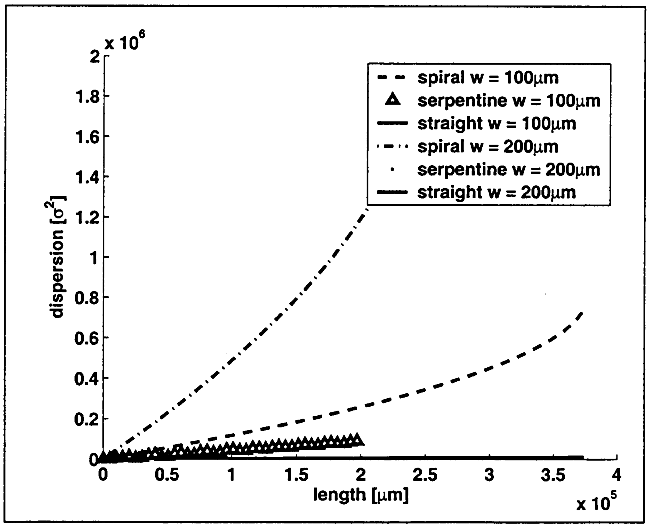

Figure 5: Dispersion vs. Length for Spiral and Serpentine Topologies (Convective Flow) *Specs: Area* $=1cm^2$, $E = .5V/\mu m$, *substance: dichlorofluorescein.*

5 Discussion of Design Methodology

An effective design technique can be implemented through the use of the simulation engine and layout algorithms. The minimum desired resolution and band separation distance must be specified based on the requirements of the detection equipment. A set of species component properties must be provided. The design space can be further bounded based on the voltage source available, and by the fact that we wish to avoid electrical breakdown and Joule Heating effects. The set of feasible designs can then be enumerated for a chip of specified area.

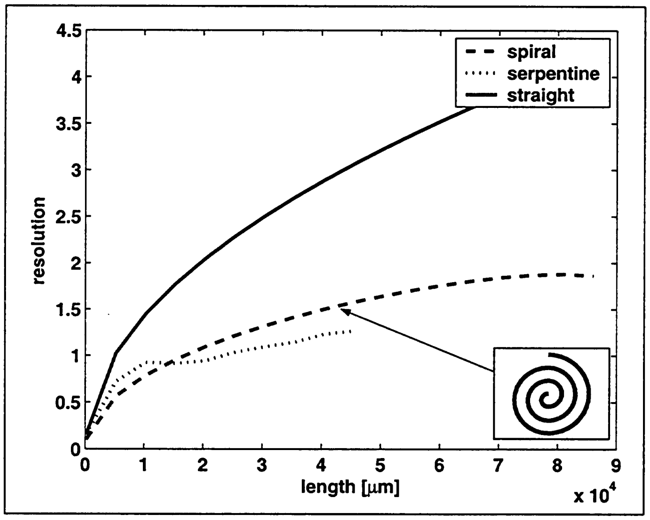

Figure 6: Resolution for Spiral and Serpentine Topologies *Specs: Area* $=.25cm^2$, $E = .005V/\mu m$, *mobilities: 5.9, 6.2* ($\times 10^{-4} cm^2 V^{-1} s^{-1}$) *Diffusivities .1, 3* ($\times 10^{-6} cm^2 s^{-1}$).

Figure 6 shows a sample design based on the separation of two species. It can be seen that if baseline resolution is desired, $R > 1.5$, only the spiral produces feasible designs at approximately 4cm length. This length corresponds to one particular spiral design. The position and length of channel sections can be readily extracted from the layout algorithms for this particular design. This design technique is made possible because of the efficiency of the simulation engine and layout algorithms.

6 Conclusion

This paper represents an initial attempt at developing systematic design techniques for electrophoretic devices. The technique is capable of quickly comparing a large number of topologically different alternatives and identify the more favorable ones. When combined with a suitable layout algorithm, this allows us to impose constraints on the area used by the channel network and thus directly address the trade-off between separation performance and physical size.

Current work has three directions: (a) refine layout generation, (b) parametric optimization within each topology, and (c) automate the search for feasible alternatives. At present, channel section layouts are based on symmetry with heuristic rules to minimize expected dispersion. While in general an optimal distribution of channel length for each sub-design is not expected to cause substantial improvements, the performance gains will be at no cost and lead to even more compact designs. Further, automatic synthesis – as a black-box tool for chip design – will improve ease of use and is seens as an integral part of design tools for complete μ-TAS devices.

Finally, more and improved section models will allow for the examination of the effect that new topologies and new physical phenomena have on chip design.

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