

IMECE2003-41289

COMPUTER-AIDED SYNTHESIS OF MICROSCALE ELECTROPHORETIC SEPARATION SYSTEMS IN CONFINED AREAS

Anton J. Pfeiffer

Department of Chemical Engineering
Carnegie Mellon University
Pittsburgh, Pennsylvania 15213
Email: pfeiffer@cmu.edu

Tamal Mukherjee

Department of Electrical
and Computer Engineering
Carnegie Mellon University
Pittsburgh, Pennsylvania 15213
Email: tamal@ece.cmu.edu

Steinar Hauan*

Department of Chemical Engineering
Carnegie Mellon University
Pittsburgh, Pennsylvania, 15213
Email: hauan@cmu.edu

ABSTRACT

Complex designs result from the desire to create compact microscale electrophoretic devices in confined chip areas. Knowledge of how the interconnectivity of electrophoretic channel sections effects chip performance is necessary to develop feasible and efficient designs. In this paper, we demonstrate an approach for the design and synthesis of microscale electrophoretic systems using computer aided simulation and optimization. We have investigated serpentine and spiral channel topologies which are commonly found in the literature. This approach is demonstrated for the design of systems in confined areas as well as the design of systems that utilize minimal area. Device performance will be evaluated in terms of plate number and resolution and limited by available voltage, detector and fabrication constraints.

NOMENCLATURE

A chip area
D molecular diffusivity
 D_{eff} effective diffusivity
dL band separation distance
 d_i band distance
E electric field strength
L separation length
 L_{axial} start of transverse diffusion regime

L_{unskew} end of transverse diffusion regime
N plate number
PAD inter-channel spacing
Pe Peclet number
R resolution
 r_c center turn radius
TR r_c/w minimum turn radius
w channel width
X input response function
 x_i x edge coordinate
 y_i y edge coordinate
 ΔL skew length
 ΔX x chip dimension
 ΔY y chip dimension
 ϕ skew angle
 σ band standard deviation

INTRODUCTION

The ability to fabricate increasingly complex microscale devices has lead to the development of several promising new technologies. Lab on a chip technology or micro total analysis systems (μ -TAS) is an important result of this technological advance. μ -TAS devices incorporate several chemical analysis and processing operations onto a single microchip. These devices have many benefits including portability, reagent economy, high speed, ease of automation, and disposability [1]. μ -TAS devices are most relevant to emerging fields in the life sciences such as

*Corresponding author.

genomics and proteomics, which require high speed analytical methods. There are many applications for μ -TAS in the pharmaceutical and biomedical industries for uses such as drug discovery and point of care clinical analysis [2].

In our view, μ -TAS devices can be thought of as being composed of the same unit operations as their macro-scale counterparts; however, the phenomena involved in μ -TAS devices are complicated by geometry and non-standard operating regimes [3]. In general, a μ -TAS device is composed of some combination of micro-mixers/splits, micro-reactors, and micro-separators. Of these unit operations, chip based electrophoresis is a separation technique that is receiving a great deal of attention [4]. Microscale electrophoresis is a very valuable technique for the separation of biological molecules, combining the possibility of high resolution and throughput in a compact design [5]. In this paper, an approach for the design and synthesis of electrophoretic systems in compact areas will be discussed.

Scope of Work

Typically, designers of chip based electrophoretic systems have used three different design methodologies. In the first approach, designers iteratively fabricate and test a multitude of different design schemes based on heuristic rules and understanding [5]. The second approach is based on developing phenomenological models for specific components of micro-electrophoretic systems [6,7]. In the third approach, the underlying PDE description of electrophoretic phenomena is solved by discretizing the equations in both time and space [8]. Large scale optimization of the PDE description [9] has been used to optimize a critical component in the system. However, such component optimization strategies may lead to sub-optimal system designs.

As of yet, there are no formal methodologies for the design of micro-electrophoretic devices, but practical designs are expanding. The current design methodologies are acceptable for the design and analysis of simple electrophoretic channel topologies, where geometry and initial conditions are pre-specified. However, the search for optimal designs within confined areas often requires the examination of complex channel topologies and large numbers of channel geometries and operating conditions. The time requirements for laboratory or numerical experiments becomes exponentially high.

Our approach begins to address the design and synthesis of chip based electrophoretic systems in compact areas. Special attention will be given to the evaluation of device performance versus chip area used. It will be shown that the appropriate selection of channel topology has a significant impact on the design and performance of micro scale electrophoretic separation systems. The core of this strategy involves the creation of an electrophoresis simulation engine, the creation of heuristic based layout algorithms for channel topology generation, and a methodology for the selection of superior solutions from a set of candidate designs

based on numerical optimization. This approach is capable of efficiently investigating a large number of designs in a short period of time.

Background and Terminology

Electrophoretic separation occurs because of the differential transport of charged species in the presence of an electric field. As an analyte mixture travels through an electrophoretic channel, the species within the mixture separate into bands according to their electrophoretic mobilities [10]. Fig. 1 is a schematic representation of two species bands being separated as they travel down an electrophoretic channel. All the while separation is oc-

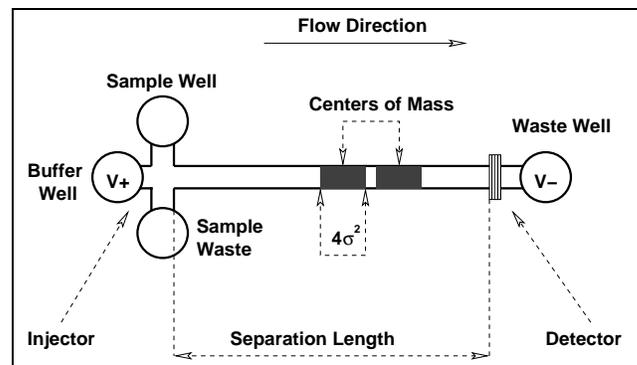


Figure 1. SCHEMATIC OF SIMPLE CHIP BASED ELECTROPHORETIC SYSTEM.

curing, the species bands are broadening or dispersing due to factors such as diffusion, geometry, Joule Heating, adsorption, and electro migration [11]. The quantity that represents the ratio of the distance between the means of two adjacent bands to the amount they have dispersed is termed resolution Eqn. (1):

$$\text{Resolution} = R = \frac{(d_2 - d_1)}{4\sigma_{avg}} \quad (1)$$

Resolution characterizes separation effectiveness [12]. However, resolution alone does not impose a precise limit on detectability. In order for a species band to be detectable, it must have a concentration greater than a particular threshold [13] and must be at least a particular distance from adjacent bands. These specifications coupled with a desired resolution define the maximum amount of allowable dispersion for two adjacent bands.

A metric that characterizes separation efficiency is known as the theoretical number of plates, Eqn. (2) [12].

$$\text{Plate Number} = N = \frac{\text{Length}^2}{\sigma^2} \quad (2)$$

This quantity is proportional to the number of species that can be simultaneously resolved by the particular separation system. In typical electrophoretic systems, plate number can be on the order of 10^5 to 10^6 [10].

A primary cause of dispersion in microchip based electrophoresis results from geometrically induced dispersion. When compact designs are desired, geometric dispersion results from the addition of turns to the design. Turns are needed to fit the required separation length onto the confined area of a microchip. The amount of turn induced dispersion is a function of the radius of curvature, channel width, and flow regime. [6, 9, 14, 15]. Turn induced dispersion results from differences in the velocity and electric fields that particles within the band experience from the inner radius to the outer radius of a turn. Skewed bands in straight channel sections also exhibit different dispersive behavior than plug shaped bands [16]. This is due to the fact that skewed bands can disperse both axially and transversely as they travel along a channel (Fig. 2).

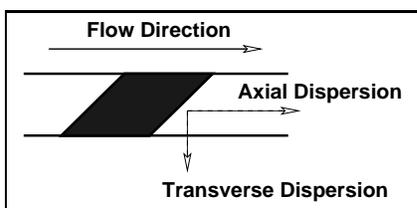


Figure 2. SKEWED BAND DISPERSING IN A STRAIGHT CHANNEL.

In serpentine topologies, a complimentary pair of turns has the potential to remove turn induced dispersion for appropriate operating conditions [9]. The simulation engine presented in this paper is capable of predicting band dispersion and shape resulting from complex topologies and operating conditions.

Throughout this paper, certain quantities will be grouped together and referred to as either *performance constraints*, *operational constraints* or *physical constraints*. The performance constraints allow for the specification of separation performance. Operational constraints are due to choices concerning equipment and hardware, such as voltage source and detection scheme. Physical constraints result from fabrication limitations and regions of model validity. Tab. 1 lists some examples of constraints that fall into these categories and their associated values. These constraints, along with appropriate species and buffer properties, serve to realistically bound the feasible design space [12, 17, 18].

COMPUTER AIDED DESIGN AND SYNTHESIS TOOLS

A micro-electrophoretic simulation engine and a set of topology packing algorithms form the key pieces of our ap-

Performance	Operational	Physical
$N > 10^5$	$R > 1.5$	$w \in [10, 100] \mu m$
$H < 10 \mu m$	$dL > 10 \mu m$	$A < 25 cm^2$
$t < 5 min$	$V < 30 kV$	$E < 40 kV/cm$

Table 1. TYPICAL CONSTRAINTS AND THEIR NUMERICAL VALUES.

proach. The simulation engine is used to quickly evaluate a fixed channel topology. The topology packing algorithms systematically propose new channel topologies for the simulator to investigate. Iterative communication between the simulator and the packing algorithms allows for the systematic exploration of the design space for feasible designs. The inputs that our algorithms require are: values for the physical constraints, species properties, buffer properties, operating conditions and performance constraints.

Simulation Engine

The concept behind the channel simulation engine is that any channel system can be decomposed into a set of component pieces or sections. Each of these sections contains an algebraic model combined with logic that captures how bands travel and disperse within that section. The underpinning phenomenological understanding that was used to develop these models was taken from the literature [6, 7, 9, 16].¹ At present, we divide channel systems into straight sections, turns, injectors and detectors. Implementation of additional section models – such as arbitrary bends, injectors, detectors and channels that are geometrically tapered – will be implemented as research progresses.

Currently, we have used only two dimensional models of dispersion in microchannels. The only model that considers the effect of channel depth on dispersion is the Joule heating model [19]. As the the required level of simulation detail increases, we will implement models that incorporate three dimensions and the effects of channel cross-section on dispersion. Improved models can be readily implemented in our preexisting framework. Our design synthesis methods are independent of the underlying phenomenological models.

Fig. 3 shows a representation of the simulator architecture. It can be seen that this architecture is independent of the underlying section models. An electrophoretic channel system can be simulated by piecing the channel sections together to produce the desired channel topology. The simulation takes in species and buffer properties and returns band variance, shape and separation time for a given topology. We are able to estimate and quantify the impact of geometric dispersion, diffusion and Joule Heating [19]. Different section models can be readily tested and

¹see notes

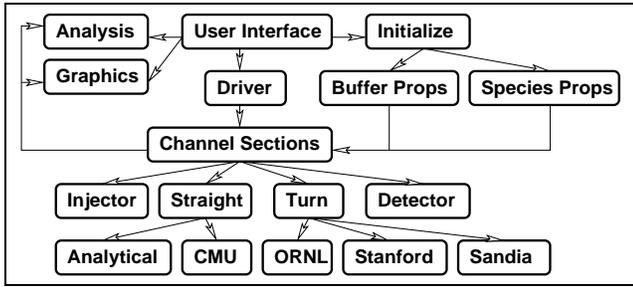


Figure 3. SIMULATION ENGINE ARCHITECTURE.

compared. Given the required physical properties, systems with various analytes and buffers can be simulated. An assortment of channel topologies can be constructed from the section models available.

Fig. 4 shows how information is passed in the turn model. Unlike earlier work where the input bands to turn models were

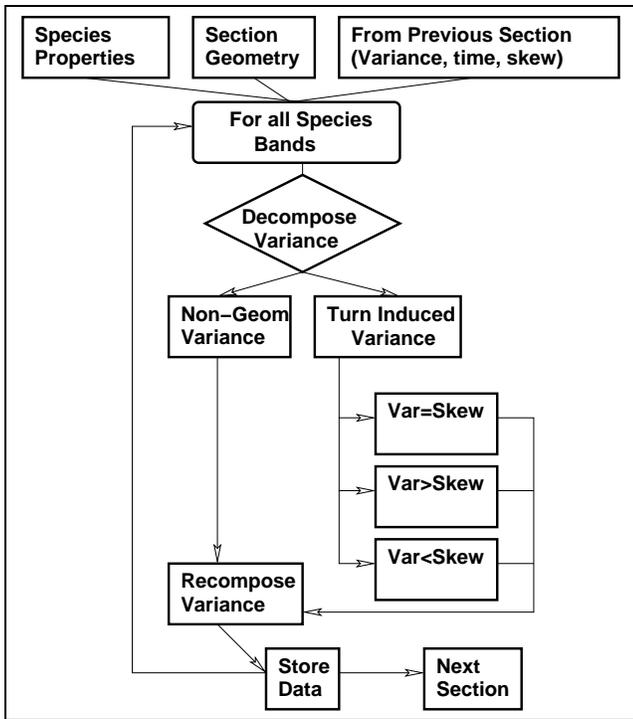


Figure 4. FLOWCHART FOR TURN SECTION MODEL.

orthogonal to the channel walls [5–7, 9], our model is capable of predicting the effect of a turn on a skewed band. This feature must be captured accurately to demonstrate the skew canceling effect that complimentary turns have for certain operating conditions [9]. We have developed a conceptual framework to char-

acterize what happens to an arbitrarily skewed band as it travels through a turn. For any band entering a turn, the band may: (1) become skewed, (2) become less skewed, (3) become more skewed (4) not be perceptibly skewed. The resulting band shape depends on the specified operating conditions and geometry of the system. The concept of band shape used here is a characterization technique rather than an indication of physical band shape. It is used to systematically capture the effect of multiple turns on an arbitrarily skewed band.

We have implemented phenomenological descriptions of band spreading in turns from various authors [6, 7, 9]. The total dispersion of a band traveling through a turn can be decomposed into contributions from geometry and contributions from diffusion and Joule Heating. After the dispersion has been decomposed, the two aspects of dispersion can be dealt with separately. For serpentine topologies geometric dispersion can be quantified according to the band's variance, Eqn. (3):

$$\sigma_i^2 = \sigma_{turn}^2 - \sigma_{i-1}^2 \quad (3)$$

The geometric dispersion for section i is the difference between the geometric dispersion calculated by one of the phenomenological models and the geometric dispersion from the previous section $i - 1$. From Eqn. (3) it can be seen that the potential exists for geometric dispersion to be completely canceled. The sign of the quantity σ_i^2 can be interpreted within the conceptual framework described previously. A $\sigma_i^2 < 0$ indicates that the band skew was under-corrected while traveling through the complimentary turns. A $\sigma_i^2 > 0$ corresponds to band skew being over-corrected. The sign of σ_i^2 is retained as this quantity travels from section to section. For spiral topologies, Eqn. (3) is modified. Instead of subtracting terms, σ_{model}^2 and σ_{i-1}^2 are added because there is no potential for skew canceling. The total dispersion leaving the turn is given by Eqn. (4):

$$\sigma_{total}^2 = \sigma_{JH}^2 + \sigma_D^2 + |\sigma_i^2| \quad (4)$$

The variance due to Joule Heating, diffusion and the absolute value of the variance due to geometry are added to obtain the total dispersion for that section.

Fig. 5 shows how information is passed within the straight section model. Depending on the incoming band shape, the model will behave differently. Skewed bands disperse differently than plug shaped bands. As a skewed band travels along the channel, it slowly diffuses back to a plug like band shape since a skewed band can diffuse in both the axial direction as well as the radial direction perpendicular to the channel walls (Fig. 2).

We have implemented a phenomenological model that captures the transverse diffusion of skewed bands in straight channel sections [16]. This model divides a straight section into three

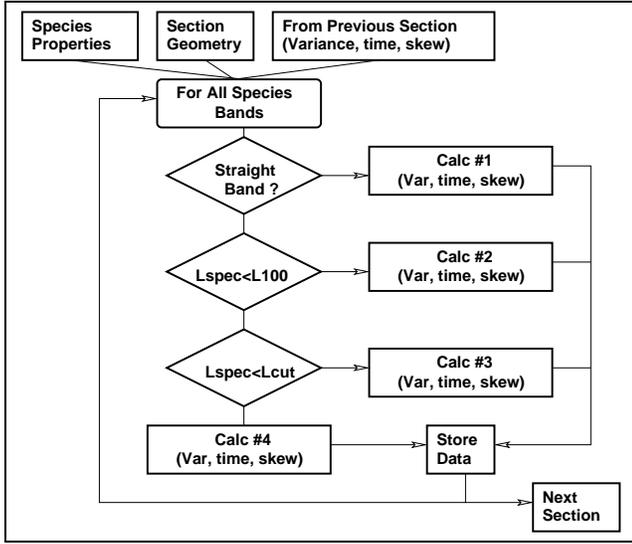


Figure 5. FLOWCHART FOR STRAIGHT SECTION MODEL.

regimes. The first regime is a relatively short section in which no transverse diffusion occurs. This regime extends until a theoretical length limit denoted by $L_{axial} = \frac{Pe \cdot w}{1000}$.² The next regime extends between L_{axial} and a length called L_{unskew} . This quantity is a function of the incoming skew angle ϕ_{i-1} . In this region, transverse diffusion occurs as a function of an effective diffusivity D_{eff} . After L_{unskew} , the band is no longer skewed and is now a plug.

If the band is in the region $[L_{axial}, L_{unskew}]$, then the geometric variance from the previous section must be translated to skew angle. This is done in Eqns. (5) and (6).

$$\Delta L = (X \cdot |\sigma_{geom}^2|)^{1/2} \quad (5)$$

$$\phi_{i-1} = \tan^{-1}\left(\frac{w}{\Delta L}\right) \quad (6)$$

The skew length, ΔL , calculated by Eqn. (5) is a function of the absolute value of the geometric dispersion from the previous section and an input response function X . In our case, we assume that $X = 12$ which corresponds to that of a plug shaped band [6, 20]. The skew angle of the incoming band, ϕ_{i-1} , calculated by Eqn. (6) is a function of the channel width and skew length. The new skew angle is calculated using D_{eff} from [16] and the molecular diffusivity D in Eqn. (7).

$$\phi_i = \sin^{-1}\left(\left(\frac{D}{D_{eff}}\right)^{1/2}\right) \quad (7)$$

Eqn. (7) quantifies the impact of transverse diffusion. Finally,

the geometric variance based on ϕ_i must be calculated by Eqn. (8).

$$\sigma_i^2 = \frac{\left(\frac{w}{\tan(\phi_i)}\right)^2}{X} \quad (8)$$

The sign of σ_i^2 must be reset to equal that of the incoming variance. The total variance for the section is then calculated by Eqn. (4). It is important to note that the axial contribution to variance in this section is calculated using the molecular diffusivity ($2Dt$) and is not calculated using the effective diffusivity (D_{eff}) as band skew is handled separately.

Preliminary verification of the simulator has been performed against a numerical PDE model as well as experimental data from the literature [17, 21]. It appears that for a reasonably broad range of operating conditions, the simulator produced variances that were usually within 10% of the finite element solution for dispersion. In all cases, the simulator produced results in only fractions of a second, while the finite element simulation took on the order of hours. Continued validation studies are on-going.³

Channel Packing Algorithms

Since the simulator is capable of quickly analyzing individual designs, we are able to conduct parametric investigations of numerous designs in a short period of time. Currently we have developed algorithms that sequentially place channel sections according to geometric considerations. The constraints on channel packing are the channel width (w), the minimum allowable turn radius (TR), and the inter-channel spacing or *channel padding* (PAD) between adjacent channels. The two channel placement/packing algorithms used are for serpentine channel topologies and for spiral channel topologies. The performance of each topology can be compared for a variety of operating conditions and system geometries. Fig. 6 shows how channel sections are added to a given chip for each topology. As the required length increases, more sections are added until no more sections will fit within the defined chip area due to the packing constraints.

The channel packing algorithms not only serve as a channel design generation method, but also impose important bounds on the feasible design search space. The channel packing algorithms are capable of determining the minimum number of sections for a given length and the maximum length and number of sections that can fit on a given chip. These bounds are important because they give a defined scope to the number of sections that must be searched to find a feasible design.

²modified from [16]

³see notes

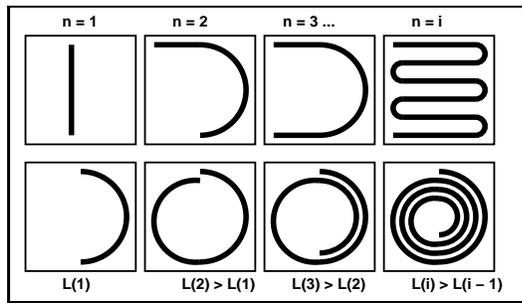


Figure 6. SECTION PLACEMENT/PACKING ALGORITHMS.

Area Constraints

A set of area constraints were developed for use with numerical optimization. Serpentine or spiral topologies are required to fit within the dimensions specified by the area constraints. The area constraints differ from the channel packing algorithms in that they do not require symmetric placement of channel sections or use of the entire specified chip area. The area constraints allow for a more rigorous analysis of the feasible design space.

The dimensions of a design are determined by assigning Cartesian coordinate points to the ends of every channel section. The initial point is set arbitrarily at $p_0 = (0, 0)$. The position of subsequent points are all tracked relative to this reference coordinate. Once the coordinates of all of the sections are set, the possible chip edges can be determined by simply adding the associated channel widths and channel spacing (PAD) in the appropriate x and y directions. The chip dimensions are then calculated by Eqns. (9) and (10).

$$\Delta X = \max(x_i) - \min(x_i) \quad (9)$$

$$\Delta Y = \max(y_i) - \min(y_i) \quad (10)$$

The difference between the maximum and minimum edge coordinates in the x and y directions give the associated chip dimensions. The area (A) is calculated as the product of ΔX and ΔY . The area constraints are implemented as a sequence of linear relations; a significant advantage [22] within an optimization framework.

Analysis of Topology Trade-offs

We have examined the design trade-offs that result from changes in topology from two perspectives. In the first perspective, a fixed chip area and operating conditions are specified. The resulting system performance is analyzed as separation length is systematically added to the topology. This results in an increase in the number of channel sections and channel packing density. In the second perspective, we examine how system performance is effected by systematically decreasing available chip area for a

specified separation length and operating conditions. This also increases the number of channel sections and channel packing density. These two perspectives enable us to formulate a design approach that is capable of selecting feasible designs that meet the constraints on system performance for various operating conditions.

Figs. 7 and 8 show how dispersion is effected as channel sections are packed onto a chip of given area. The length range examined is from the lower bound on channel length to the upper bound on channel length. The lower bound is the shortest length required for a straight channel to achieve the desired band separation distance (dL). The upper bound is the length at which no more sections can be added without violating the geometric constraints in the channel packing algorithm. In both graphs, the performance of a straight channel that is not constrained to fit in the desired area is plotted as an upper bound on system performance.

Fig. 7 shows how separation performance changes for serpentine and spiral topologies. In this case, the spiral topology is better for most of the realistic design space. This is because, for less convective flow regimes, spiral topologies approach the dispersive behavior of straight channels. In Fig. 8 the serpentine

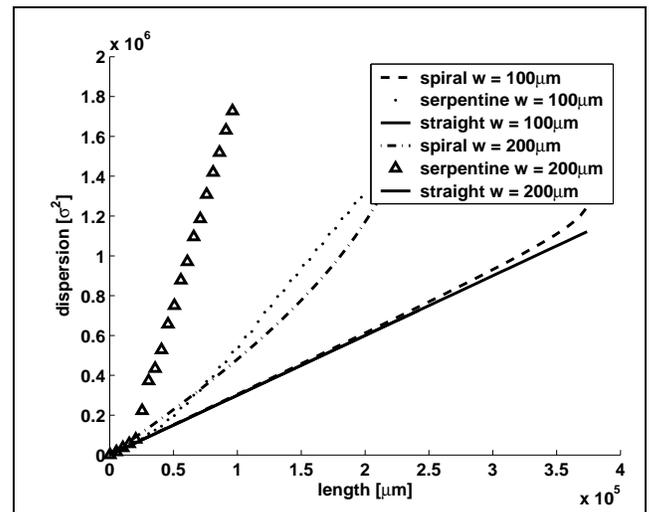


Figure 7. DISPERSION VS. LENGTH FOR SPIRAL AND SERPENTINE TOPOLOGIES (Taylor Flow) Specs: Area = 1cm^2 , $E = 50\text{V/cm}$, species: dichlorofluorescein, buffer: Sodium Tetraborate/HEPES.

topology is shown to out perform the spiral topology. In this case the flow is convective. The benefits conferred by complimentary turns are most noticeable for serpentine topologies during convective flow [6, 17].

In Fig. 9 we examine how diminishing available chip area

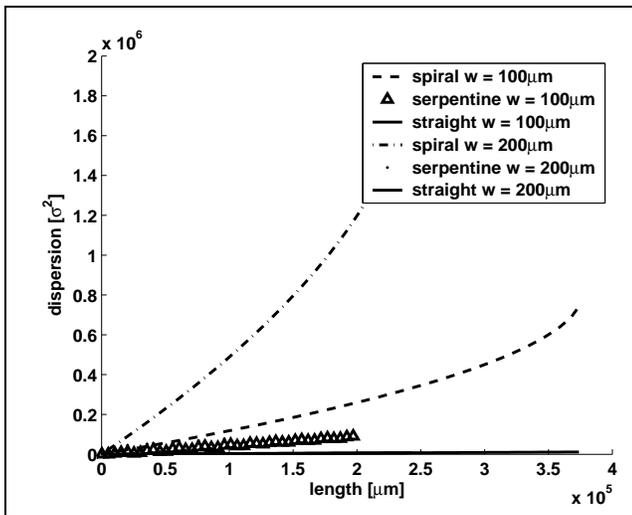


Figure 8. DISPERSION VS. LENGTH FOR SPIRAL AND SERPENTINE TOPOLOGIES (Convective Flow) Specs: Area = 1cm², E = 5000V/cm, species: dichlorofluorescein, buffer: Sodium Tetraborate/HEPES.

for a fixed separation length, affects system resolution. The straight line at the top of the graph represents the performance of a straight channel section that is not required to fit within the given area. This provides an upper bound on system performance. Both the spiral and serpentine topologies are constrained to fit within the specified area. As the available area is reduced from right to left, the number of channel sections for both topologies increases in order to fit the required separation length on the chip.

For spirals, as area decreases and sections are added, resolution continuously diminishes. This is because as spiral sections are added, band skewing increases due to the decrease in the turns' radii of curvature. The serpentine is less intuitive. This is because the heuristic packing algorithm for the serpentine attempts to fill the entire available chip area (Fig. 6). This leads to systematic discontinuities in performance. The serpentine section numbers are labeled on the graph at the point each new section is added. At the start of the graph, the performance of a single serpentine section is identical to the straight upper bound (1). As area decreases, a turn is added and there is a discontinuous change in topology (2). The turn results in a discontinuous reduction in resolution due to the higher dispersion generated by a turn. The resolution continues to decrease until a third straight section is continuously added (3). The straight section attempts to compensate for some of the loss in resolution resulting from the turn. Next, there is a surprising jump in resolution and a jump in section number (*from 3 sections to 5 sections*). The fact that the 4 section topology was skipped is because for this aspect ratio chip, a 4 section topology does not provide more overall separa-

tion length than a 3 section topology. The jump in dispersion can be explained by the skew canceling effect of complimentary turns. When the sixth section is added, there is a discontinuous drop in resolution corresponding to the addition of a turn.

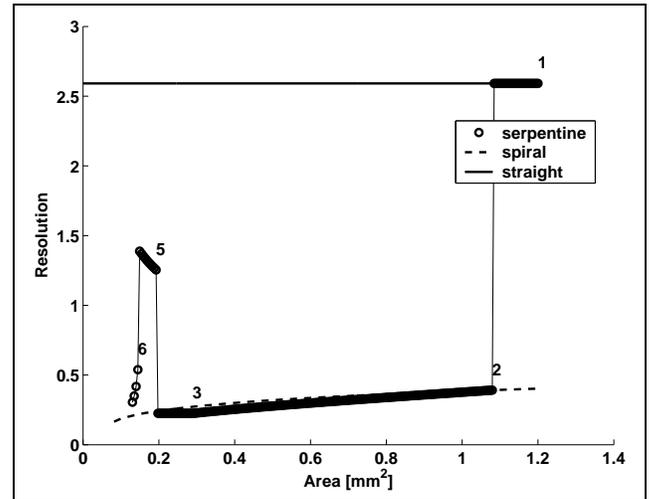


Figure 9. AREA VS. RESOLUTION FOR SPIRAL AND SERPENTINE TOPOLOGIES (Specs: Aspect ratio $\frac{\Delta X}{\Delta Y} = 1$, L = 1mm, V = 1000V).

Figs. 7, 8 and 9 show that when designing electrophoretic systems in confined areas, the appropriate design decisions are not always obvious. In Figs. 7 and 8, we observe how a heuristic rule based on flow regime and channel geometry could be used to select the appropriate channel topology when the flow is either clearly convective or clearly diffusive. However, there are a broad range of intermediate flow regimes where it is not clear which topology is more appropriate. Furthermore, Fig. 9 indicates that the number, type and placement of sections plays an important part in system performance. This is evident in the discontinuous jump in resolution from the 3 section topology to the 5 section topology. It is also not always true that filling the entire available chip area with channel sections results in the best system performance. This is made apparent by the subtle increase in system performance for the 5 section serpentine as the area is reduced. For any given topology, there is an optimal distribution of channel section lengths that may or may not use the entire available chip area. Our design approach has begun to address these issues.

DESIGN APPROACH

Our design approach automatically searches for feasible designs for both the serpentine and spiral topologies. All feasible designs must meet the user specified operational, physical and

performance constraints mentioned earlier. Once the set of feasible designs has been found, a design that most meets the needs of the designer can be chosen from among this set.

Our design approach addresses two possible scenarios that arise when attempting to construct electrophoretic separation systems in confined areas. In the first scenario, the designer has a specified area in which to design a system. Bounds are placed on the operating conditions and the design space is searched for feasible designs that meet the performance specifications. In the second scenario, the designer wishes to know the design which occupies the smallest area on the chip but still satisfies the bounds on operating conditions and performance specifications.

We have addressed the first design scenario using an iterative heuristic design approach and an iterative optimization design approach. In the iterative heuristic design approach, separation length is iteratively searched. The packing algorithms are used to determine the number, type, placement and length of each section. The initial channel length is determined by the length of a straight section that satisfies the constraint on separation distance (dL). The search is continued until no more channel length can fit in the specified area due to geometric constraints within the channel packing algorithms. While this method is fast, (< 10 seconds/1000 function evaluations), it cuts off part of the feasible design space. It is only capable of examining designs that use the entire available chip area and is not capable of evaluating an asymmetric distribution of section lengths.

We have started to address the shortcomings of the iterative heuristic method by implementing an iterative optimization design approach. In this method, the number of possible channel sections is enumerated and optimized independently. The lower bound on number of sections is determined by using the channel packing algorithms to translate the initial length from the iterative heuristic algorithm into a minimum number of channel sections. The upper bound on the number of channel sections corresponds to the maximum number of sections capable of fitting within the chip area as determined by the channel packing algorithms. A sequential quadratic programming (SQP) optimization routine [23] is used to size the design with the lowest possible dispersion. The optimizer constrains both separation performance and the bounds on chip area. This method searches a much larger portion of the feasible design space by considering asymmetric channel length distributions and designs that do not use the entire chip area. While this method is more rigorous, it is slow due to the fact that we desire to avoid local convergence. The non-ideal nature of the equations within the section models make it possible to converge to locally infeasible or locally optimal solutions. A non-biased multi-start method is employed to initialize the optimization of each sub-design. This approach significantly increases the number of function evaluations and therefore solution time.

We have also developed a method for addressing design scenarios in which we desire to minimize design area. Again, an

iterative optimization design approach is employed. In this case, the designer wishes to minimize the area of the separation system while maintaining a desired level of system performance. As in the previous method, designs are iteratively searched for the one that results in the lowest area usage subject to the operational performance and physical constraints. The method described in the *Area Constraints* section is used to calculate the area used by the design. This method is capable of significantly compacting designs while ensuring that the desired level of performance is maintained. This method has some of the same local convergence issues as noted earlier.

Iterative Heuristic Design Results

Fig. 10 is an example of the first scenario in which area and operating conditions are specified and an attempt is made at achieving the desired performance criterion. In this example we have placed bounds on resolution ($R > 1.5$), band separation distance ($dL > 10\mu\text{m}$) and electric field strength ($E < 10\text{kV/cm}$). We have specified the available chip area ($A = 1\text{mm} \times 1\text{mm}$) and the voltage source ($V = 2\text{kV}$). The designs are further constrained by the implicit assumptions within the channel packing algorithms.

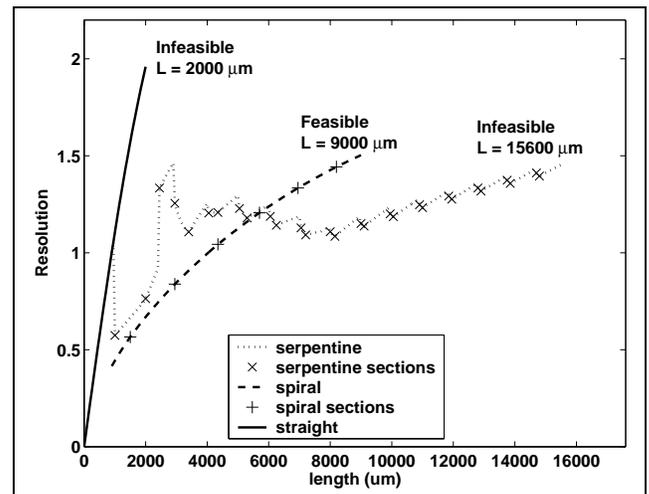


Figure 10. ITERATIVE HEURISTIC DESIGN EXAMPLE - Specs: $A = 1\text{mm}^2$, $V = 2\text{kV}$, 5 component mixture, computation time < 20 sec.

The separation length is increased from the minimum length required to achieve the required band separation distance to the maximum length that can be fit on the chip by either a serpentine or spiral topology.

The solid line, which shows the performance of a straight channel section, represents the upper bound on system performance, however, a single straight section is infeasible. The

straight channel section must be 2mm long to satisfy the constraints on electric field and resolution. This is too long to fit within the dimensions of the chip. The dotted line represents the search for a feasible serpentine topology. It duplicates the straight section up to the point where the straight section becomes infeasible due to channel padding requirements. When the straight section becomes infeasible, a turn is added which leads to a discontinuous drop in resolution. The serpentine is continuously searched until the upper bound on channel length is reached. This upper bound is determined by the constraints within the channel packing algorithm. The dashed line represents the search for a feasible spiral topology. After seven sections, all of the constraints of the spiral design have been met.

Iterative Optimization Design Results

Fig. 11 is an example of the second scenario where area is minimized subject to constraints on operating conditions and system performance. In this example, we have bounded the plate number ($N > 10^6$) and band separation distance ($dL > 10\mu\text{m}$). We have also bounded the voltage source ($V < 30\text{kV}$) and electric field strength ($E < 1.2\text{kV/cm}$). The minimum and maximum number of possible sections that bound the search space are determined by the channel packing algorithms. Spiral sections are

increase in required voltage.

The design experiment presented here is very similar to the spiral device presented by Culbertson et.al [17]. The Culbertson device was fabricated on a $5\text{cm} \times 5\text{cm}$ chip and had a performance of over 10^6 theoretical plates. If we neglect the area required for waste and injection wells, our iterative optimization method indicates that the area required for the separation channel could be reduced to 1.1cm^2 . Approximately 16 spiral designs of the same performance could readily fit in the original area.

CONCLUSION

We have implemented design algorithms that search for feasible designs for the serpentine and spiral topologies. The search is bounded by user specified constraints on chip fabrication capabilities, operational constraints, and desired separation performance. We have demonstrated that developing feasible micro electrophoretic designs in compact areas is a complex process that requires knowledge of input conditions, channel placement, channel geometry and desired performance.

Our design methodologies can be used to generate feasible designs in only minutes that would typically take months to generate using current standard practices. Our heuristic based methods allow for effective approximate exploration of the design space. However, this approach only searches a subset of the feasible region. We have begun to incorporate more rigorous numerical optimization techniques that allow us to obtain detailed design information without the use of heuristics. We are developing the ability to automatically design complex systems in a systematic and efficient way. This capability is of increasing importance as our design methodology is extended to multi-unit devices that may incorporate reaction, mixing and separation systems on a single chip.

Future work will focus on more sophisticated initialization and formulation techniques which will improve the speed and robustness of our algorithms. Incorporation of new and improved section models, such as the inclusion of more rigorous injector and detector models, will be an ongoing activity. The effects that these new models have on system performance and design area will be examined. The goal of our work is a methodology for the synthesis of complete lab-on-a-chip systems.

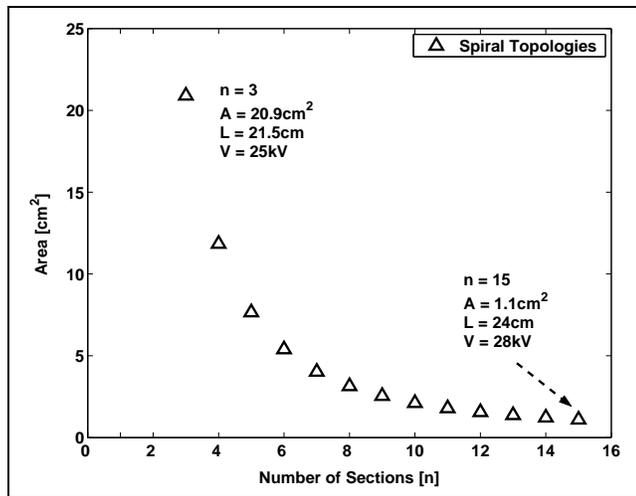


Figure 11. ITERATIVE OPTIMIZATION DESIGN EXAMPLE - Bounds: $V < 30\text{kV}$, $E < 1.2\text{kV/cm}$, $N > 10^6$, $dL > 10\mu\text{m}$.

iteratively increased from the fewest sections that produce a feasible result to the point at which there is little change in the chip area. Each design is then optimized using *SQP*. It can be seen that a change from a three section design to a 15 section design results in a 95% reduction in required chip area with only a small

ACKNOWLEDGMENT

This work is funded by contract #F30602-01-2-0587 in the SIMBIOSYS program run by DARPA and the US Air Force Research Laboratory. The authors also want to acknowledge fellow group members for model development, validation and constructive criticism: Profs James F. Hoburg (ECE) and Qiao Lin (MechE) and their students Bikram Baidya, Ryan S. Magargle, Yi Wang, Michael D. Vahey, Jeremy H. Elman and Syed W. Husain.

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Method	Metric	Pe = 30	Pe = 1000	Pe = 2000
Numerical	σ^2 (μm^2)	2530	571	333
	time (min)	11.3	58.0	60.5
Simulator	σ^2 (μm^2)	2530	540	295
	time (min)	< 1sec	< 1sec	< 1sec

Table 2. MODEL VALIDATION AND TIMING

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NOTES

The section models presented in this paper are models from the literature that have been adapted to work in a component based simulation engine. Since submitting this paper we have implemented highly accurate component based models developed by Wang et.al. [24]. A comparison between the simulator using these new models and a numerical PDE simulation can be seen in Tab. 2. While the design methods presented here are independent of underlying models, we always attempt to implement the most accurate and efficient models available.