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A VERSATILE, FAST AND INEXPENSIVE MICROFABRICATION TECHNIQUE USING A ONE METAL AND ONE SILICON DIOXIDE FILM

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ABSTRACT

A versatile fabrication process that allows users to quickly construct micromachined structures using a one metal, one silicon dioxide film stack on a silicon wafer is presented. This simplified process, which we have labeled Mock CMOS or M-CMOS, (a) starts from pre-processed wafers and requires only one photolithography step, (b) provides a conductor material for actuating electrostatic and thermal devices, (c) avoids electrical shorting between metal microstructures or to the silicon substrate by using silicon dioxide as an insulator, and (d) allows quick prototyping of true CMOS-MEMS structures similar to those designed at Carnegie Mellon University (CMU). Devices successfully microfabricated with M-CMOS include surface-normal and lateral electrostatic and thermal actuators, the majority of which were designed by forty students in an Introduction to MEMS course in Fall 2001 at Carnegie Mellon University.

INTRODUCTION

The fabrication processes for Microelectromechanical Systems (MEMS) typically require a variety of lithographic, deposition and etching equipment. Depending on the type of device chosen, an array of tools and materials are available to create microstructures. Unfortunately, the fabrication of even the simplest MEMS device requires expensive and complex processing equipment. This paper presents a fabrication process that allows a quick (less than two-weeks) design-to-device turnaround using only lithographic and etching equipment. Wafers are pre-deposited with all of the necessary films using an outsourced foundry service, thus obviating the need for semiconductor deposition equipment.

Using a metal and oxide film stack over a silicon wafer, users are able to create a variety of electrostatic and thermal microstructures. The concept of using bimorph films for demonstrating micromechanical devices was first demonstrated in 1977 [1]. Petersen illustrated voltage-addressable optical modulators that were composed of gold-coated silicon dioxide

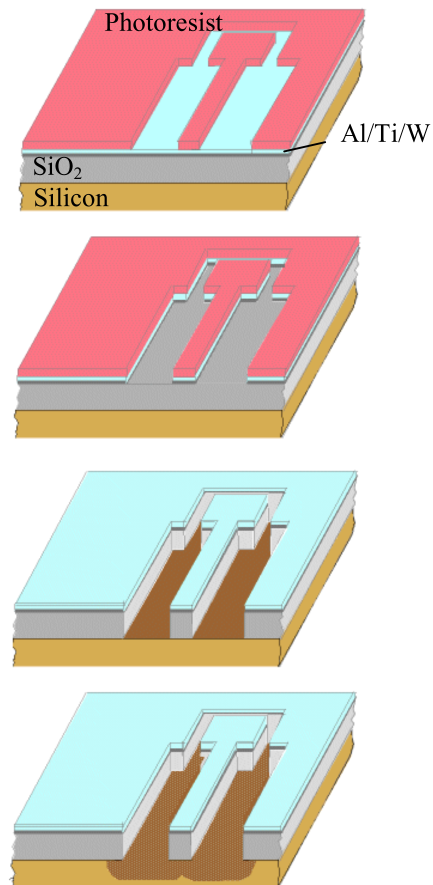

Figure 1. Fabrication procedure involves (a) Lithographic patterning of resist layer. (b) Isotropic wet etch to remove the Al and Ti/W layers. (c) Anisotropic silicon dioxide etch down to the silicon substrate. (d) Xenon difluoride etch to release the microstructures.

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cantilever beams. Bimorph microstructures using metal and oxide continue to be commonly-used fabrication process for applications such as thermomechanical and electrostatic relays [2][3]. Carnegie Mellon has developed an integrated CMOS-MEMS process in which microstructures contain various combinations of laminated films that contain silicon dioxide, aluminum, titanium tungsten, and polysilicon [4]. High-aspect-ratio composite-beam suspensions are fabricated with a sequence of dry-etching steps, where etching masks are provided by the interconnect metal layers in the standard CMOS process. This CMOS-MEMS process has been used to construct various sensor and actuator designs such as accelerometers, gyros and acoustic speakers.

Using the same morphology, consisting of a top meal mask and the bottom insulator film, the M-CMOS process follows equivalent fabrication steps to create suspended microstructures. The M-CMOS process allows designers the ability to use large wafer real estate for multiple devices or array devices at a significantly lower cost and faster turnaround compared to CMOS-MEMS foundry services. The increased real estate also enables the integration of macro devices, such as optical fibers or fluidic tubing, which typically require significant die area.

WAFER SPECIFICATION

To mimic the mechanical functionality of a 1-metal/1-oxide CMOS-MEMS die, materials and dimensions were matched as close as possible to standard CMOS processes. Wafers were purchased from an outside vendor with all three films (aluminum, titanium tungsten, and silicon dioxide) already deposited. The titanium tungsten film, used as a barrier metal and adhesion layer in the CMOS process, is included in the film stack but can be eliminated to simplify the processing. Figure 2 provides a structural comparison of a 3-metal/3-oxide CMOS-MEMS structure and a 1-metal/1-oxide M-CMOS cross section.

The pre-processed wafers were provided by *MEMS Exchange* (Reston, Virginia), an intermediary for various university and corporate fabrication centers [5]. A batch of 4-inch diameter, <100> oriented, n-type, 500 µm thick, single-sided polished, prime quality silicon wafers were used for subsequent processing. Wafers need to be sufficiently conductive to use the substrate as an electrode for electrostatic actuation, therefore wafers with a resistivity in the 1 to 20 Ω-cm range were used. The type of dopant is not important. Double-sided polished wafers should be used for cases where backside resist patterning is needed, such as in deep reactive ion etching (DRIE).

MEMS Exchange provides a thermal wet oxide on the polished wafer side, grown to a thickness of approximately 1.25 µm. The silicon dioxide film thickness on three different 24-wafer batch runs provided by MEMS Exchange has produced a varied set of numbers (1.17 µm, 1.28 µm, and 1.66 µm) according to spectrophotometric film measurement plots. A thermal wet oxide is used instead of low pressure chemical vapor deposition (LPCVD) oxide since this type of layer mimics the field oxide deposited during the local oxidation of silicon (LOCOS) process in a CMOS foundry to isolate transistors.

A 0.13 µm titanium tungsten layer was then deposited above the oxide layer, followed by a 0.44 µm thick aluminum film. These films were deposited by *Lance Goddard Association* (*LGA Films*), a *MEMS Exchange* fabrication site that can perform the cosputter of titanium and tungsten. Finally, a 0.44 µm thick aluminum film is also deposited by *LGA Films* above the titanium tungsten. Sputtering parameters used by *LGA Films* were 3 kW of power 10 mTorr of Argon pressure. For the titanium tungsten deposition, a sputtering machine is needed with cosputtering capability in order to form a balanced alloy film. To prevent any particle contamination or possible native oxide growth from the titanium tungsten layer, the aluminum was deposited immediately after the titanium tungsten without breaking vacuum in the sputtering process.

The total price for the three film depositions on a batch of twenty-four 4-inch silicon wafers costs $2000, based on February 2002 prices from *MEMS Exchange*.

FABRICATION

Starting with the pre-deposited wafers, the fabrication process first begins with a lithography step that results in a patterned photoresist layer over the top aluminum film of the wafers. *Shipley* S1813 is the positive-tone thin photoresist often used at a thickness of 1.3 to 1.5 µm. This resist has been successfully used in contact alignment down to 1 µm features.

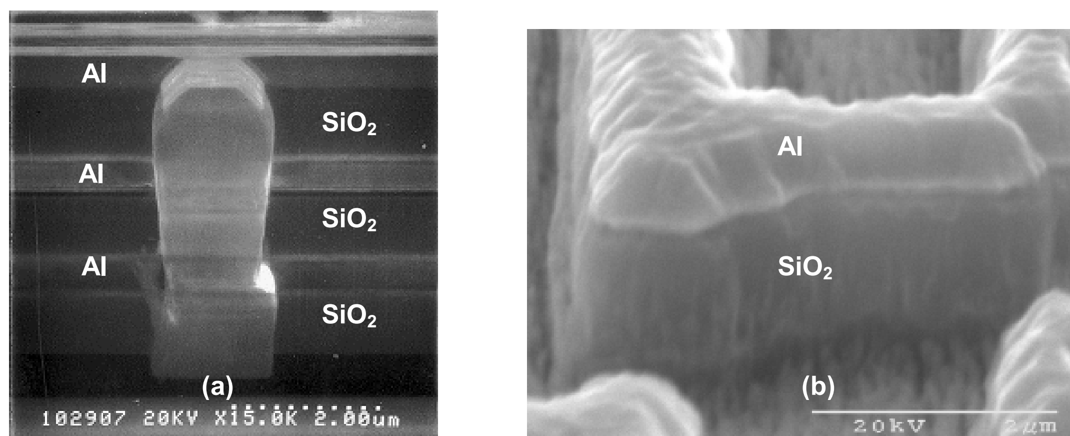

Figure 2. Cross section comparison of CMOS-MEMS and M-CMOS microstructures. (a) Three metal film stack from a MOSIS *Agilent* 0.5 micron CMOS process. (b) One metal film stack of a M-CMOS microstructure before release.

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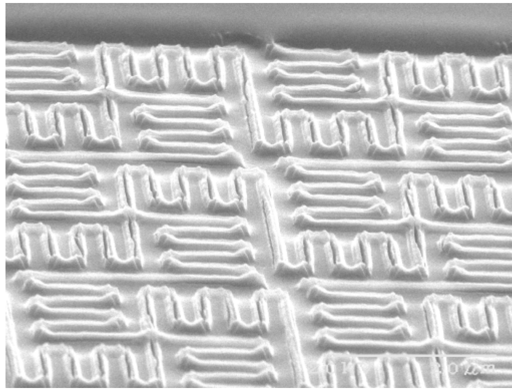
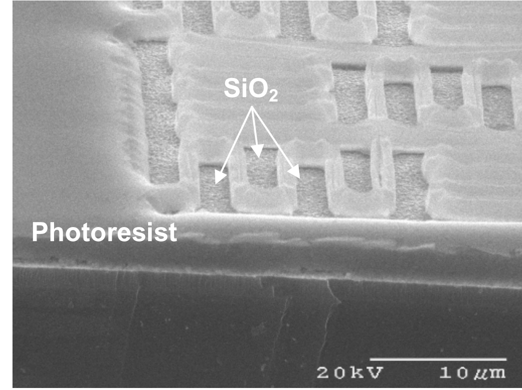




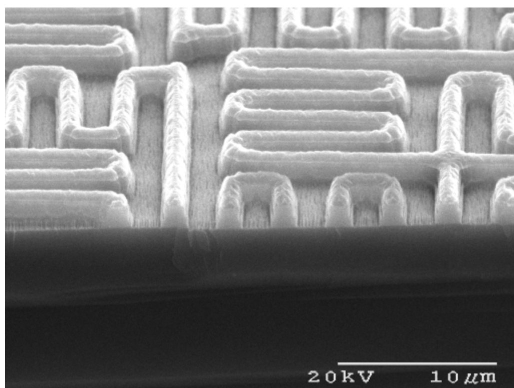
(a) **(b)**

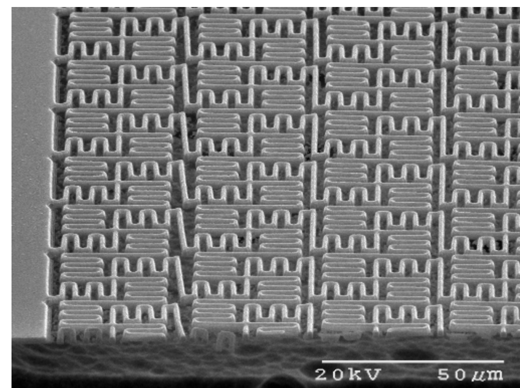
Figure 3. Micrograph showing the M-CMOS wafer (a) after aluminum etching with a pre-mixed commercial etchant and (b) after titanium tungsten etching with hydrogen peroxide.

The photoresist is spun at 4000 RPM for 30 seconds with an initial 6 second spread at 500 RPM. The softbake is conducted at 110°C on a hotplate for 90 seconds. After wafer cooling, the resist is exposed for a total dose of 75 mJ/s^2. Development is performed for 1 minute using a 1:1 mixture of deionized water and *Shipley* Microposit Developer (a special developer that does not etch aluminum).

A subsequent dry or wet etch removes the aluminum and titanium tungsten films. In this specific case, a commercial wet aluminum etchant and hydrogen peroxide solution were used to remove the aluminum and titanium tungsten films, respectively. The aluminum etchant used was Type A Pre-mixed Aluminum Etchant provided by *Transene Corporation*. The etchant is composed of phosphoric, acetic and nitric acid mixture along with a small part of deionized water. Any commercial hydrogen peroxide solution will perform the titanium tungsten etch. Both etches were performed at 45-50°C liquid temperatures to accelerate the etching (hot plate settings were at 70°C). The advertised etch rate for the pre-mixed aluminum etchant at the stated temperature is 100 Å/s, while the titanium tungsten etchant has an etch rate of 20 Å/s (as determined from visual inspection). The wafer was kept in the aluminum etchant for 40 seconds then rinsed in deionized water before being placed in the titanium tungsten etchant for 80 seconds. Figure 3a shows a micrograph after the wet aluminum etch, while Figure 3b shows a micrograph after the titanium tungsten etch using hydrogen peroxide.

After the metal layers are patterned, the aluminum film is used as an etch-resistant mask during the subsequent etching that creates the microstructures (the photoresist layer, which was used as a mask for etching the metal layers, erodes during subsequent plasma processing). Silicon dioxide areas not covered by metal are anisotropically etched to create vertical sidewalls using a trifluoromethane (CHF_3) and oxygen reactive ion etch (RIE) performed in a *Plasma Therm* 790 RIE system. The parameters used are 22.5 sccm flow of CHF3 mixed with a 5 sccm flow of O2, 100W power, 125 mTorr chamber pressure, for a 60 minute time interval. Figure 4a is a micrograph of a M-CMOS wafer after a 30 minute silicon dioxide etch. An





(a) **(b)**

Figure 4. (a) Micrograph after performing anisotropic silicon dioxide etch using CHF3/O2 reactive ion etch for 30 minutes, (b) Micrograph after performing isotropic silicon etch using xenon difluoride for 15 minutes. Depth of 10 microns approx.

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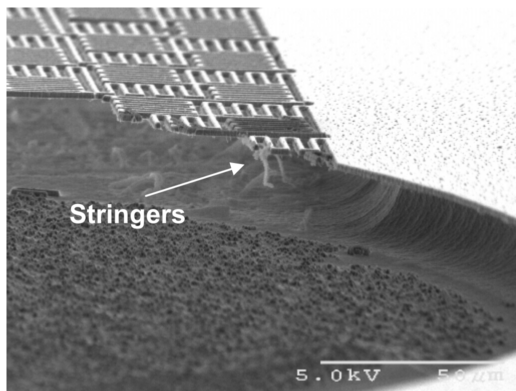
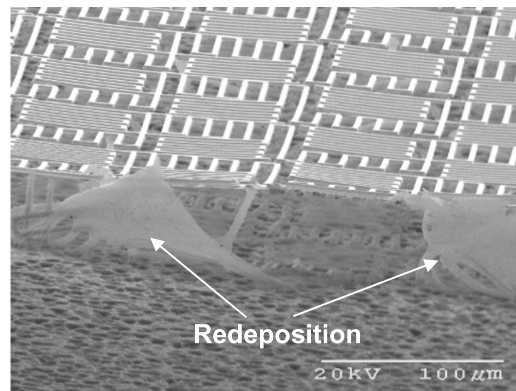




(a) (b)

Figure 5. Micrographs illustrating the aluminum redeposition problem. (a) Stringers can be seen under the suspended microstructure. (b) Large patches of a polymer-like film were seen in-between and under microstructures.

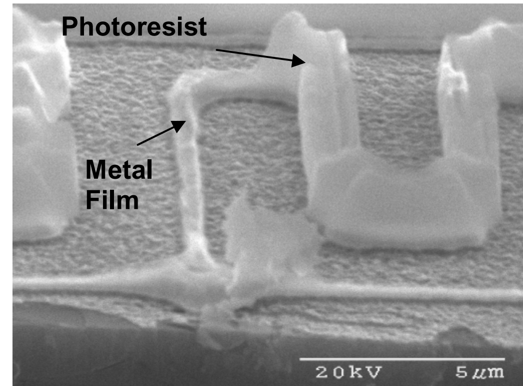
advantage of using trifluoromethane (CHF3) to etch the silicon dioxide layer is the formation of a thin polymer passivation layer on the vertical sidewalls that deposits during the oxide etching. This prevents electrical shorting during in-plane actuation of microstructures.

A final silicon etch, using xenon difluoride or any other silicon etchant, releases the microstructure. To reduce the amount of exposure time to plasma processing, XeF_2 is the preferred etchant for the M-CMOS process since it is very selective to silicon and is a dry release etch [6]. The xenon difluoride etch is performed on a *XACTIX* Xetch Xenon Difluoride Etch System [7]. The parameters used for the etch are 3 Torr XeF_2 pressure, 0 Torr N_2 pressure, 15 pulses with each pulse time being 60 seconds (15 minute total etch time). Figure 4b is a micrograph showing the released microstructure after the silicon etch.

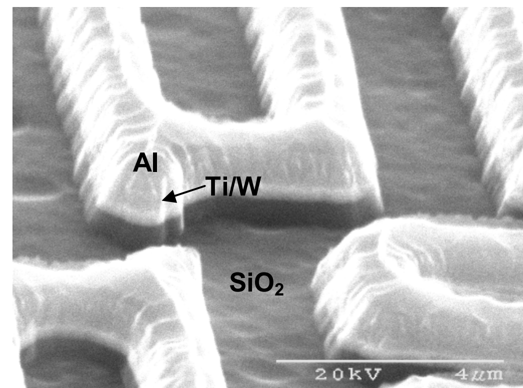
PROCESS REFINEMENT

Minor adjustments were needed throughout the fabrication sequence until a fully functional device was created. One of the major problems involves performing full wafer processing instead of individual die processing, as is done with CMOS-MEMS dies. All of the material etching processes discussed (aluminum, titanium tungsten, silicon dioxide and silicon) are dependent on the amount of material exposed to the etching species. This is often referred to as the "loading effect" and is especially apparent in plasma etching processes. To alleviate this problem, a full wafer was diced into smaller samples before reactive ion etching of the oxide film and subsequent silicon etching using xenon difluoride. This dicing process can lead to particulate accumulation on samples, which may cause occluding during etching processes.

A significant problem during the reactive ion etching of silicon dioxide was the resputtering of aluminum onto the entire wafer. Aluminum has a low sputter energy therefore it can be easily redeposited when exposed to high energy ions, as in a reactive ion etch plasma cloud. Figure 5a shows small stringers that are dangling below the released microstructure while Figure 5b shows the large patches of a polymer-like film forming in the gaps between the microstructure. This film has been analyzed by a fellow researcher using energy dispersive



(a)



(b)

Figure 6. Comparison between wet etching and ion milling of metal layers (a) Resist layer is significantly degraded after wet chemical etchants. (b) The ion beam mill provides a cleaner profiler without a reduction in width.

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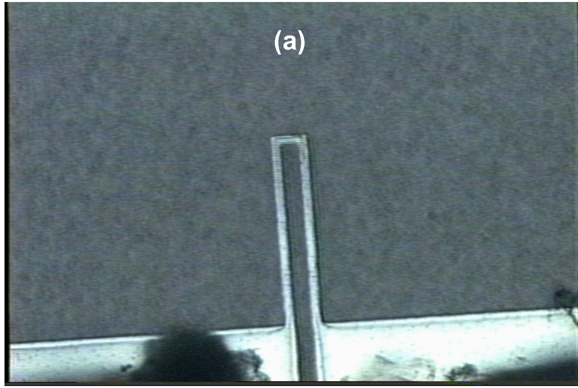


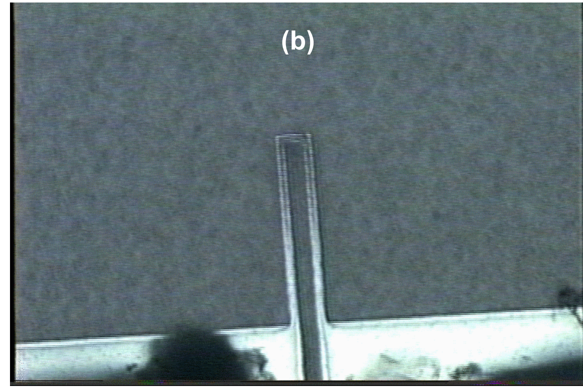


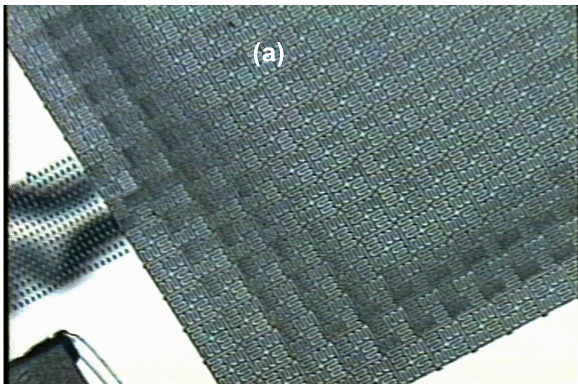
Figure 7. Micrograph of an out-of-plane thermal actuator (two cantilever beams joined at the end). (a) The actuator without any current flow. (b) After a 20 mA current is applied. The out-of-plane motion is demonstrated with a loss of surface reflectivity from the aluminum surface. Device Courtesy S. Zadeh

X-ray diffraction (EDX) and determined to contain aluminum, carbon and fluorine. To prevent this problem, the photoresist layer, that remains after metal patterning, was used to shield the aluminum from this plasma energy. Unfortunately the photoresist erodes during the ion bombardment but can be made to withstand this erosion by reducing the oxygen flow rate during the oxide RIE from the typical 16 sccm used in the CMOS-MEMS process to 5 sccm. In addition, by hard baking the photoresist layer, the resist forms a tough layer that makes it more difficult for oxygen to remove. Attempts were made to spin-on a thicker photoresist layer that could withstand longer plasma processing and protect the aluminum film. *Shipley* S1813 can be spun at 1000 RPM to create a ~2.5-3 μm thick photoresist layer. Softbake was done for 90 seconds at 115°C while exposure dose was 225 mJ/s^2. The thicker resist may cause difficulties in resolving fine features.

Wet etching of thin films, as during the metal layer patterning, has certain undesirable properties. The main problem lies in the isotropic nature of the wet etchant which will cause undercutting of the mask layer by the same distance as the etch depth. Numerous features in our design mask have minimum feature size widths of 1.6 μm, therefore the timed wet etch must be precise in its definition or the feature will be lost. A dry reactive ion etch can perform an anisotropic etch with no mask undercutting. The resources for a dry reactive ion etch of the metal films were not available, but the availability of an ion beam mill allowed an anisotropic profile. An ion beam mill works by physically bombarding the surface with high energy ions to etch films instead of using a chemical reaction, as reactive ion etching does. Figure 6 provides a comparison between a wet etched microstructure and an ion milled microstructure.

RESULTS

Devices successfully created include surface-normal and in-plane electrostatic and thermal actuators, the majority of which were designed by forty students in an Introduction to MEMS course in Fall 2001 at Carnegie Mellon University. Thermal actuators were created by running a small current through a finite width metal loop which acted as a small resistor, Eagle et al. used this actuation for probe tip actuation in the CMOS-MEMS process [8]. The loop is basically two cantilever beams joined at their end. Figure 7a and 7b demonstrates an out-of-plane thermal actuator before and after



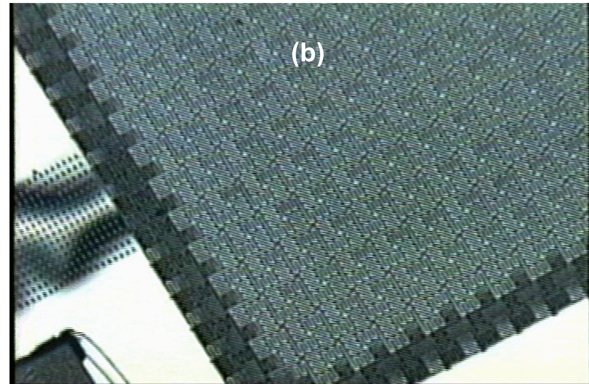


Figure 8. Micrograph of an out-of-plane electrostatic actuator based on a large suspended membrane. (a) The actuator without any voltage bias. (b) After a 30 Volt DC bias is applied. The out-of-plane motion is demonstrated with a loss of surface reflectivity from the aluminum surface on the outer membrane fringes.

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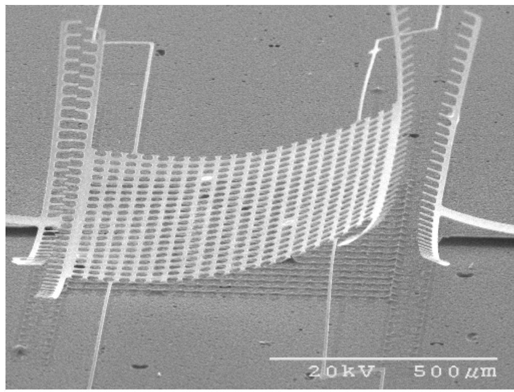

(a)

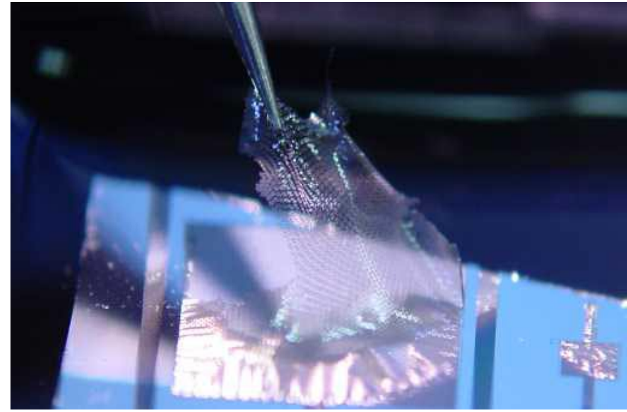

Figure 9. (a) Micrograph showing the large residual stress gradient apparent in the multilayer resonator. (b) Optical photograph of tweezers pulling a 8mm wide square membrane.

passing 20 mA of current, respectively. The out-of-plane motion is demonstrated with a loss of surface reflectivity from the aluminum surface. As this resistor heated up, the loop curled out-of-plane from the silicon wafer. After the current was turned off, the loop immediately cooled and dropped to its original position due to the low thermal mass of the structure. It is possible to create lateral movement thermal structures by having a different width around the loop; one of the cantilevers would have a larger width than the other.

Electrostatic actuators were demonstrated by creating a large flexible membrane based on a design by Neumann et al. [9]. The serpentine structure of the membrane allows the membrane to flex and touch the silicon substrate, the silicon dioxide layer underneath the metal provides insulation preventing any electrical shorting. Figure 8a and 8b shows the membrane before and after actuation with a 30 Volt DC bias. The short xenon difluoride etch allowed the creation of a small gap below the suspended membrane (approximately 15 μm), thus allowing for a minimal actuation voltage.

The temperature dependent residual stress gradients that cause CMOS-MEMS microstructures to curl was successfully recreated using the M-CMOS process as evidenced in Figure. Stresses in each of the three films deposited are temperature dependent, this is caused by the differences in thermal coefficient of expansion for each layer [10]. This problem was analyzed by Lakdawala et al. with the development of modeling tools to better predict when multilayer microstructures will curl.

EDUCATIONAL TOOL

To provide students at Carnegie Mellon University (CMU) with hands-on exposure to microfabrication, the M-CMOS process was incorporated into a 15-week semester course titled Introduction to Microelectromechanical Systems. Currently, there are very few one-term, student design, hands-on MEMS courses offered throughout universities. The primary constraint on one-term design courses is the lack of suitable facilities for microfabrication open to relatively inexperienced users. Although CMU's fabrication facility houses various semiconductor processing equipment, the ability to perform certain deposition and etching procedures is limited. For example, ideal circumstances would allow the metal etch to be performed using a reactive ion etch system with appropriate gases (Cl_2, BCl_3, etc.).

Using foundry services such as MUMPs (Multi-User MEMS Process) by Cronos Inc., North Carolina, provides an inadequate fit for the semester schedule [11]. MUMPs takes approximately ten weeks to finish the manufacturing process, which starts at certain pre-determined dates throughout the year. In addition, the release of polysilicon micromachining requires the use of hydrofluoric acid, thus creating a significant safety risk when used by inexperienced students.

Since the fabrication process is divided into one lithography and four etching steps, students can perform a single step during one week of the semester. Students were provided with design rules, given a 1cm x 1cm region of the wafer as their project area, and allowed two weeks to complete their designs. A chrome mask was then manufactured by an outside vendor that contained all of the student's designs. The last two to three weeks of the semester was used to test their devices using characterization equipment such as probe stations.

FUTURE WORK

Future work involves using test structures to measure the effective Young's modulus and residual stress of these metal and oxide microstructures [12]. The effective Young's modulus is determined by optically measuring the lateral resonance frequency of simple cantilever beams. Residual stress will be measured using bent-beam strain sensors [13]. In addition, vertical stress gradient will be measured by measuring the out-of-plane radius of curvature for various length beams. We also plan to develop a set of design rules to help designers during layout of various dimension microstructures.

CONCLUSION

The M-CMOS process was presented as a fabrication process that allows a quick design-to-device turnaround using only lithographic and etching equipment. Electrostatic and thermal microstructures were created using a simple metal and oxide film stack over a silicon wafer. Using the top metal layer as an etch mask, the M-CMOS process follows equivalent fabrication steps to Carnegie Mellon's CMOS-MEMS process while allowing a larger real estate and cheaper cost. This paper

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discussed some of the process refinements that were necessary to achieve successful device operation. Some of the devices successfully created include out-of-plane electrostatic membranes and curling thermal actuators, the majority of which were designed by forty students in an Introduction to MEMS course in Fall 2001 at Carnegie Mellon University. Future work will involve characterizing M-CMOS microstructures as well as developing a set of design rules.

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