

Design and Optimization of Compact Microscale Electrophoretic Separation Systems

Anton J. Pfeiffer,[†] Tamal Mukherjee,[‡] and Steinar Hauan^{*†}

Departments of Chemical Engineering and Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, Pennsylvania 15213-3890

The ability to manipulate and synthesize chemical species on microchip devices provides access to a new and exciting field. These technologies have several advantages throughout the industrial and scientific communities, especially in the emerging areas of biomedical engineering and the life sciences. Recent advances in microscale mixing, reaction, separation, and fluid handling have opened new areas in which process systems engineering techniques can be applied. Here we discuss our initial efforts at creating automatic synthesis methods for the design of microchip-based electrophoretic separation systems that occupy minimal areas. We use piecewise algebraic and logic models to compare the conflicting design goals of maximum system performance and minimum device area. We have implemented both heuristic and numerical optimization design techniques. The long-term goal of our work is the development of methodologies for the design of complete lab-on-a-chip devices.

1. Introduction

The ability to fabricate complex microscale devices precisely and efficiently has grown enormously during the past half century. Advances in integrated circuit (IC) technology starting in the 1950s have provided the capability to batch fabricate microchip devices quickly and inexpensively. IC fabrication capabilities became an enabling technology for the development of microelectromechanical systems (MEMS) in the 1980s.¹ Advances in MEMS technology allowed for the eventual development of chip-based microfluidic and microchemical systems in the early 1990s.²

MEMS technology is now common¹ in commercial devices ranging from pressure and inertial sensors to ink-jet printheads. MEMS research has also been used to develop fluid- and heat-transport devices in the microscale. Designs are also available for microscale pumps, valves, and heat exchange devices.^{2–4} These devices represent some of the important auxiliary equipment needed for chemical processing on a microchip.

The microscale domain is starting to become sufficiently advanced for the effective application of process system engineering (PSE) techniques for the design, synthesis, and optimization of microscale chemical devices. Practical designs for microscale unit processes such as mixing, reaction, and separation⁵ exist in the literature. These designs were created only after many man-hours of experimentation and analysis. Currently, no formal methods exist for the design of microscale chemical systems. Our goal is to develop design methodologies using concepts taken from PSE, very-large-scale integration (VLSI) approaches, and computational geometry to produce accurate working designs in far less time than conventional methods allow.

1.1. Motivation. The main benefits of miniaturization⁶ are portability, reduced cost, automation, reagent

economy, high speed, and efficiency. Researchers have attempted to reap these benefits in the areas of chemical production, sensing, and analysis.

Microscale devices for chemical production are an attractive option whenever small quantities of specialty materials must be produced or highly degradable materials must be produced on demand.⁷ This technology has a great deal of potential in the pharmaceutical and biomedical fields for specific applications in which device size, product purity, and efficiency are critical factors. Microscale devices that can be implanted within the human body to perform specific tasks, such as microdialysis, represent an exciting application of this technology.^{8,9} Although it is unlikely that microscale chemical devices will be used for bulk chemical production,⁶ these devices do have a place in the traditional chemical industries for applications in quality control, high-speed analysis, and specialty production.

Microscale devices for chemical sensing and detection have a number of attractive qualities. The portability and disposable nature of these devices make them ideally suited for applications ranging from personal chemical and biological weapons detection to at-home medical diagnostics tools.^{10,11} Noninvasive devices for blood glucose monitoring are currently commercially available.¹² Mass-production capabilities reduce device costs and complexity and allow for single-use applications.

Microscale chemical devices have had an impact in the fields of analytical chemistry and the life sciences. Massively parallel, high-throughput microdevices are currently used in the fields of genomics and proteomics^{13,14} and have contributed to the realization of such daunting tasks as the mapping of the human genome. As scientific knowledge in these areas grows, there is an increasing demand for more efficient, highly automated analytical devices.

However, the design of microscale chemical devices is complicated by a number of interesting problems. These problems arise because of nonstandard operating regimes, new materials, intricate fabrication techniques, and complex device geometries.¹⁵ The interconnectivity

* To whom correspondence should be addressed. Tel.: (412) 268-4393. Fax: (412) 268-7139. E-mail: hauan@cmu.edu.

[†] Department of Chemical Engineering.

[‡] Department of Electrical and Computer Engineering.

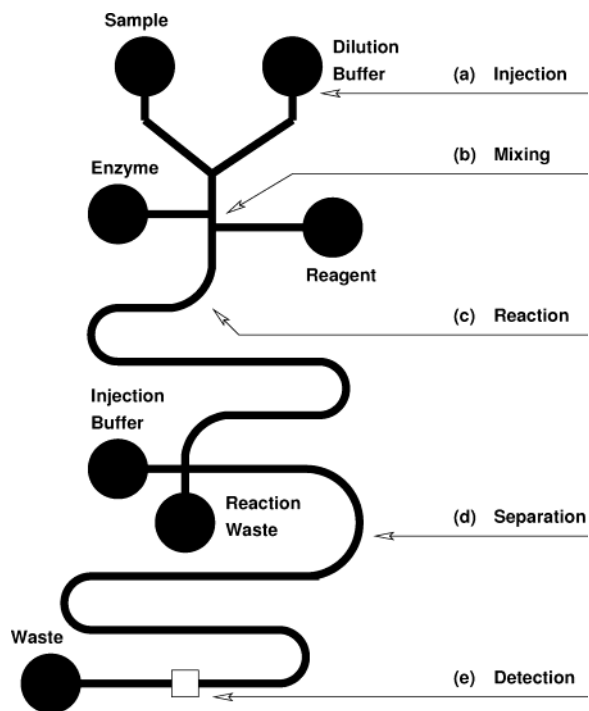


Figure 1. Canonical lab on a chip.

and placement of processing components on the chip become increasingly important as device size decreases.¹⁶ Research in microscale chemical devices includes a broad and varied range of topics. We have narrowed our focus to the creation of methodologies for the design of microscale analytical devices. In particular, we examine a subset of these devices known as “labs on a chip” (LoC) or “micro total analysis systems” (μ -TAS).

1.2. Lab on a Chip. The LoC approach is an area of microtechnology that is currently receiving a great deal of interest in the chemistry and life-science communities.^{17,13} This approach can be thought of as the integration and miniaturization of a complete analytical chemistry laboratory onto a single microchip.

Figure 1 shows our concept of a canonical lab on a chip. At a, chemical species are injected into the chip. This is typically accomplished by pressure-driven or electrokinetic flow. In region b, mixing of reagents takes place, typically induced by phenomena such as diffusion, convection, or electrokinetic instabilities.¹⁸ Following mixing, the mixture of reagents and injected chemical species passes through the reactor section (c) of the chip. Typical on-chip reactions are polymerase chain reaction (PCR)¹⁹ and molecular tagging by fluorescent or radioactive markers.²⁰ In region d, the species of interest are separated by techniques such as high-performance liquid chromatography (HPLC) or electrophoresis. Species detection takes place at e. Detection is typically performed either on-line or off-line²¹ using optical techniques such as laser-induced fluorescence (LIF) or electrochemical techniques such as amperometry or potentiometry.

Currently, a substantial research effort is being conducted in the area of separation on a microchip. Microchip-based separation and detection systems have immediate applicability for use in DNA and protein mapping, cell identification, and other bio-molecule sensing and quantification applications.²² A broad range of separation techniques have been effectively miniatur-

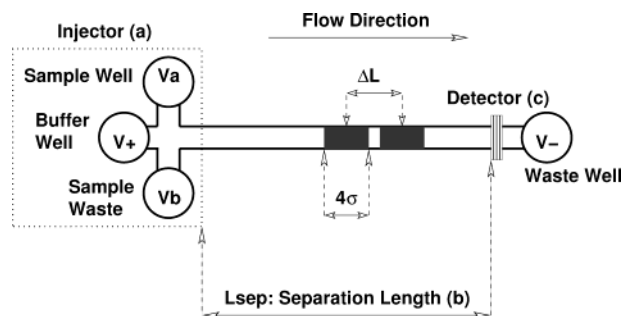


Figure 2. Simple chip-based CE schematic.

ized, including HPLC, micellar electrokinetic chromatography (MEKC), free-flow capillary zone electrophoresis (CE), and isotachopheresis.²³ Among these techniques, CE has received significant attention because of its broad range of applicability and relative simplicity.²⁴

We have developed methodologies for the optimal design of microchip-based CE systems. These methodologies illustrate some of the important issues and challenges inherent in complete LoC system design. Herein, we present our current design methodologies and then discuss extensions to these methods that will enable the design of complete LoC systems.

1.3. Principles of Microchip-Based CE. Figure 2 illustrates the major components of a typical chip-based capillary electrophoretic separation system. The chip is composed of (a) an injector where the analyte (mixture to be separated) is injected into (b) the separation channel. Although traveling along the separation channel, the analyte has time to separate into individual species bands. Finally, in (c) the detector, the species bands are identified. Electrodes are positioned in the four wells and their voltages are manipulated to produce a desired separation speed and species travel direction.

In electrophoretic separation systems, a voltage is applied along the separation channel in order to produce an electric field within the stationary liquid phase or background electrolyte (BGE). The electric field causes the charged species within the analyte to move with a particular velocity toward either the positive or negative electrode. The carrier fluid within the channel is known as the background electrolyte or buffer solution. The electrophoretic mobility of species i , μ_i^{ep} , along with the electric field strength, E , determines the species' velocity ($\mu_i^{\text{ep}} E = U$).²⁵ Although not the only factor determining ease of separation, the larger the difference in mobility between species in a mixture, the more readily the species can be separated. Electroosmosis, which refers to the bulk flow of the BGE in response to an applied electric field, often accompanies electrophoresis. Electroosmosis will alter the velocities of various species during separation, and for this reason, it cannot be neglected.^{26,27} The change in mobility due to electroosmosis is most often dealt with by determining an apparent mobility, $\mu_i^{\text{a}} = \mu_i^{\text{ep}} + \mu^{\text{eo}}$, where the apparent mobility is the sum of the species' electrophoretic mobility, μ_i^{ep} , and the electroosmotic mobility, μ^{eo} .²⁸

As a species band travels down the separation channel, it broadens (or disperses) as a result of a number of different phenomena. The main causes of dispersion in microscale electrophoretic systems are²⁹ diffusion, channel geometry, Joule heating, adsorption, and electromigration. Dispersion has the negative effect of smearing out species bands, thus impeding separation.

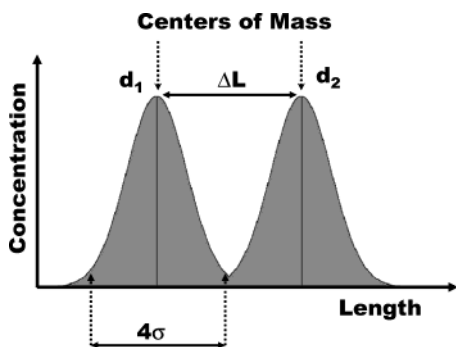


Figure 3. Two species bands represented as Gaussian distributions.

Also, because dispersion results in the dilution of the species band into the BGE, dispersion causes a reduction in species-band concentration. In the worst case, band dispersion can result in species concentrations that are below the detection limit of a particular detector. However, electrokinetic flow has a distinct advantage over pressure-driven flow when it comes to dispersion. A dispersive phenomena known as Taylor dispersion, which results from parabolic velocity profiles, is typically insignificant in electrokinetic flow in microchannels, which have largely flat velocity profiles.^{30,31}

1.4. CE Performance Metrics. Resolution (R) is an important design specification for CE separation systems. Maintenance of the appropriate resolution helps to ensure that species bands will be separated sufficiently far apart to be effectively detected. Conceptually, resolution can be defined as the ratio of the distance between two adjacent bands to some function of the band dispersion. Resolution has been mathematically defined in many ways;^{25,28,32–35} here we define it as Giddings does

$$R = \frac{(d_2 - d_1)}{4\sigma_{\text{avg}}} \quad (1)$$

The distance between adjacent bands ($d_2 - d_1$) is measured with respect to the centers of mass of the concentration distributions of the two bands (Figure 3). The dispersion is quantified as 4 times the average standard deviation of the two bands. Most often, species bands are approximated as Gaussian distributions. Four times the standard deviation of a Gaussian distribution captures 95.6% of the mass within the band. A typical desirable resolution value is 1.5, which corresponds to baseline resolution.²⁵

Equation 1 can potentially break down for two extreme conditions. The first case occurs when only single components of a separation system are to be optimized without consideration of additional dispersion sources such as injectors or detectors. Neglecting these dispersion sources has the potential of leading to designs that are unrealistically short. To prevent this, we require that the peaks of adjacent bands maintain at least a certain separation distance, ΔL , which is defined by the detection scheme applied.

Another issue arises when very long separation channels are employed to increase the resolution for difficult separations. It is possible that, by the time the species bands reach the detector, dispersion might have reduced the concentration of the bands below the lower detection threshold of the detector. Thus, even though the desired resolution might have been attained, the species are

undetectable. At present, we are able to simulate changes in peak concentration; however, concentration tracking has not yet been fully integrated into our design algorithms.

Two additional historical performance metrics for capillary electrophoresis are²⁸ plate height

$$\left(H = \frac{\sigma_i^2}{L_{\text{sep}}} \right)$$

and plate number

$$\left(N = \frac{L_{\text{sep}}^2}{\sigma_i^2} \right)$$

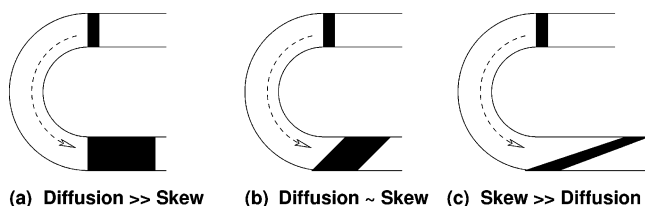
Plate height, H , is the ratio of an analyte band's variance, σ_i^2 , to the total separation length, L_{sep} , and represents the amount of dispersion that has occurred for a given separation length. In diffusion-dominated regimes, plate number, N , is proportional to the square of resolution. Unlike resolution, plate height has only intuitive physical meaning,²⁵ and plate number is ambiguous as a measure of separation efficiency³⁴ in continuous separation systems such as CE and HPLC. These metrics have been inherited from earlier work done using equilibrium-stage separations. However, they do provide a means of comparing different separation systems. In general, lower plate heights and higher plate numbers are preferable. CE systems on microchips have been shown to produce plate numbers greater than 1×10^6 .³⁶ Several other performance metrics have been suggested that incorporate plate number, plate height, or resolution and some other characteristic of the design such as time,³⁷ voltage,²⁸ or detector signal-to-noise ratio.³⁴

An objective that is not explicitly considered in either traditional or microchip-based CE design is the minimization of device area. We believe that this objective is important because it allows for the design of devices that have increased functionality per unit size, novel configurations and applications, and reduced power consumption. However, increasing separation performance and reducing device area represent conflicting goals. In our methods, we search for the minimum area design that satisfies a set of performance specifications and fabrication constraints.

1.5. Channels on Microchips. When an increase in resolution for macroscale CE columns is desired, a typical approach is simply to increase the channel length. However, adding channel length conflicts with the design goal of generating compact systems. Consequently, LoC systems employ turns to reduce the area needed to carry out a particular separation.

The introduction of turns into LoC designs leads to a phenomenon known as turn-induced dispersion.^{38–42} Turn-induced dispersion has the potential to diminish or eliminate any performance gains that would have occurred as a result of the increase in channel length. Channel geometry, channel topology¹⁶ or interconnectivity, and fluid flow regime play important roles in the performance of separation systems containing turns.

When a species band travels around a turn, the analyte particles on the inside of the turn travel more quickly than the particles on the outside of the turn. This is because particles on the inside of a turn have a shorter distance to travel and experience a larger



(a) Diffusion >> Skew (b) Diffusion ~ Skew (c) Skew >> Diffusion

Figure 4. Three possible results for bands leaving turns.

(a) Serpentine Topology (b) Spiral Topology

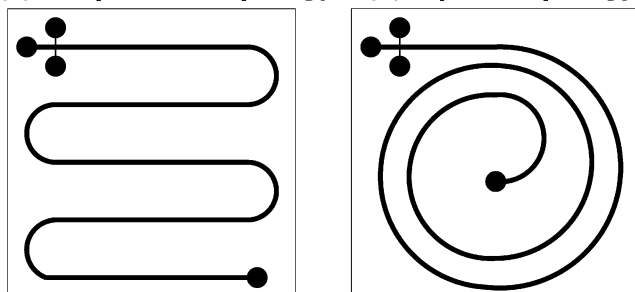


Figure 5. Serpentine and spiral topologies.

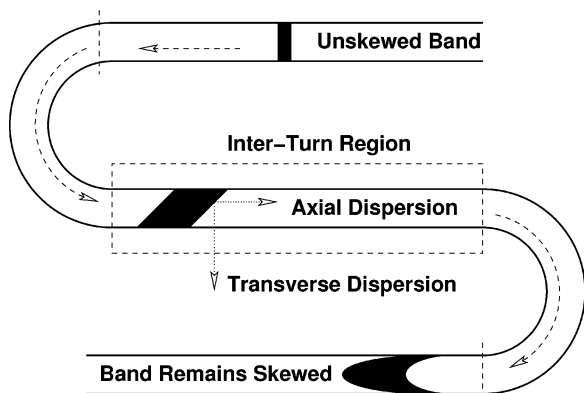


Figure 6. Complimentary turn pair schematic.

electric field than particles on the outside of the turn.⁴¹ When diffusion is the predominant source of dispersion, the band exiting the turn will appear similar to that depicted in Figure 4a. When diffusion is less predominant, the band exits the turn with a concentration distribution that is increasingly skewed (Figure 4b and c).⁴⁰

Two typical compact channel configurations^{36,42} are the *serpentine* and *spiral* channel topologies (Figure 5). In the case of the spiral topology, turn-induced dispersion continuously increases as the analyte band travels along the channel. Turn-induced dispersion in the serpentine topology is more complicated. Skewed bands exiting a turn travel through an inter-turn straight section (Figure 6) in which the band can smear out in both the axial and transverse directions. In the extreme case, the skewed band can diffuse into an elongated plug shape. In the serpentine configuration, it is possible for a downstream turn to mostly remove the skew caused by the upstream turn by rotating the band in the opposite direction (Figure 6).⁴¹ Skew canceling by complimentary turn pairs is especially noticeable when diffusion can be considered negligible. However, electric field effects within the turn will typically cause incomplete skew canceling⁴³ and can cause the exiting band to take on a parabolic concentration distribution.

Current analytical models for turn-induced dispersion^{39–41} provide an accurate description of the disper-

sion produced only when unskewed plug-shaped bands enter a turn. We have implemented highly accurate composable section models that are capable of capturing the dispersive effects of both plug-shaped and skewed bands entering turns. These models also capture the dispersive effects of skewed bands within the inter-turn straight section.^{44,45} Flexible composable models of this nature allow for fast and accurate simulation of a large range of operating conditions and system configurations.

It is tedious and often impossible to determine, a priori, the operating conditions, channel geometry, and system topology that will yield a minimum area design. For a large and often poorly defined design space, significant tradeoffs exist between channel geometry, topology, system performance, and device area. Models capable of capturing the effects of these tradeoffs over a large range of design scenarios are important.

2. Design Problem

Currently, three common approaches are employed for the design of microelectrophoretic systems: laboratory experimentation,³⁸ analytical solution of the governing partial differential equations,^{39,40} and numerical simulation,^{46–48} as well as combinations of the above techniques.^{41,49} However, iterative design of even relatively simple layouts using laboratory experiments or numerical simulations can take weeks or months. Analytical solutions to PDE models are typically specific to a single geometric structure and set of initial conditions and generally cannot be extended outside of this domain.

There has been some recent interest in developing shortcut methods for microchannel system design. A practical approach has been proposed by Griffiths and Nilson⁵⁰ based on their analytical expression for dispersion in turns.³⁹ In their approach, turn sections are designed to produce at most an order of magnitude less dispersion than an associated upstream or downstream straight channel section. Although practical for some flow regimes, their method does not account for differences in dispersion within inter-turn straight channel sections and does not apply for skewed bands entering turns, thus neglecting important parts of the design space. Another interesting approach has been proposed by Fiechtner and Cummings⁵¹ in which faceted designs rather than turns are used to redirect microchannel flow. However, the authors make a point of the fact that they have not yet incorporated diffusion effects into their models. It is likely that transverse diffusion effects within a faceted channel design will degrade performance for all but the lowest diffusivity regimes.

Some recent work has also focused on creating designs that use constricted or *tapered* turns^{38,40} for the purpose of reducing turn-induced dispersion. Although models for constricted turns could be incorporated into our methods, we currently do not consider them because of the large number of commercial and academic designs that do not include them. Constricted turns cause an increase in fabrication complexity and a consequent increase in fabrication cost.

We have overcome the issues of time and flexibility by implementing a collection of highly accurate reduced-order component models.⁴⁴ These models appear both computationally fast and sufficiently general to allow complex topologies to be constructed. They accurately capture the diffusion-based and turn-induced dispersive effects experienced by species bands as they travel

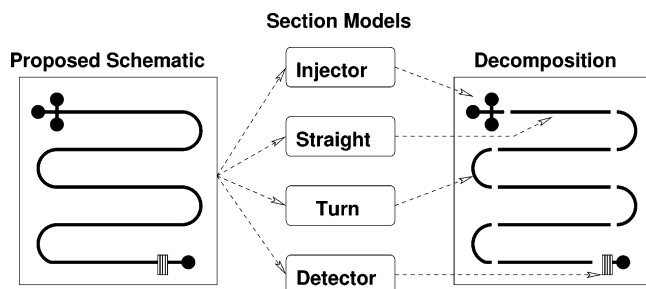


Figure 7. Decomposition of channel system.

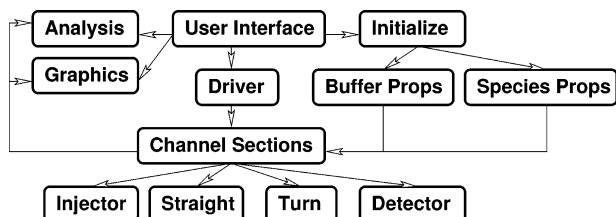


Figure 8. System simulator architecture.

through system topologies containing both turns and straight channel sections. When compared to finite-element simulations, the variance calculated by these models has a worst-case relative error of less than 10% for all flow regimes except the high pure-advection flow regime.⁴⁴

Our design approach has three fundamental components: (1) a microelectrophoretic system simulator capable of simulating proposed designs in seconds; (2) rigorous area constraints and heuristic channel packing and placement algorithms (CPP); and (3) tailored design optimization methods that utilize the system simulator, CPP algorithms, numerical optimization, and area constraints.

2.1. System Simulator. The interactions between channel geometry, topology, and system performance require an efficient and physically accurate means of evaluating alternative designs. We have done this through the creation of a simulation engine for chip-based electrophoretic separation systems. The simulation engine can be used to quickly evaluate a specific channel topology with given operating conditions and species physical properties.

The main idea behind the simulation engine is one of decomposition, as schematically outlined in Figure 7. We assume that any channel system can be decomposed into a set of component pieces or sections. Each of these sections is described by an algebraic model combined with logic that captures how bands travel and disperse within that section. The phenomenological models used are highly accurate algebraic reduced-order component models.⁴⁴ At present, we divide channel systems into straight sections, turns, injectors, and detectors.

Figure 8 shows a representation of the simulator architecture. This architecture is independent of the underlying section models. As new and improved section models are developed, they can be readily integrated into this framework. Given all necessary section models, we believe that any electrophoretic channel system can be simulated by piecing the channel sections together to produce the desired channel topology. The modular nature of the simulator allows it to be used for either interactive design simulation or iterative use within a synthesis tool. Figure 9 represents the input/output diagram of a generic channel section.

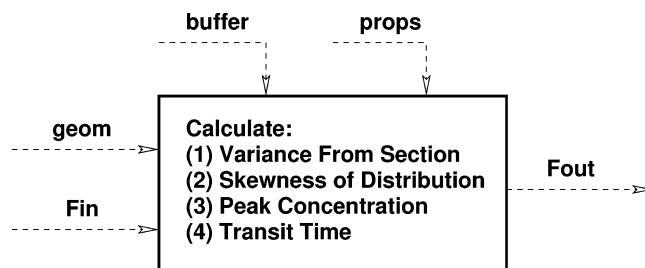


Figure 9. Generic channel section model.

Table 1. Typical Constraints and Their Numerical Values

performance	operating	physical
$N \geq 10^4$	$R \geq 1.5$	$w \in [10, 100] \mu\text{m}$
$H \leq 10 \mu\text{m}$	$\Delta L \geq 10 \mu\text{m}$	$A \leq 25 \text{cm}^2$
$t \leq 2 \text{min}$	$V \leq 30 \text{kV}$	$E \leq 10 \text{kV/cm}$

The two streams, props and buffer, entering at the top are objects containing vectors of species properties and buffer properties. The props object contains species mobility and diffusivity data. The buffer object contains quantities such as buffer concentration and buffer thermal conductivity. The two objects entering through the side contain section-specific quantities. The geom object contains quantities such as channel width, length, and depth that describe the geometry for that particular channel section. The Fin object contains the variance, peak concentration, transit time, and skewness for each species from the previous section. The band skewness is quantified as a vector of Fourier series coefficients as described by Wang et al.⁴⁴ The object Fout leaving the section becomes the Fin object for the next section.

The simulator provides the ability to rapidly compare complex topologies. The simulator is capable of estimating and quantifying the impact of dispersion resulting from diffusion, geometry and Joule heating.⁵² Section models can be readily tested and compared. Any number or type of analytes and any specific buffer properties can be specified. Our current library of section models enables the construction of the majority of the system topologies found in the literature.

2.2. Design Constraints. We have approached the design of microelectrophoretic devices from two perspectives. Specifically, we wish to (1) determine the highest performance design that can fit within a given chip area and (2) minimize the area occupied by a design while maintaining device feasibility.

We have divided the constraints on the design problem into performance constraints, operating constraints, and physical constraints as summarized in Table 1. Performance constraints provide a lower bound on the effectiveness of the separation system (e.g., maximum allowable plate height or minimum allowable plate number). Operating constraints are dictated by external equipment such as available voltage sources or available detectors. Even if this equipment does not occupy physical space on a chip, it can have a significant impact on the final design. Physical constraints are those dictated by the phenomena taking place in the system, regions of model applicability, and fabrication limits. For instance, bounding the electric field strength prevents sparking between electrodes. Fabrication constraints capture manufacturing limits, two of the most important being the minimum channel width and the spacing between channels.

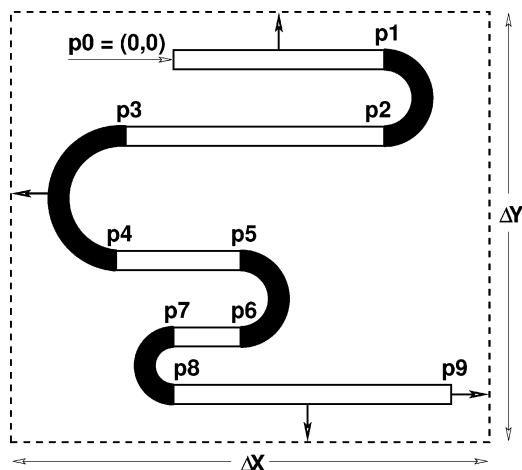


Figure 10. Determination of topology bounding box.

Device Area Connectivity and Overlap Constraints. Explicit constraints on the overall physical dimensions of a design are important when compact designs are being synthesized. The ordering and placement of channel sections is also critical to the success of the design. We have developed a method for determining the area occupied by a design and a method for enforcing proper connectivity of channel sections.

The area calculation is performed by assigning coordinates to the ends of each channel section. The beginning of the first channel section is given the coordinate point $p_0 = (0, 0)$ (Figure 10). The positions of subsequent points are all tracked with respect to this reference coordinate. Once the coordinates of all of the channel section end points are assigned, the set of possible chip edges is determined by adding channel spacing and half widths in the appropriate x and y directions. The set of points e_i represent the edge points calculated from the points p_i . The dimensions of the design are then calculated over the set of edge points, e_i , by eqs 2 and 3.

$$\Delta X = \max(x_i) - \min(x_i) \quad (2)$$

$$\Delta Y = \max(y_i) - \min(y_i) \quad (3)$$

The difference between the maximum and minimum edge coordinates gives the x and y dimensions of the design. The area for the bounding box of the design is given by $A = \Delta X \Delta Y$.

During synthesis, bounds can be set for ΔX and ΔY and designs that fit within the desired dimensions are generated automatically. Section lengths are not explicitly constrained. This results in a set of locally optimal channel lengths. The designs might not need to use the entire allocated area, and they are not required to maintain any kind of symmetry.

It is also necessary to enforce the condition that the outlet of any channel section must attach precisely and with a particular orientation to the following section. The coordinate end point of section k must correspond with the start of section $k + 1$. Channel sections that connect must be prevented from doubling back on each other (Figure 11a). This is accomplished by defining a flow direction vector in the direction of material flow. The flow direction leaving section k must equal the flow direction entering section $k + 1$ (Figure 11b).

Enforcing proper flow direction eliminates the possibility of channel sections doubling back on each other.

However, the problem of preventing geometric structure overlap^{53–55} in a general way remains unresolved, especially for large-scale systems and systems of unknown topology. We have developed sets of constraints specifically for these serpentine and spiral topologies to prevent channel section overlap. Ideally, we would like to prevent overlap in a general way regardless of the layout topology or type of channel section. The prevention of channel section overlap is an area of ongoing research.

2.3. Heuristic Channel Packing and Placement Algorithms. The channel packing and placement algorithms are geometry-based layout generation algorithms. These algorithms pack channel sections into a specified chip area. They were created to provide an expedient method of searching the design space for feasible designs. Currently, we have created two CPP algorithms: one for spiral topologies and one for serpentine topologies.

Designs generated by the CPP algorithms are calculated according to the chip dimensions, ΔX and ΔY ; the channel width, w ; the minimum turn ratio

$$TR = \frac{r}{w}$$

(where r is the centerline radius); and the channel spacing, PAD. The ΔX and ΔY values define the available chip area. The channel width, minimum turn ratio, and channel spacing constrain the total amount of channel length that can fit within the available area.

The heuristic rule employed by the CPP algorithms is that *good designs arise when the dispersion introduced by each individual section is minimized*. This leads to minimum-curvature turns and results in designs that use the entire allotted chip area. The CPP algorithms place channel sections as illustrated in Figure 12. For a given specified separation length and chip area, a minimum-curvature channel section is added. If the section does not provide the necessary length, another section is added. This procedure continues until the desired requirement on the separation length is satisfied. The variance produced by the topology is then estimated by adding the variance produced up to the final completed section to a linearly interpolated measure of the variance for the last section that is based on channel length.

Explicit use of the CPP algorithms for design most often result in suboptimal designs from the point of view of device area. However, the CPP algorithms have some important positive features:

(i) Fast Partial Enumeration. Many designs can be evaluated over both continuous design variables and integer sections (> 10 designs/second).

(ii) Show Tradeoffs between Various Constraints and Objectives. CPP algorithms can give an indication of Pareto-optimal conditions.

(iii) Conservative Estimate of the Feasible Region. Because the CPP algorithm fills the entire available design area, there is a tendency in some instances to overshoot the desired separation performance metric, but undershooting never occurs. Designs found with CPP algorithms are guaranteed to be feasible, although smaller designs might exist.

(iv) Determine Precise Lower Bounds on Possible Number of Channel Sections and Upper Bounds on Total Channel Length and Number of Sections. Because of the heuristic within the CPP

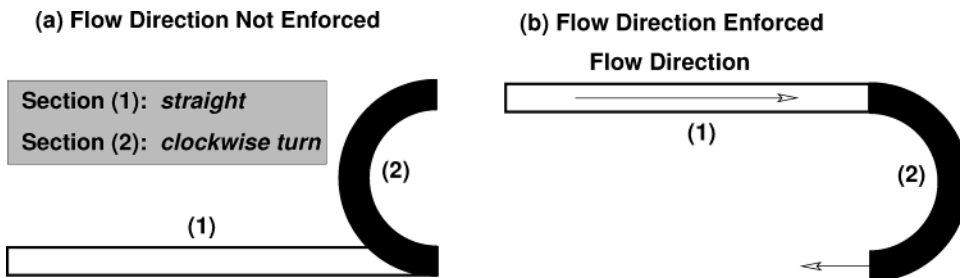


Figure 11. Overlap prevention from channels doubling back.

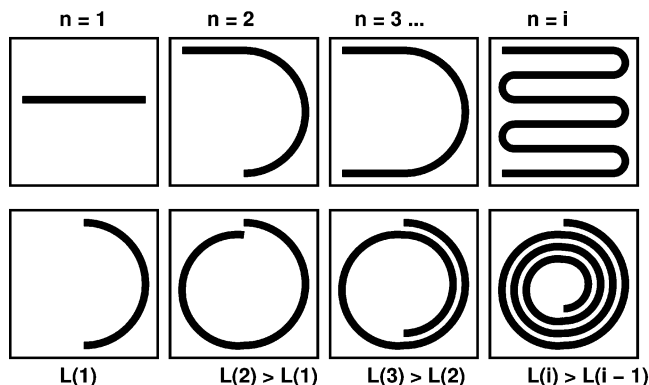


Figure 12. Channel packing procedure.

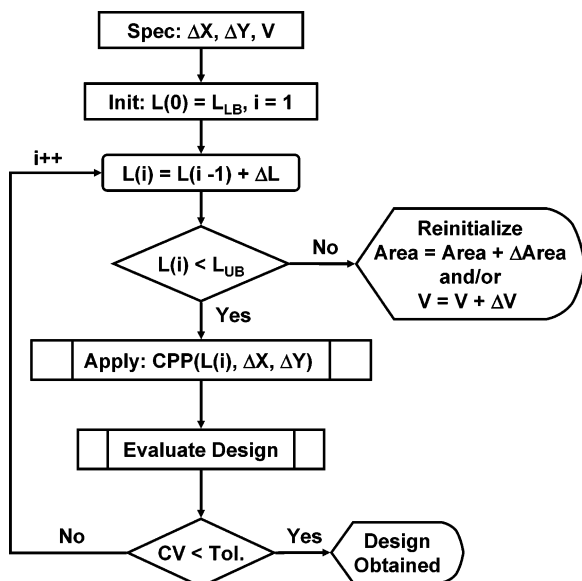


Figure 13. Length incrementation algorithm.

algorithms, a given length will automatically be fit into the fewest number of sections. As the channel length to be packed increases, the number of sections increases until no more sections can be added. This yields the upper bounds on channel length and number of sections.

2.4. Design Optimization Methods. We have developed design optimization methods for creating designs within fixed compact areas, as well as for creating designs that occupy minimal areas. Our algorithms are based on two fundamental techniques: (1) heuristic-based partial enumeration and (2) robust numerical optimization.

2.4.1. Length-Incrementation Heuristic Algorithm. In this algorithm, channel length is incrementally increased within a design area of fixed dimensions (Figure 13). The design dimensions, defined by ΔX and ΔY , and the voltage V are specified. The length is

initialized to L_{LB} (eq 4).⁵⁶ This quantity is calculated to satisfy the constraint on peak separation distance, ΔL . The peak separation distance is the minimum distance by which two adjacent bands must be separated to be detectable. This ensures that, if a feasible design is possible, the constraint on ΔL is always satisfied. Usually, we assume $\Delta L = 10 \mu\text{m}$.

$$L_{LB} = \Delta L \frac{\mu^*}{\min(\Delta\mu)} \quad (4)$$

In eq 4, $\min(\Delta\mu)$ is the smallest difference in mobilities for all of the chemical species in the simulation. The quantity μ^* is the larger of the two mobility values from $\min(\Delta\mu)$.

After the length is initialized, it is checked to make sure that it fits within the specified design area. This is accomplished by the CPP algorithm described in section 2.3. Given the total separation length, $L(i)$, and the design area dimensions, the CPP algorithm will generate the channel length and section type for each section within a particular topology. The design generated by the CPP algorithm is then simulated by the simulator. If the constraint violation, CV , is less than the tolerance, Tol , for resolution, electric field strength, and peak separation distance, then the design is accepted as feasible. If the design does not meet the constraints, an incremental amount of channel length is added to the previous channel length. The incremental length step size is usually set to the peak separation distance, ΔL ; however, this value can be increased if a faster (but coarser) solution is desired. Design iterations continue until either a design is found or no more channel length will fit within the specified area. If no design is feasible, the designer might wish to increase the available design area, the voltage or a combination of the two and run the search again.

Figure 14 shows an example result for serpentine design synthesis using the heuristic length-incrementation algorithm. The dashed line shows the performance of a single straight channel section and represents an upper bound on system performance. The solid line represents the solution path for the serpentine topology. The line spans serpentine designs from 1 to 25 sections. The line is jagged because of the discrete changes in topology that occur as sections are added to the serpentine design. The graph shows that the first feasible design occurs at approximately 12 sections. Finer gridding of the incremental length step size would give a more precise estimate.

The points marked by \times represent optimized designs obtained using the optimization methods described in sections 2.4.3–2.4.5. It should be noted that these methods give a much more precise indication of the first feasible design (11 sections), as well as the optimal operating voltage and the precise lengths of all sections.

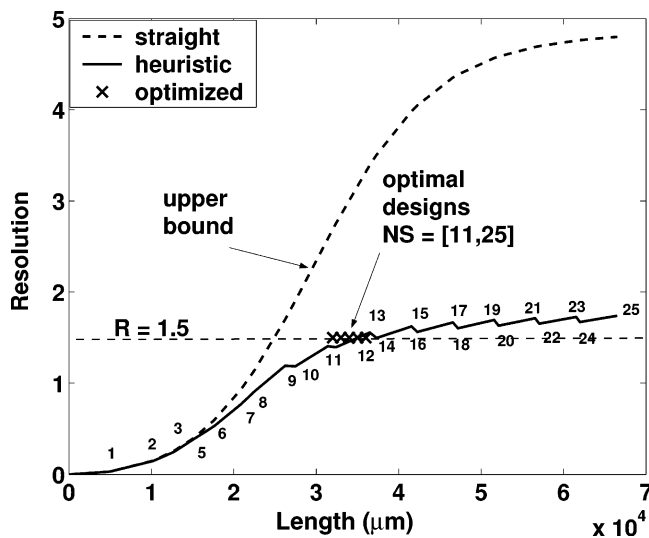


Figure 14. Serpentine design search.

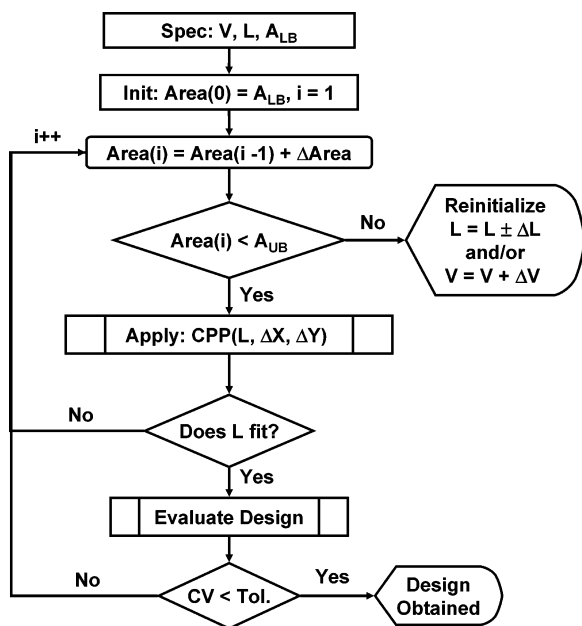


Figure 15. Area incrementation algorithm.

2.4.2. Area-Incrementation Heuristic Algorithm.

In this algorithm, the total channel length and voltage are specified, and the design area is incrementally increased (Figure 15). The search begins with the user setting the initial area, A_{LB} , at an arbitrarily small value. If the assigned design area is less than the maximum allowable design area, A_{UB} , then the CPP algorithm for spirals is invoked to create a design. If the channel length input by the user does not fit within the specified area, then the area is incrementally increased. When the specified channel length does fit within the area required, the design is simulated by the simulator. As in the previous algorithm, if the constraints are not violated, then a feasible design has been identified. If the constraints are not met, an incremental amount of area is added. Adding area results in turns with less curvature and therefore reduces dispersion for the design. The value of the incremental area step size ($\Delta Area$) is chosen by the user depending on the acceptable level of granularity. The algorithm terminates when either a feasible design has been found or when the area hits A_{UB} , the upper limit.

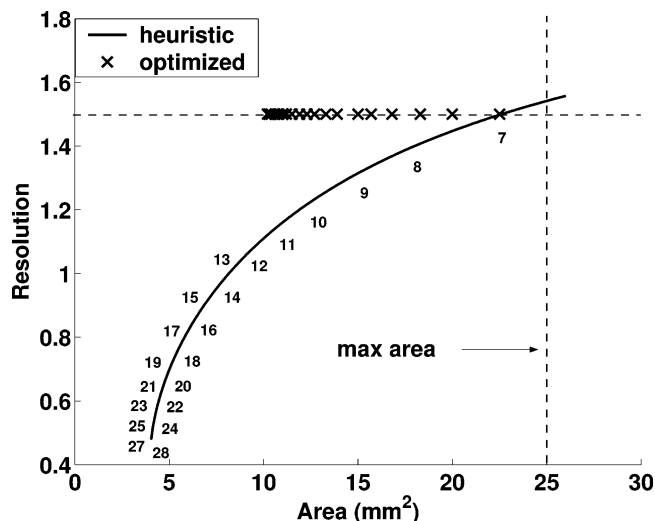


Figure 16. Spiral design search.

Upon failure to find a design, the user can adjust the channel length and increase the voltage. The channel length can be increased to decrease violation of operating constraints or decreased to fit within the specified area.

Figure 16 shows an example spiral synthesis result for the area-incrementation heuristic algorithm. The solid curve represents the solution path for the spiral design. For spirals, the topology changes smoothly as sections are added. The solution procedure starts by putting the required length in as small an area as possible (28 sections) and then slowly expanding the area until feasibility is reached (7 sections). The maximum allowable area for this example is 25 cm^2 , and the first feasible design that is found has 7 sections.

Here again, the points marked by \times represent designs found using the more rigorous optimization methods described in sections 2.4.3–2.4.5. It should be noted that, although both the heuristic and optimization approaches indicate that the 7-section spiral is feasible, the optimization approach is able to find designs that use more sections but require far less area.

Both of the heuristic design techniques are based on iteratively evaluating hundreds or thousands of possible alternative designs in a short period of time. For the examples presented here, over 600 different designs are evaluated per minute. The algorithms provide a good indication as to the relative merits of one design or topology versus another. They are able to search over integer numbers of sections as well as continuous variables. However, because both algorithms rely entirely on the CPP algorithms for channel-layout generation, they are restricted by the implicit assumptions of the CPP algorithms from section 2.3. The numerical optimization approaches described in sections 2.4.3–2.4.5 are more rigorous than the heuristic approaches, but they are currently limited to a prespecified topology with a fixed number of channel sections.

2.4.3. NLP Optimization. We have implemented numerical optimization techniques to create synthesis methods that no longer rely on the implicit assumptions contained within the CPP. Synthesis algorithms using numerical optimization can be made both efficient and robust, which is important when automated design tools are desired. The design problem can be represented as the following nonlinear program (NLP).

$$\min \text{Area}_j = \Delta X \Delta Y \quad \forall i = \text{NS}^L, \dots, \text{NS}^U \quad (5)$$

$$\text{s.t. } R_{j,k} \geq R_{\text{spec}} \quad \forall j, k = 1, \dots, \text{NC} \quad (6)$$

$$\Delta L_{j,k} \geq \Delta L_{\text{spec}} \quad \forall j, k = 1, \dots, \text{NC} \quad (7)$$

$$\Delta X \leq \Delta X_{\text{spec}} \quad (8)$$

$$\Delta Y \leq \Delta Y_{\text{spec}} \quad (9)$$

$$0 \leq V \leq V_{\text{max}} \quad (10)$$

$$w \leq \mathbf{Ls} \leq \Delta X_{\text{spec}} \quad (11)$$

$$\pi w(\text{TR}) \leq \mathbf{Lt} \leq \frac{\pi \Delta Y_{\text{spec}}}{2} \quad (12)$$

Here, we search the integer set of channel sections, NS, between the lower bound on channel sections, NS^L, and the upper bound on channel sections, NS^U, for the design that occupies the minimal area and satisfies the constraints. The lower bound on the number of channel sections required is based on the L value given by eq 4 and the CPP. The maximum number of sections is also given by the CPP algorithms.

For each topology i , we attempt to minimize the area of the design for the vector of section lengths, $\mathbf{L} = [\mathbf{Ls}, \mathbf{Lt}]$, and the voltage V (eq 5). The design is subject to the requirement that the minimum ($R_{j,k}$) resolution between any two species bands be at least R_{spec} for all of the species, NC (eq 6). Furthermore, the minimum separation distance ($\Delta L_{j,k}$) between any two species bands must be greater than or equal to the peak separation distance, ΔL_{spec} , which is usually set to 10 μm . (eq 7). The final design must also fit within the allocated area defined by $A = \Delta X_{\text{spec}} \Delta Y_{\text{spec}}$ (eqs 8 and 9).

The design variables of the system, V and \mathbf{L} , are also bounded. The voltage must be maintained between a realistic upper and lower bound (eq 10). Each straight section in the set of horizontal straight section lengths, \mathbf{Ls} , must be no shorter than one channel width and no longer than ΔX_{spec} (eq 11). Serpentine designs are typically designed within rectangles with the straight channel sections running parallel to the longer dimension of the rectangle (in our formulation $\Delta X_{\text{spec}} \geq \Delta Y_{\text{spec}}$). This aspect ratio is generally preferred because it increases the ratio of straight length to turn length, which provides superior separation performance. However, if long narrow designs are required, the ΔY_{spec} dimension can be set greater than the ΔX_{spec} dimension. Spiral topologies always fit within an approximately square aspect ratio. Each turn section in the set of turn section lengths, \mathbf{Lt} , must be within the region of model applicability defined by the minimum turn ratio ($\text{TR} = r/w$) and the maximum length that can fit within the area in the minimum length direction (eq 12). At present, both serpentine and spiral topologies are constructed using 180° turns.

The solution of the above NLP results in a locally optimal set of channel lengths and an operating voltage. Several methods are available that can be used to solve this type of problem.⁵⁷ A standard successive quadratic programming (SQP)⁵⁸ algorithm was successfully used to solve this problem for spiral topologies. A more tailored approach was used for the optimization of serpentine topologies because the current problem formulation results in discontinuous gradients. This is

because the design area is dictated by the maximum dimensions of the design and not by all of the design variables simultaneously. Small changes in some sections lengths might or might not have an influence on the gradient during optimization. Furthermore, multimodality in the objective space can contribute to convergence difficulties by resulting in regions of local infeasibility.

2.4.4. General Penalty Reformulation. A more robust procedure for the optimization of serpentine topologies was developed through the use of a penalty function. The penalty function was developed first by converting the NLP from section 2.4.3 into the form

$$\min \text{Area}_j(\mathbf{L}, V) \quad (13)$$

$$\text{s.t. } c_i(\mathbf{L}, V) \geq 0 \quad \forall i = 1, \dots, m \quad (14)$$

Both the constraints, eqs 6–9, and bounds, eqs 10–12, from the NLP were converted into a set of inequalities, $i = 1, \dots, m$, all having the same form (eq 14). The constraints in eq 14 are satisfied only when the constraint residuals (c_i) are greater than or equal to 0 for all of the constraints $i = 1, \dots, m$. Below is the generalized penalty reformulation of the transformed NLP (eq 15).⁵⁹

$$\min P(x^k, p^k) = \text{Area}(x^k) + p^k \sum_{i=1}^m [\min(0, c_i(x^k))]^2$$

where

$$p^k = [10, 100, \dots, p^K] \quad \text{and} \quad k = 1, \dots, K \quad (15)$$

The original constrained NLP is converted into an unconstrained minimization of $P(\mathbf{x}, p^k)$, where $\mathbf{x} = (\mathbf{L}, V)$ and p^k is the penalty parameter. The constraints and bounds are essentially compiled into an unconstrained objective function. Whenever any constraint is not satisfied [i.e., $c_i(\mathbf{x}) < 0$], a penalty is added to the objective function, causing the objective to increase. When the constraint is not violated, there is no penalty contribution for that constraint. For each iteration k , larger and larger values of p^k are chosen until the constraints are sufficiently satisfied. As $p^k \rightarrow \infty$, the solution of the penalty function approaches that of the original NLP. In this way, successively more difficult problems can be solved until the constraints are satisfied to the desired level of accuracy.⁶⁰

2.4.5. Adaptive Penalty Parameters. The appropriate selection of penalty parameters can lead to improved convergence. Penalty parameters that are either very large or very small can result in ill-conditioning of the Hessian.⁶¹ Selection of penalty parameters that are too small results in infeasible designs. The goal is to select penalty parameters that are large enough to guarantee feasibility but small enough to prevent numerical problems.

We have attempted to create a simple method that automatically produces a well-scaled penalty parameter for each of the constraints of the NLP. In eq 16, a specific penalty parameter is selected for each constraint, $i = 1, \dots, m$. The vector of penalty parameters, \mathbf{p}^k , is a function of the scaled constraint violation from the previous iteration

$$\frac{|\min(0, c_i(x^{k-1}))|}{\text{SPEC}}$$

and a scalar σ^k . The scalar value SPEC is the target value for the constraint. If the constraint is not violated at the termination of the previous iteration, then $p_i^k = p_i^{k-1}$ to maintain constraint satisfaction during the current iteration. Ideally, σ^k can become large without directly affecting the conditioning of the Hessian because proper scaling is taking place for each iteration. In this method, more emphasis is given to the most violated constraints.

$$\min P(x^k, p^k) = \text{Area}(x^k) + \sum_{i=1}^m p_i^k [\min(0, c_i(x^k))]^2$$

where

$$p_i^k = \sigma^k \frac{|\min(0, c_i(x^{k-1}))|}{\text{SPEC}}$$

if

$$p_i^k = 0, \quad p_i^k = p_i^{k-1}$$

and

$$\sigma^k = [10, 100, \dots, \sigma^K] \quad k = 1, \dots, K \quad (16)$$

For the first iteration, $k = 1$, a scalar penalty parameter is determined for all constraints $p_i^k = \sigma^k$. The initial point, x^0 , is not used to set the individual penalty parameters because such points are typically selected with limited knowledge of the solution space. Basing the vector of penalty parameters on the initial point could lead to a poorly scaled penalty function. Scaled penalty parameters are selected for each subsequent iteration.

The penalty functions described by eqs 15 and 16 can be solved using any number of standard unconstrained optimization algorithms. This is convenient because of the large number of robust unconstrained optimization algorithms that are available. However, the nature of the bounding-box calculation (section 2.2.1) results in discontinuous derivative values that pose problems for most gradient-based optimization techniques.⁶⁰ To handle this complication, we solve the penalty function using an implementation of a modified version of Shor's R algorithm for nonsmooth optimization.⁶²

2.5. Optimization over Multiple Sections. Recall from the NLP formulation in section 2.4.3 that the optimization of serpentine and spiral channel topologies must be performed over an integer set representing the number of channel sections. Currently, the optimization is accomplished by optimizing each design for a fixed number of sections. This is a reasonable approach given the facts that the problem is currently not combinatoric and the number of possible sections is bounded above and below for a given chip.

Results for a series of optimizations of both spiral and serpentine topologies can be seen in Figure 17. Initially, there is a significant decrease in area for both topologies. As the number of sections increases, the area used for the system becomes nearly constant.

It is interesting to note that serpentine designs with even numbers of sections consistently require more area

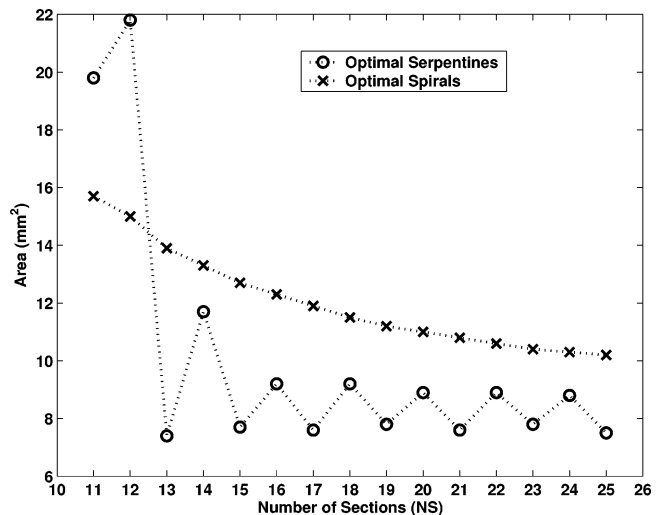


Figure 17. Section number vs area for serpentine and spiral designs.

Table 2. Comparison of Optimization Algorithms for Serpentine Topologies

sections	metrics	SQP	penalty	genetic
9	area (mm ²)	fails	0.168	0.169
	CPU time (min)		1.3	42.8
13	area (mm ²)	0.174	0.173	0.179
	CPU time (min)	3.9	6.1	58.6
17	area (mm ²)	0.176	0.170	0.199
	CPU time (min)	7.7	14.8	124.1
21	area (mm ²)	fails	0.163	0.241
	CPU time (min)		29.5	118.0

than designs with odd numbers of sections. This is because designs with odd numbers of sections use the available area more efficiently by maintaining a higher ratio of total straight channel length to total turn length. The area reduction occurs in a smooth fashion for spiral designs, as would be expected.

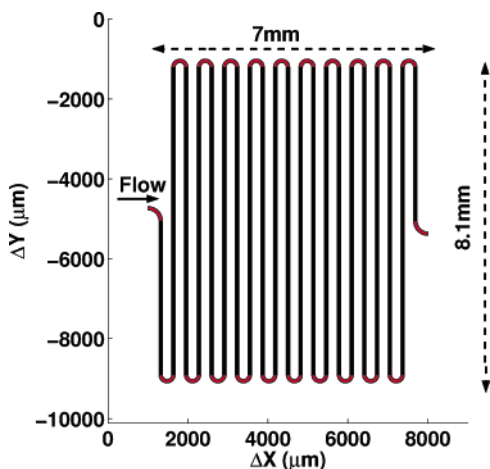
Comparison of Optimization Methods. Table 2 represents a set of optimization trials for serpentine designs. It compares the NLP formulation solved using SQP,⁵⁸ the penalty-function formulation solved using Shor's R algorithm,⁶² and the penalty-function formulation solved using a genetic algorithm.⁶³

In general, the SQP algorithm converges much more rapidly than either the penalty function or the genetic algorithm, but it fails for the 9- and 21-section designs. This is unacceptable, as a robust algorithm is required for synthesis. The penalty function solved using Shor's R algorithm is more robust than the SQP implementation and faster than the genetic algorithm implementation. Furthermore, the Shor's R algorithm implementation has a defined termination criterion based on the values of the objective and design variables, unlike the genetic algorithm, which is simply terminated after a predefined number of generations.⁶⁴

The NLP formulation for spiral designs and the penalty formulation for serpentine designs provide a general, readily adaptable framework for future modification and improvement. The methods used to solve the design optimization problem show promise for eventual implementation as web-based, interactive design tools. Increasing synthesis algorithm speed and robustness is an effort that will receive further attention in the future.

Table 3. Serpentine Design Data^a

parameter	values
actual design area	7.0 mm × 8.1 mm ($A = 57 \text{ mm}^2$)
total separation length	165 mm
channel width	90 μm
channel depth	10 μm
applied electric field	170 V cm^{-1}
applied voltage (over 165 mm)	2.8 kV
maximum available voltage	4.4 kV
number of plates (at 165 mm)	$N_{\text{RB}} = 38\ 100$, $N_{\text{SHA}} = 29\ 000$

^a Extracted from ref 42.**Figure 18.** Original serpentine design.

3. Example Applications

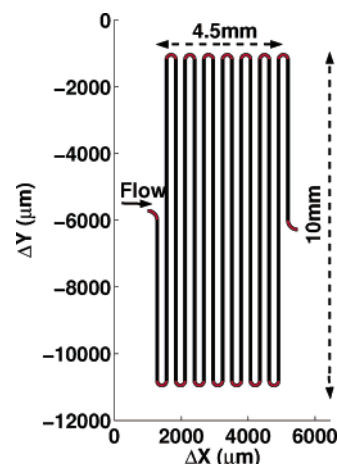
Here we compare designs generated using our techniques with a serpentine design developed by Jacobson et al.⁴² and a spiral design developed by Culbertson et al.³⁶ An interchannel spacing design specification of $\text{PAD} \geq 5 \mu\text{m}$ was obtained from Micronit,⁶⁵ a microfluidic chip fabrication company. Our designs were required to always meet or exceed this requirement. It is shown below that our methods are capable of reducing the areas required for these designs while still maintaining the desired level of separation efficiency.

3.1. Heuristic Design of a Serpentine Channel.

Jacobson et al. present a 43-section serpentine design⁴² that fits within a $1 \text{ cm} \times 1 \text{ cm}$ area. The chemical species to be separated were rhodamine B and sulforhodamine within a sodium tetraborate mobile phase. Table 3 lists some of the important design features and data. Mobilities were extracted from the results presented by Jacobson et al.⁴² and diffusivities were extrapolated using the simulator (section 2.1).

Figure 18 shows a schematic of the original 43-section separation system. We wish to create a design that fits within the $1 \text{ cm} \times 1 \text{ cm}$ design area, maintains the plate number for rhodamine B ($N_{\text{RB}} \geq 38\ 100$) and sulforhodamine ($N_{\text{SHA}} \geq 29\ 000$) and requires less area than the original design.

Through the use of the heuristic algorithms discussed in sections 2.4.2 and 2.4.1, the design in Figure 19 is obtained. By allowing the design to expand to the full y dimension and reducing the number of channel sections to 31, we are able to reduce the design area by approximately 21%. This is all done while maintaining the applied voltage at 2.8 kV. If the applied voltage is increased to 4 kV and the design is allowed to utilize the entire $1 \text{ cm} \times 1 \text{ cm}$ area, an increase in plate

**Figure 19.** Synthesized serpentine design.**Table 4. Spiral Design Data^a**

parameter	value
actual design area	3.7 cm × 3.8 cm ($A = 14 \text{ cm}^2$)
total separation length	22.2 cm
channel width	40 μm
channel depth	15 μm
applied electric field	1170 V cm^{-1}
applied voltage (over 22.2 cm)	26.0 kV
maximum available voltage	30.0 kV
number of plates (at 22.2 cm)	$N_{\text{DCF}} = 1.04 \times 10^6$

^a Extracted from ref 36.

number of approximately 55% or a reduction in area of approximately 25% (for 43 sections) can be achieved.

The design shown in Figure 19 was obtained in under 1 min using our heuristic methods. The benefits of using an automated synthesis tool for this kind of design is clear: whereas there is no guarantee of optimality, a designer is able to quickly and efficiently push designs toward a desired objective.

3.2. Optimization of a Spiral Design. Culbertson et al.³⁶ presented a spiral design with four channel sections between the injector and detector. The entire design, including all wells, fits within a $5 \text{ cm} \times 5 \text{ cm}$ area. The spiral topology itself fits within an approximately $3.7 \text{ cm} \times 3.8 \text{ cm}$ area. In our comparison, we focus only on the area occupied by the spiral topology. The chemical species used was dichlorofluorescein (DCF), and its physical properties were extracted from the results presented by Culbertson et al.³⁶ The mobile phase used was a boric acid/TRIS buffer solution. Table 4 lists some of the important design features and data.

Figure 20 shows a schematic of the separation portion of the original spiral topology. Here, we use the optimization methods described in section 2.4 to design a spiral separation system that is smaller than the original design and maintains the same or greater plate number ($N_{\text{DCF}} \geq 1.04 \times 10^6$).

As can be seen in Figure 20, the original design is essentially four semicircles with large radii and narrow channel widths. This configuration leads to the lowest possible dispersion. However, the design leaves a great deal of interchannel spacing that allows for significant compaction of the design. In Figure 21, we see that the design can actually be reduced in area by approximately 56%. This results from the addition of six new channel sections resulting in a 10-section design. An applied voltage of 27 kV was used, which leaves an extra 3 kV for channel routing to the wells.

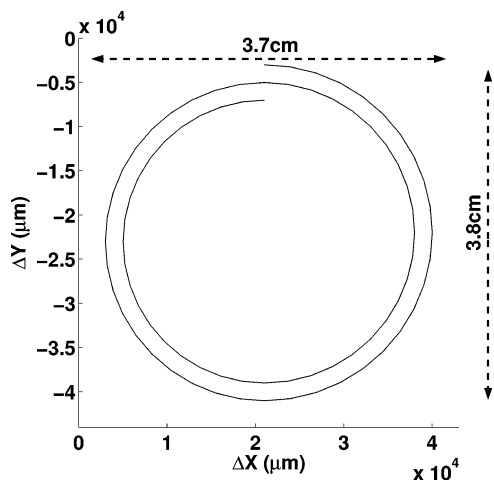


Figure 20. Original spiral design.

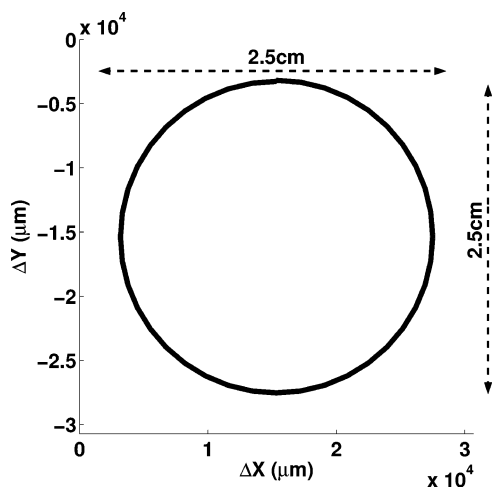


Figure 21. Optimized spiral design.

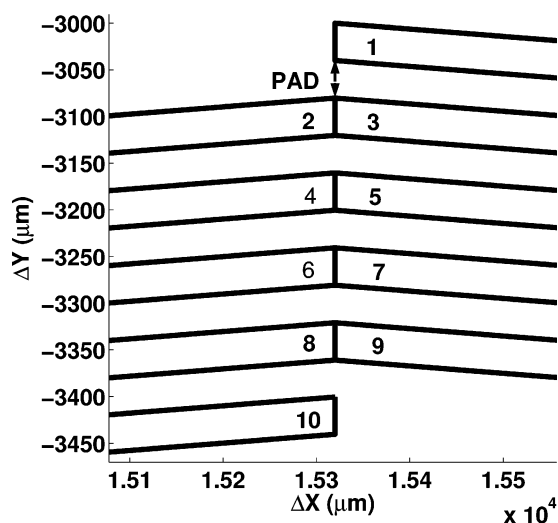


Figure 22. Magnification of optimized spiral design.

It can be seen that the channels are compressed as close as possible to each other but still maintain the minimal set channel spacing. Figure 22 shows a magnification of the optimized design. It can be seen that the interchannel spacing requirement is met. Furthermore, this design retains approximately 4.5 cm^2 of space interior to the spiral for the placement of the waste well. This design could be further compressed by adding more

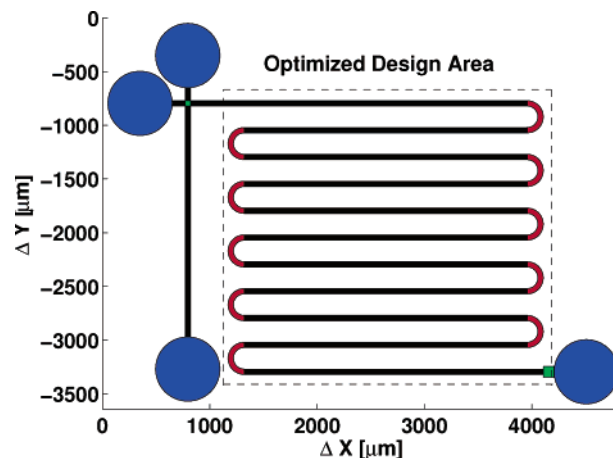


Figure 23. Optimal serpentine design.

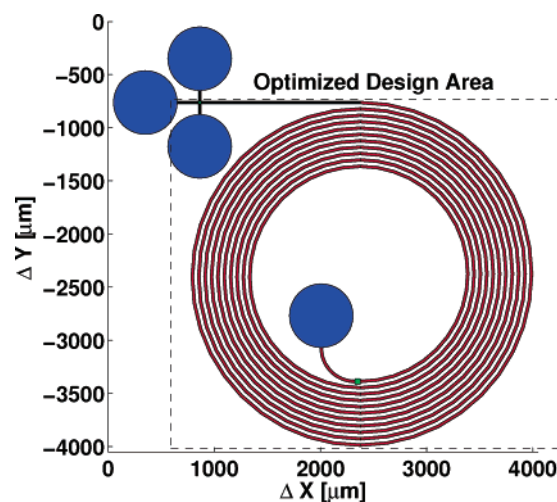


Figure 24. Optimal spiral design.

sections, or by increasing the applied voltage, or by decreasing the required interchannel spacing.

4. Conclusion and Future Directions

Figures 23 and 24 show example minimum-area designs for 21-section serpentine and spiral topologies generated using the numerical optimization based algorithms described in sections 2.4.3–2.4.5. Both of these designs meet the performance, operating, and physical constraints on the system. For both topologies, the channel sections were optimized and the injection and waste wells were routed afterward by hand. It can be seen that the dimensions of the optimized part of the design, the optimized design area (bounded by dashed lines), is smaller for the serpentine than for the spiral topology. However, the overall design area is smaller for the spiral. This example illustrates the idea that the area occupied by all pieces of the system must be considered simultaneously to obtain truly optimal designs. This is a key area of future research.

We have just begun to explore many of the ways in which PSE techniques can be applied to the synthesis of LoC devices. We have made headway into the design and optimization of microchip-based electrophoretic separation systems. We have also identified some of the key issues and established appropriate groundwork for the expansion of our methods toward full-scale LoC device synthesis. In the future, we would like to develop methods for the synthesis of complex LoC devices.

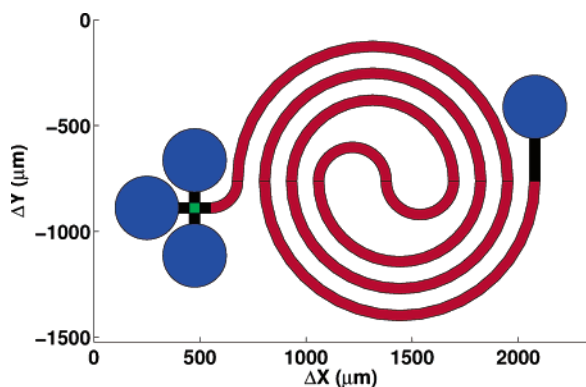


Figure 25. Complimentary turn spiral design.

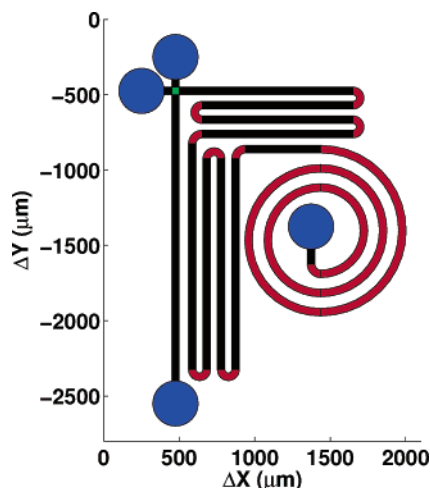


Figure 26. Variable topology hybrid design.

4.1. Defining Complexity. Currently, there is no clear definition of complexity in LoC design. The most complex designs to date consist of arrays of hundreds of replicated simple channel structures functioning in parallel on a microchip.⁶⁶ These devices perform a single function in a multiplexed fashion, thereby increasing throughput. We would like to define complexity as the difficulty of the task that the LoC device is capable of handling. We would like to answer the following questions: (i) Can a single general LoC device be designed that is capable of performing various difficult separation, mixing or reaction operations? (ii) Can a fully integrated LoC device be created that incorporates mixing, reaction, and separation on a single device? (iii) Can general synthesis methods be developed to accomplish each of these tasks?

4.2. Variable Topology Integrated Systems. To accomplish these tasks, it will no longer be possible to remain confined to standard serpentine or spiral topologies. The optimal design and placement of units with irregular and variable dimensions in precise orientations must be addressed. Further, the design area itself might be irregular as a result of the fixed placement of auxiliary equipment such as power supplies, structural components, or fluid-handling equipment. Figures 25 and 26 show examples of possible hybrid topologies. Figure 25, which is similar to the folded channel topology presented by Griffiths and Nilson,⁵⁰ allows a spiral topology to be integrated in-line with other on-chip components because the waste well is moved to the outside of the design. Figure 26 shows a variable-topology hybrid design that might arise from an ir-

regularly shaped design area. We would like to develop general synthesis methods to handle these topologies as well as parallel and integrated systems on a chip.

The proper placement of injection and waste wells, which has to do with a concept known as the world-to-chip interface, will become of increasing importance as progress is made toward practical devices. The integration of on-chip reaction, mixing, and injection will pose new modeling, simulation, and layout challenges.

4.3. Practical Solution Approaches. We will apply both traditional and novel PSE techniques to meet the design and synthesis challenges mentioned above. Microchip system design might be amenable to superstructure optimization or disjunctive programming approaches.⁶⁷ We are also currently investigating VLSI Floor-planning formulations.^{53–55} Computational geometry techniques for determining segment–segment and nonconvex polygon intersection⁶⁸ could be of great use. It might be possible to draw practical design optimization insights from structural design optimization methods that deal with shape-related, geometrical, and topological problems.⁶⁹ Agent-based optimization⁷⁰ is a promising method currently being pursued.

Acknowledgment

This research effort was sponsored by the Defense Advanced Research Projects Agency (DARPA) and U.S. Air Force Research Laboratory under Contract F30602-01-2-0587 (DARPA DSO SIMBIOSYS Program, Dr. Anantha Krishnan, Program Manager) and by the National Science Foundation under Grant NSF/ITR/CCR-0325344. The authors thank the members of the SYNBIOSYS group at Carnegie Mellon, especially James F. Hoburg, Qiao Lin, Bikram Baidya, Ryan S. Magargle, and Yi Wang, for discussions on LoC modeling and design methodologies.

Literature Cited

- (1) Maluf, N. *An Introduction to Microelectromechanical Systems Engineering*; Artech House, Inc.: Boston, MA, 2000.
- (2) Reyes, D. R.; Iossifidis, D.; Auroux, A.; Manz, A. Micro Total Analysis Systems. 1. Introduction, Theory, and Technology. *Anal. Chem.* **2002**, *74*, 2623–2634.
- (3) Gravesen, P.; Branebjerg, J. Microfluidics—A Review. *J. Micromech. Microeng.* **1993**, *3*, 168–182.
- (4) Cuta, J. M.; Bennett, W. D.; McDonald, C. E.; Raviguru- rajan, T. S. Fabrication and testing of microchannel heat exchangers. In *Microlithography and Metrology in Micromachining*; Postek, M. T., Jr., Ed.; SPIE Press: Bellingham, WA, 1995; pp 152–160.
- (5) Auroux, A.; Iossifidis, D.; Reyes, D. R.; Manz, A. Micro Total Analysis Systems. 2. Analytical Standard Operations and Applications. *Anal. Chem.* **2002**, *74*, 2637–2652.
- (6) Ehrfeld, W.; Hessel, V.; Lehr, H. *Microreactors: New Technology for Modern Chemistry*; Wiley-VCH: Weinheim, Germany, 2000.
- (7) Jensen, K. F. The impact of MEMS on the chemical and pharmaceutical industries. In *Solid-State Sensor and Actuator Workshop. Technical Digest*; IEEE Press: Piscataway, NJ, 2000; pp 105–110.
- (8) Kehr, J. A. survey on quantitative microdialysis: Theoretical models and practical implications. *J. Neurosci. Methods* **1993**, *48*, 251–261.
- (9) Chaurasia, C. In vivo microdialysis sampling: Theory and applications. *Biomed. Chromatogr.* **1999**, *13*, 317–332.
- (10) Freemantle, M. Downsizing Chemistry. *Chem. Eng. News* **1999**, *77*, 27–35.
- (11) Tang, W. C.; Lee, A. P. Military applications of microsys- tems. *Ind. Phys.* **2001**, *7* (1), 26–29.
- (12) Robert, J. Continuous monitoring of blood glucose. *Horm. Res.* **2002**, *57*, 81–84.

- (13) Malsch, I. Protein research calls for advanced instruments. *Ind. Phys.* **2003**, *9* (4), 18–22.
- (14) Shaorong, L.; Shi, Y.; Ja, W. W.; Mathies, R. A. Optimization of high-speed DNA sequencing on microfabricated capillary electrophoresis channels. *Anal. Chem.* **1999**, *71*, 566–573.
- (15) Gad-el Hak, M. The Fluid Mechanics of Microdevices. *J. Fluids Eng.* **1999**, *121*, 5–33.
- (16) Pfeiffer, A. J.; Mukherjee, T.; Huan, S. Topology tradeoffs in the synthesis of chip-based electrophoretic separation systems. In *NanoTech 2003: Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show*; NSTI (Nano Science & Technology Institute): Cambridge, MA, 2003; Vol. 1, pp 250–253.
- (17) Nighswonger, G. Micromachines: A big future for small devices. *Med. Device Diagn. Ind. Mag.* **1999**, *21*, 48.
- (18) Oddy, M. H.; Santiago, J. G.; Mikkelsen, J. C. Electrokinetic instability micromixing. *Anal. Chem.* **2001**, *73*, 5822–5832.
- (19) Waters, L. C.; Jacobson, S. C.; Kroutchinina, N.; Khandurina, J.; Foote, R. S.; Ramsey, J. M. Multiple sample PCR amplification and electrophoretic analysis on a microchip. *Anal. Chem.* **1998**, *70*, 5172–5176.
- (20) Lundqvist, A.; Chiu, D. T.; Orwar, O. Electrophoretic separation and confocal laser-induced fluorescence detection at ultralow concentrations in constricted fused-silica capillaries. *Anal. Chem.* **2003**, *76*, 1737–1744.
- (21) Landers, J. P. *Handbook of Capillary Electrophoresis*; CRC Press LLC: Boca Raton, FL, 1996.
- (22) Ouellette, J. A new wave of microfluidic devices. *Ind. Phys.* **2003**, *9* (4), 14–17.
- (23) Jacobson, S. C.; Ramsey, J. M. Microfabricated Chemical Separation Devices. *High-Performance Capillary Electrophoresis*; Khaledi, M., Ed.; Wiley: New York, 1998; Chapter 18, pp 613–632.
- (24) Lacher, N. A.; Garrison, K. E.; Martin, R. S.; Lunte, S. M. Microchip capillary electrophoresis/electrochemistry. *Electrophoresis* **2001**, *22*, 2526–2536.
- (25) Giddings, C. J. *Unified Separation Science*; John Wiley & Sons: New York, 1991.
- (26) Steinar, F.; Hassel, M. Control of electroosmotic flow in nonaqueous capillary electrophoresis by polymer capillary coatings. *Electrophoresis* **2003**, *24*, 399–407.
- (27) Doherty, E. A. S.; Meagher, R. J.; Albarghouthi, M. N.; Barron, A. E. Microchannel wall coatings for protein separations by capillary and chip electrophoresis. *Electrophoresis* **2003**, *24*, 34–54.
- (28) Khaledi, M. G., Ed. *High-Performance Capillary Electrophoresis*; John Wiley & Sons: New York, 1998.
- (29) Gaš, B.; Kenndler, E. Dispersive phenomena in electromigration separation methods. *Electrophoresis* **2000**, *21*, 3888–3897.
- (30) Probst, R. F. *Physicochemical Hydrodynamics: An Introduction*, 2nd ed.; Wiley & Sons: New York, 1994.
- (31) Cummings, E. B.; Griffiths, S. K.; Nilson, R. H.; Paul, P. H. Conditions of similitude between the fluid velocity and electric field in electroosmotic flow. *Anal. Chem.* **2000**, *72*, 2526–2532.
- (32) Porras, S. P.; Riekkola, M.; Kenndler, E. Resolution in capillary electrophoresis with nonaqueous methanol as solvent: Theoretical prediction and experimental confirmation. *Electrophoresis* **2001**, *22*, 3798–3804.
- (33) Kerby, M. B.; Chien, R. Increase of separation resolution through field enhancement in microchips. *Electrophoresis* **2002**, *23*, 3545–3549.
- (34) Bharadwaj, J. G.; Santiago, R.; Mohammadi, B. Design and optimization of on-chip capillary electrophoresis. *Electrophoresis* **2002**, *23*, 2729–2744.
- (35) Jacobson, S. C.; Culbertson, C. T.; Daler, J. E.; Ramsey, J. M. Microchip structures for submillisecond electrophoresis. *Anal. Chem.* **1998**, *70* (16), 3476–3480.
- (36) Culbertson, C. T.; Jacobson, S. C.; Ramsey, J. M. Microchip devices for high-efficiency separations. *Anal. Chem.* **2000**, *72*, 5814–5819.
- (37) Jacobson, S. C.; Hergenroder, R.; Koutny, L. B.; Ramsey, J. M. High-speed separations on a microchip. *Anal. Chem.* **1994**, *66* (7), 1114–1118.
- (38) Paegel, B. M.; Hutt, L. D.; Simpson, P. C.; Mathies, R. A. Turn geometry for minimizing band broadening in microfabricated capillary electrophoresis channels. *Anal. Chem.* **2000**, *72*, 3030–3037.
- (39) Griffiths, S. K.; Nilson, R. H. Band spreading in two-dimensional microchannel turns for electrokinetic species transport. *Anal. Chem.* **2000**, *72*, 5473–5482.
- (40) Molho, J. I.; Herr, A. E.; Mosier, B. P.; Santiago, J. G.; Kenny, T. W.; Brennen, R. A.; Gordon, G. B.; Mohammadi, B. Optimization of turn geometries for microchip electrophoresis. *Anal. Chem.* **2001**, *73*, 1350–1360.
- (41) Culbertson, C. T.; Jacobson, S. C.; Ramsey, J. M. Dispersion sources for compact geometries on microchips. *Anal. Chem.* **1998**, *70*, 3781–3789.
- (42) Jacobson, S. C.; Hergenroder, R.; Koutny, L. B.; Warmack, R. J.; Ramsey, J. M. Effects of injection schemes and column geometry on the performance of microchip electrophoresis devices. *Anal. Chem.* **1994**, *66*, 1107–1113.
- (43) Magargle, R. S.; Hoburg, J. F.; Mukherjee, T. A simple description of turn-induced transverse field dispersion in microfluidic channels for system level design. In *NanoTech 2003: Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show*; NSTI (Nano Science & Technology Institute): Cambridge, MA, 2003; Vol. 1, pp 214–217.
- (44) Wang, Y.; Lin, Q.; Mukherjee, T. Analytical dispersion models for efficient simulation of complex microchip electrophoresis systems. In *Proceedings of MicroTAS 2003*; Preferred Meeting Management, Inc.: San Diego, CA, 2003; pp 135–138.
- (45) Wang, Y.; Lin, Q.; Mukherjee, T. Composable system simulation of dispersion in complex electrophoretic separation microchips. In *NanoTech 2004: Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show*; NSTI (Nano Science & Technology Institute): Cambridge, MA, 2004; Vol. 1, pp 59–62.
- (46) Ermakov, S. G.; Jacobson, S. C.; Ramsey, J. M. Computer simulations of electrokinetic transport in microfabricated channel structures. *Anal. Chem.* **1998**, *70*, 4494–4504.
- (47) Ermakov, S. V.; Jacobson, S. C.; Ramsey, J. M. Computer simulations of electrokinetic mass transport in microfabricated fluidic devices. In *MSM '99: Technical Proceedings of the 1999 International Conference on Modeling and Simulation of Microsystems*; NSTI (Nano Science & Technology Institute): Cambridge, MA, 1999; pp 534–537.
- (48) Ermakov, S. V.; Jacobson, S. C.; Ramsey, J. M. Computer simulations of electrokinetic injection techniques in microfluidic devices. *Anal. Chem.* **2000**, *72*, 3512–3517.
- (49) Griffiths, S. K.; Nilson, R. H. Low-dispersion turns and junctions for microchannel systems. *Anal. Chem.* **2001**, *73*, 272–278.
- (50) Griffiths, S. K.; Nilson, R. Design and analysis of folded channels for chip-based separations. *Anal. Chem.* **2002**, *74*, 2960–2967.
- (51) Fiechtner, G. J.; Cummings, E. B. Faceted designs of channels for low-dispersion electrokinetic flows in microfluidic systems. *Anal. Chem.* **2003**, *75*, 4747–4755.
- (52) Wang, Y.; Lin, Q.; Mukherjee, T. Universal Joule Heating model in electrophoretic separation microchips. In *Proceedings of MicroTAS 2002*; Preferred Meeting Management, Inc.: San Diego, CA, 2002; pp 82–84.
- (53) Ying, C.; Wong, J. S. An analytical approach to floorplanning for hierarchical building block layout. *IEEE Trans. Comput.-Aided Des.* **1989**, *8* (4), 403–412.
- (54) Wang, T.; Wong, D. F. Optimal floorplan area optimization. *IEEE Trans. Comput.-Aided Des.* **1992**, *11* (8), 992–1002.
- (55) Etawil, H.; Areibi, S.; Vannelli, A. Attractor–repeller approach for global placement. In *Proceedings of the 1999 IEEE/ACM International Conference on Computer-Aided Design*; IEEE Press: Piscataway, NJ, 1999; pp 20–24.
- (56) Dolnik, V.; Liu, S.; Jovanovich, S. Capillary electrophoresis on a microchip. *Electrophoresis* **2000**, *21*, 41–54.
- (57) Floudas, C. A.; Pardalos, P. M., Eds. *Encyclopedia of Optimization*; Kluwer Academic Publishers: Dordrecht, The Netherlands, 2001.
- (58) *MATLAB–MATrix LABoratory*, version 6.5; The MathWorks, Inc.: Natick, MA (<http://www.mathworks.com>) (accessed June 2003).
- (59) Edgar, T. F.; Himmelblau, D. M.; Lasdon, L. M. *Optimization of Chemical Processes*, 2nd ed.; McGraw-Hill: New York, 2001.
- (60) Gill, P. E.; Murray, W.; Wright, M. H. *Practical Optimization*; Academic Press: New York, 1981.
- (61) Fletcher, R. *Practical Methods of Optimization*, 2nd ed.; Wiley: New York, 2000.
- (62) Kuntsevich, A.; Kappel, F. *SolvOpt, the Solver for Local Nonlinear Optimization Problems*; Karl-Franzens University of Graz: Graz, Austria, 1997.

(63) Chipperfield, A. J.; Fleming, P. J.; Pohlheim, H.; Fonseca, C. M. *Genetic Algorithm Toolbox for Use with Matlab*, version 1.2; Department of Automatic Control and Systems Engineering, University of Sheffield: Sheffield, U.K., 1995.

(64) Mitchell, M. *An Introduction to Genetic Algorithms*; The MIT Press: Cambridge, MA, 1996.

(65) Micronit Microfluidics B.V., Enschede, The Netherlands. <http://www.micronit.com> (accessed Nov 2003).

(66) Emrich, C. A.; Tian, H.; Medintz, I. L.; Mathies, R. A. Microfabricated 384-lane capillary array electrophoresis bioanalyzer for ultrahigh-throughput genetic analysis. *Anal. Chem.* **2002**, *74*, 5076–5083.

(67) Biegler, L. T.; Grossmann, I. E.; Westerberg, A. W. *Systematic Methods of Chemical Process Design*. Prentice Hall: Upper Saddle River, NJ, 1997.

(68) Cormen, T. H.; Leiserson, C. E.; Rivest, R. L. *Introduction to Algorithms*; The MIT Press: Cambridge, MA, 1992.

(69) Haftka, R. T.; Gürdal, Z.; Kamat, M. P. *Elements of Structural Optimization*; Kulwer Academic Publishers: Dordrecht, The Netherlands, 1990.

(70) Sirola, J. D.; Huan, S.; Westerberg, A. W. Toward agent-based process systems engineering: Proposed framework and application to nonconvex optimization. *Comput. Chem. Eng.* **2003**, *27* (12), 1801–1811.

Received for review August 15, 2003

Revised manuscript received January 27, 2004

Accepted February 2, 2004

IE034071T