Synthesis of a Wideband Low Noise Amplifier

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ABSTRACT

Two generations of a wideband low noise amplifier (LNA) employing noise canceling principle have been synthesized. The first generation design was fabricated in a 0.35 μm SiGe BiCMOS process. It has a measured peak S_{21} of 17 dB and noise figure less than 3 dB over a bandwidth of 2.6 GHz while consuming 32.5 mW of power from a 2.5 V supply. The calculated figure of merit (FOM) is better than many reported wideband LNAs, including a few from even more advanced processes. The synthesis design constraints were improved based on the analysis of the first generation design. A second generation design was synthesized with the updated constraints. Its simulation results show that its FOM is better than its predecessor.

Categories and Subject Descriptors

B.7.1 **[Integrated Circuits]**: Types and Design Styles - *Advanced Technologies*

General Terms

Design

Keywords

Synthesis, Wideband LNA, RFIC

1. INTRODUCTION

Traditional wireless communication systems are designed for only one communication standard with its own dedicated frequency band(s). However, the consumer demand to have the same handset do everything, everywhere, is leading to developers of wireless systems integrating multiple standards onto a single device. Multiple standards imply that the handset radio must support multiple frequency bands. Design of such radio systems focus on issues such as frequency planning and hardware sharing [1]. These issues lead to two alternate front end architectures: *parallel* [2] or *reconfigurable* [3]. The parallel architecture has a dedicated signal path for each desired frequency band of operation. Each of these signal paths has its own band-pass filter (BPF) and a narrowband low noise amplifier (LNA), tuned to the desired band using passive circuit elements [4]. This architecture suffers from increased system size which translates into a higher system cost [5]. One possible way of reducing this cost is by sharing the system hardware over the different signal paths. Since reconfigurable BPFs have been demonstrated in [6], hardware sharing in multiband transceiver can be achieved by using a wideband LNA in conjunction with such a filter. This approach replaces multiple signal paths with a single path. Therefore, to reduce the system size, in this paper, we consider a wideband LNA.

An approach to a wideband amplifier design is the distributed amplifier, in which several lumped inductor and capacitor elements interconnect simple amplifier topologies [7]. Although each stage adds to the gain, it simultaneously degrades the noise, leading to noise figure (NF) that are too large for LNA applications. Also since such amplifiers use multiple stages of simple amplifiers they consume a lot of power and take up a lot of area because of the use of on chip passives. Wideband LNAs can also be designed using wideband matching networks. Even though amplifiers employing this method [8], [9] do not consume high power they still consume large chip area as they make use of area expensive passives. Apart from above stated drawbacks, on-chip inductors add their own noise because of their poor quality factor.

In low noise amplifier, the critical design trade-offs tend to be between gain and noise. Typically, one does not want to give up on gain, so alternate ways for reducing noise are needed. Some noise reduction is likely if micromachining techniques are used to improve the quality factor of lumped on-chip inductors [10]. However, this approach cannot completely eliminate inductor noise. Complete inductor noise elimination requires an inductorless topology (which also substantially reduces area). However, even with such a topology, the transistors and resistors continue to contribute to circuit noise. To further reduce this noise, an approach that cancels some of the transistor and resistor noise in wideband LNAs is desired. The wideband LNA designs in this paper focuses on a wideband LNA topology that employs noise cancellation [11]

RF circuit performance measures (power, gain and NF to name few) are affected significantly by the circuit parasitics. Managing the trade-offs between many competing RF specifications, while handling the parasitics that limit RF performance makes RF design complex and time consuming. Simulation-based optimization tools are therefore critical to reducing design cycle time and handling design complexity while not compromising circuit performance. Such tools are now commercially available, and have already been used to synthesize narrowband LNAs [12].

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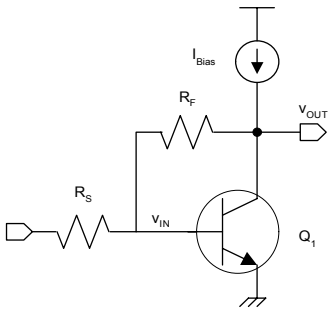

Figure 1. Shunt-feedback common emitter schematic.

This paper discusses the design of two generations of a SiGe HBT based noise-canceling LNA designed using an automated synthesis tool. The LNAs have been designed for integration with the reconfigurable RF MEMS circuits [6] and mixer-filters [13] of interest in reconfigurable radios [3]. The SiGe LNA has the same topology as the CMOS one in [11]. The SiGe BiCMOS process is chosen as it has several advantages [14] over CMOS processes. The main advantages are that SiGe HBTs have lower noise and better transconductance at a given bias current.

2. WIDEBAND LNA TOPOLOGY

In the LNA design getting input matching to 50 Ω is a very important requirement. It can be achieved over a wideband of frequencies by using a common emitter (CE) stage with resistive shunt feedback as shown in Figure 1. Low frequency expressions for its input impedance, gain and output impedance can be derived using first order analysis as described below.

Considering the small signal equivalent of the circuit shown in Figure 1 and assuming that (a) the parasitic base resistance is small compared to the transistor's small signal input resistance, $r_b \ll r_\pi$, (b) the feedback resistance is small compared to the transistor's output resistance, $R_F \ll r_o$ and (c) the current gain, β, is large, we can obtain the gain, input and output impedance as:

$$A_V = -(g_{m1}R_F - 1) \quad (1)$$

$$R_{in} = 1/g_{m1} \quad (2)$$

$$R_{out} = (R_S + R_F)/2 \quad (3)$$

Setting $R_{in} = R_S = 50\Omega = R_{out}$ in equation (2) & (3) leads to $R_F = 50\Omega$ and $g_{m1} = 1/(50\Omega)$. Unfortunately, this implies zero gain. In order to obtain finite gain, an emitter follower can be added as a second stage as shown in Figure 2 (the high pass filter is used to independently bias the two stages). This new stage decouples the gain and output impedance match requirements. However, this is at the expense of the added noise from the second stage.

Cancellation of the noise due to input stage transistors, by taking advantage of the resistive feedback, R_F, can be used to compensate for the added second stage noise. R_F causes the noise at node V_{OUT1} due to transistors Q_1 and P_1 to appear at V_{IN} with an attenuation of $A = R_F/R_S + 1$. Assuming unity gain for the emitter-follower, the noise at V_{OUT1} also appears at V_{OUT} without any attenuation. This output noise can be cancelled by amplifying the attenuated noise fed back through R_F to the input by using Q_2 (originally a current source) as an inverting amplifier with gain $-A$.

The final topology is shown in Figure 3. The current source, P_2, provides an extra degree of freedom which is used to decouple the output impedance match from Q_2's gain. The output impedance, $1/g_{m3}$ (if the output resistances of Q_2 and P_2 are ignored), is matched to 50Ω. Gain from the input of transistor Q_2 to the output is $-g_{m2}R_{out}$ which simplifies to $-g_{m2}/g_{m3}$. Maximum noise cancellation requires Q_2's gain to equal $-A$. Since the ratio of the transconductances is the same as the ratio of collector currents, this is achieved by sizing Q_2 such that it pulls A times I_{Q3}. The extra current comes from transistor P_2 which is sized to ensure the current ratio is A.

3. AUTOMATED DESIGN SYNTHESIS

The equations in the previous section assumed a simplified transistor model. Optimizing circuit performance to ensure noise cancellation over a wide bandwidth while meeting the other LNA specifications requires careful attention to the detailed device model that can only be considered through circuit simulation. Therefore, a commercial synthesis tool that employs simulation for performance evaluation [15] was adopted to synthesize the circuit with desired specifications while employing minimum design time and effort.

In this tool, an optimization-based synthesis engine iteratively calls a circuit simulator with suggested candidate designs. The simulator evaluates the candidate circuit performance, which is compared against the specifications by the synthesis engine to determine the next candidate design. The tool stops when best attainable design is achieved.

In addition entering the circuit topology (Figure 3.), the synthesis setup involves identifying the design variables, the circuit design constraints and design goals (performance matrices like S-parameters, power etc.). The variables used during synthesis include device geometries (lengths and widths of the HBT emitters, MOS gates, polysilicon resistors and MIM capacitors), device multiplicity, as well as the bias currents.

4. FIRST GENERATION LNA

4.1 Design

The target of the first generation design was to maximize the noise-cancellation, thereby minimizing the contribution of the

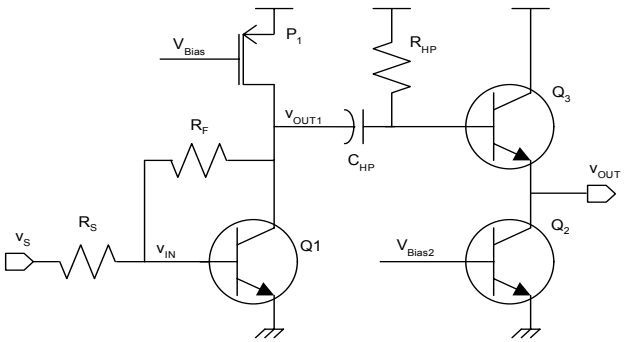

Figure 2.LNA with emitter follower as second stage.

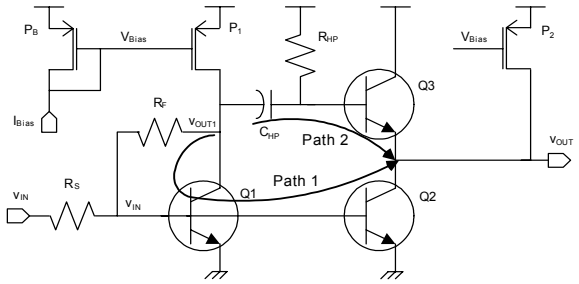

Figure 3.Overall noise-canceling wideband LNA.

noise in the first stage of the LNA. An additional goal was high gain needed for the MEMS-based radio [3].

Maximum first stage noise cancellation occurs when the gains along "Path 1" and "Path 2" (shown in Figure 3), are matched. Therefore constraints relating the devices sizes to ensure this matching occurs was included in the synthesis run. These relations were obtained using the equations derived in Section 2 and are shown in Figure 4. As described in Section 2, Q_2 is constrained to be $A*Q_3$. For design simplicity and layout matching Q_3 is constrained to be identical to Q_1. The overall gain of "Path 1" is equal to the product of gain through transistor Q_2 and attenuation through feedback resistor R_F. Thus, the value of R_F is tied to the multiplicity of Q_2 through the relation $R_F = (1+A)*R_S$. These relations had the added benefit of reducing the number of variables and thus the size of the design space, shortening the synthesis time.

To achieve the high gain, and ensure good noise performance, only S-parameters and NF were set as the design goals. Following synthesis, the LNA layout was generated manually. The LNA was fabricated in a 0.35µm SiGe BiCMOS process.

4.2 Measurement Results

Figure 5 shows the die photograph of fabricated circuit with probe pads for RF I/O and DC biasing. The LNA was tested using a Cascade Microtech Probe station. S-parameters were measured using an Agilent E8364A Vector Network Analyzer. The noise figure was measured using an Agilent E4440A Spectrum Analyzer with Noise Figure personality. The circuit non-linearity was also characterized using the spectrum analyzer.

Figure 6(a) shows the measured transmission gain (S_{21}) and noise figure (NF) frequency responses of the LNA with 50 Ω termination. It has peak S_{21} of 17 dB over a -3 dB bandwidth of 2.64 GHz.

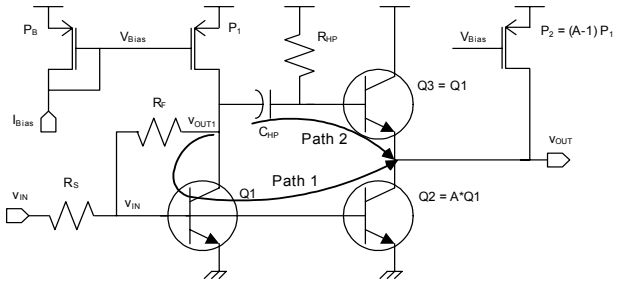

Figure 4.First generation design constraint.

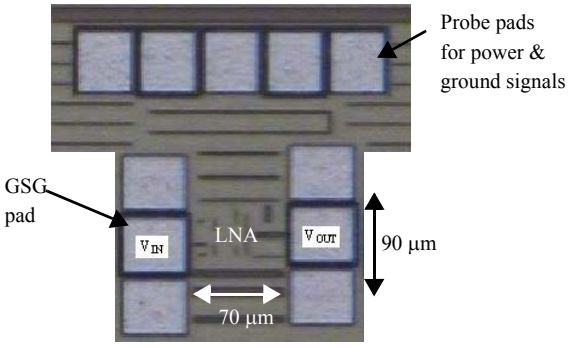

Figure 5.Die photograph showing wideband LNA sandwiched by GSG input and output pads. DC probe pads are located north of the LNA.

The noise figure is less than 3 dB over the entire bandwidth. All of the S-parameters are shown in Figure 6(b). The circuit has a measured third-order intermodulation intercept, IIP3, (obtained using two tones at 1.5 and 1.505 GHz) of -1.14 dBm. The 1 dB input compression point, ICP, was -16.5 dBm at 1.5 GHz. For these measurements the circuit was biased at 13 mA from a 2.5 V supply.

Table 1 summarizes the measured circuit performance and compares it with the post-layout simulation of the extracted circuit. Narrowband LNAs are often compared using a figure of merit (FOM), $S_{21}/(NF \cdot P_{DC})$ [16]. As bandwidth is equally important

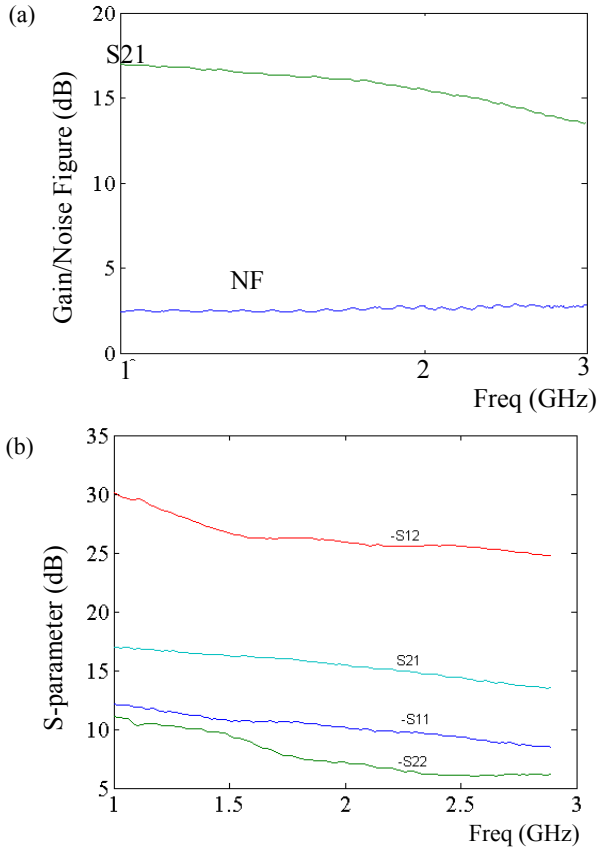

Figure 6.Measured (a) Gain and NF frequency response and (b) S-parameter frequency response.

Table 1. 1st generation wideband LNA performance (measured vs post layout simulation)

	Measurement	Simulation
S_{21} [dB]	17	18
S_{11} [dB]	< -8.9	< -8
S_{12} [dB]	< -25.3	< -23.5
S_{22} [dB]	< -6	< -6.7
BW [GHz]	2.6	2.8
NF [dB]	< 3	< 2.7
ICP [dBm]	-16.5	-14.6
IIP3 [dBm]	-1.1	-3.2
Power [mW]	32.5	32.5
Area [μm^2]	70x90	70x90
Technology	0.35 µm SiGe	0.35 µm SiGe
FOM	0.46	0.62

for wideband LNAs a modified FOM expression that includes bandwidth, $FOM = (S_{21} \cdot BW)/(NF \cdot P_{DC})$, is used in Table 1.

A comparison of this work with other reported designs is shown in Figure 7. This figure plots the FOM for each design, against the feature size of the process in which it was fabricated. The feature size is used instead of f_T as some of the papers do not report f_T. The higher the FOM the better the design. The marker shape indicates the type of process. Our LNA has a higher FOM than all the designs except a few from more advanced foundry technologies.

5. SECOND GENERATION LNA

5.1 Design

Even though the first generation design achieved good S_{21} and NF it consumed a lot of power. This is because the first generation design had no power constraints during circuit synthesis, and resulted in excessive use of the power to meet the specified S-parameters and NF. Since power and bandwidth appears in the FOM expression, a second generation design was synthesized, in which both power and bandwidth were considered together with gain and NF. The constraints were S_{21} > 17 dB, NF < 3 dB, power < 35 mW and bandwidth > 3 GHz. Furthermore, since this is a wideband design (unlike [12]), the synthesis was constrained such that S_{21} and NF specifications were met over the entire bandwidth.

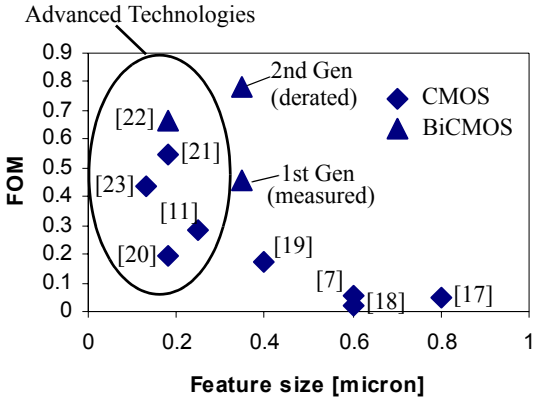

Figure 7.Wideband LNA Figure of Merit vs Lithographic feature size.

Furthermore, as the FOM is used for design comparison, its expression was set as an optimization goal, to achieve the best possible candidate design for comparison with the other wideband LNA in the literature.

In the amplifier circuit the second stage cancels the noise generated in the first stage noise. As the gain (*i.e.*, bias current) of the second stage is increased, more of the first stage noise is cancelled initially. Further increase in second stage bias current leads to increasing shot noise from the second stage. Thus, there is a trade-off between the noise added by the second stage and its cancellation of the first stage noise. This implies that maximum first stage noise cancellation doesn't necessarily lead to best overall NF.

The overall required gain is shared by the first CE stage (with resistive feedback) and the second CE stage (Q_2). The gain of the first CE stage is $\sim -g_{m1}R_F$ (equation 1) and that of through Q_2 is given by $-g_{m2}R_{out}$. Since $R_F \gg R_{out}$ (R_{out} = 50Ω), investing current into Q_1 rather than Q_2 in order to improve $-g_{m1}$ instead of $-g_{m2}$ will lead to the most power efficient way to achieve gain. This will affect the input matching of the circuit, therefore, $-g_{m1}$ should be changed to the extent that S_{11} is in the acceptable range. On the other hand, the gain through Q_2 needs to be close enough to the gain through the emitter follower to achieve some amount of noise cancellation. Thus, there is a trade-off between the gain, input matching, power and noise figure.

One of the main functions of the inclusion of the FOM optimization goal in the second generation synthesis was to get circuit with maximum FOM in presence of these trade-offs.

The constraints relating the devices used in the first generation design were removed to give the synthesis tool additional design freedom to achieve the best FOM design. These constraints were based on hand analysis (including the unity gain assumption for the emitter follower) which are more appropriate for manual design, than for a synthesis tool that uses a circuit simulator in its inner loop.

5.2 Simulation

The circuit has been synthesized in the same technology as the first generation LNA but is still awaiting fabrication. Therefore, for comparison, post-layout extracted simulations of both the first and second generation design are used. These simulation results are presented in Table 2. The FOM for the second generation is ~1.7x better than the first one. Since this circuit has not yet been fabricated, its simulated FOM was derated using the ratio of measured to simulation in Table 1. From this, the second generation LNA is expected to have a FOM of 0.78. This has been added to Figure 7, where it clearly has the best overall FOM.

For the second generation, entering the new synthesis constraints and running the circuit synthesis took a total of approximately 6 hours. Achieving such a performance improvement with very little design effort and in a very short time shows the strength of a FOM driven synthesis.

Table 2. Comparison of post layout simulation performance of 1st and 2nd generation wideband LNAs.

	Simulation 2nd Gen	Simulation 1st Gen
S_{21} [dB]	17.2	18
S_{11} [dB]	< -11.2	< -8
S_{12} [dB]	< -27.2	< -23.5
S_{22} [dB]	< -14	< -6.7
BW [GHz]	2.9	2.8
NF [dB]	< 2.8	< 2.7
ICP [dBm]	-18.4	-14.6
IIP3 [dBm]	-7.4	-3.2
Power [mW]	16.5	32.5
Area [μm^2]	118x78	70x90
Technology	0.35 μm SiGe	0.35 μm SiGe
FOM	1.05	0.62

The two primary differences between the first and second generation synthesis runs are the added power constraint and the FOM goal in the second run. A control synthesis run without the FOM goal was also run. While both the control and actual second generation synthesis runs met the target specifications, the run with the FOM goal achieved the best overall FOM, and is the one considered in Table 2.

5.3 Analysis

If incomplete cancellation of the noise from the first stage improves the overall circuit NF, as claimed in the previous section, then there should be two differences in the second generation circuit compared to the first generation one: (i) there should be a difference in the gains between the two noise cancellation paths; (ii) the second generation designs should have a better NF. Figure 8 compares magnitude of the difference in the gain between "Path 1" and "Path 2" (normalized to that for the first generation design) and the minimum NF across the two designs. It can be seen that the minimum NF has improved, even though the error in the noise cancellation path has increased for the second generation designs

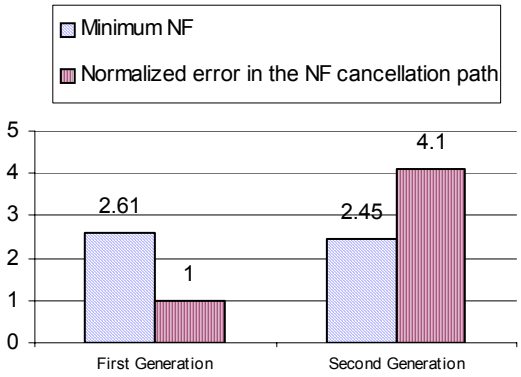

Figure 8. Comparing minimum NF and normalized error in first stage noise cancellation across the two generations.

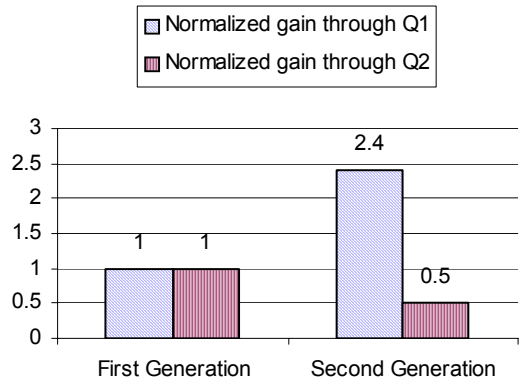

Figure 9. Comparison of gain from transistor Q_1 and Q_2 across the three designs.

Gains provided by the first CE stage (with resistive feedback) and the second CE stage (Q_2) for the two designs are normalized to the value for the second generation and compared in Figure 9. The second generation design has more gain for the first CE stage and less gain through second CE stage, compared to first generation design.This is one of the contributor to the lesser power consumption of the second generation design compared to the first one.

6. CONCLUSION

Two generations of a noise-canceling wideband LNA circuit have been synthesized in a 0.35 μm BiCMOS process. The first generation circuit was fabricated, and its measured performance was aggregated into a Figure of Merit (FOM) for comparison with other recently reported wideband LNAs. This circuit focused only on noise figure and gain, and had a FOM comparable to the best reported in the literature (fabricated in more advanced CMOS technologies). This FOM comparison showed the importance of considering all the specifications present in a FOM expression during synthesis. A second generation synthesis augmented the first generation constraints with the additional bandwidth and power constraints, as well as optimized for FOM. FOM optimization is important because it is the index of quality used for comparison. Simulation results of the second generation circuit improves the FOM by 1.7x compared to the first generation, potentially leading to the best overall wideband LNA when this design is fabricated. This improvement shows the benefits of FOM optimization driven synthesis in leading to the high performance designs within a day.

7. ACKNOWLEDGEMENT

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