Synchrophasors:

Definition, Measurement, and Application

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Abstract

The concept of using phasors to describe power system operating quantities dates back to 1893 and Charles Proteus Steinmetz's paper on mathematical techniques for analyzing AC networks[1]. More recently, Steinmetz's technique of phasor calculation has evolved into the calculation of real time phasor measurements that are synchronized to an absolute time reference. Although phasors have been clearly understood for over 100 years, the detailed definition of a time synchronized phasor has only recently been codified in the IEEE 1344 and the soon to be voted IEEE C37.118 Synchrophasor for Power Systems standards. This paper will review the concept of a phasor and examine the proposed IEEE standard as to "how" a synchronized phasor is to be defined, time stamped, and communicated. The paper will then examine the issues of implementing such measurements in the face of off-nominal frequency components, timing errors, sensor errors, and system harmonics. Simulations of various system transients and their phasor response will be presented. Finally, this paper will review the application of synchrophasors to observe power system dynamic phenomenon and how they will be used in the real-time control of the power system. Examples of system disturbances will be presented.

Introduction

As the electric power grid continues to expand and as transmission lines are pushed to their operating limits, the dynamic operation of the power system has become more of a concern and has become more difficult to accurately model. In addition, the ability to effect real-time system control is developing into a need in order to prevent wide scale cascading outages. For decades, control centers have estimated the "state" of the power system (the positive sequence voltage and angle at each network node) from measurements of the power flows through the power grid. It is very desirable to be able to "measure" the system state directly and/or augment existing estimators with additional information.

Alternating Current (AC) quantities have been analyzed for over 100 years using a construct developed by Charles Proteus Steinmetz in 1893 know as a phasor. On the power system, phasors were used for analyzing AC quantities assuming a constant frequency. A relatively new variant of this technique that synchronizes the calculation of a phasor to absolute time has been developed[2], which is known as synchronized phasor measurement or synchrophasors. In order to uniformly create and disseminate these synchronized measurements, several aspects of phasor creation had to be codified[3]. The following text spells out the definitions and requirements that have been established for the creation of synchronized phasor measurements.

Synchrophasor Definition

An AC waveform can be mathematically represented by the equation:

$$x(t) = X_m \cdot \cos\left(\phi + \int_{-\infty}^{t} \omega(\tau) \cdot d\tau\right) \qquad \text{Eqn. 1}$$

where: X_m = magnitude of the sinusoidal waveform
$\omega = 2 * \pi * f$ where f is the instantaneous frequency
ϕ = angular starting point for the waveform

Note that the synchrophasor is referenced to the cosine function. In a phasor notation, this waveform is typically represented as:

$$\overline{\mathbf{X}} = X_m \angle \phi$$

Since in the synchrophasor definition, correlation with the equivalent RMS quantity is desired, a scale factor of $1/\sqrt{2}$ must be applied to the magnitude which results in the phasor representation as:

$$\overline{\mathbf{X}} = \frac{X_m}{\sqrt{2}} \angle \phi$$

Adding in the absolute time mark, a synchrophasor is defined as the magnitude and angle of a cosine signal as referenced to an absolute point in time as shown in figure 1.

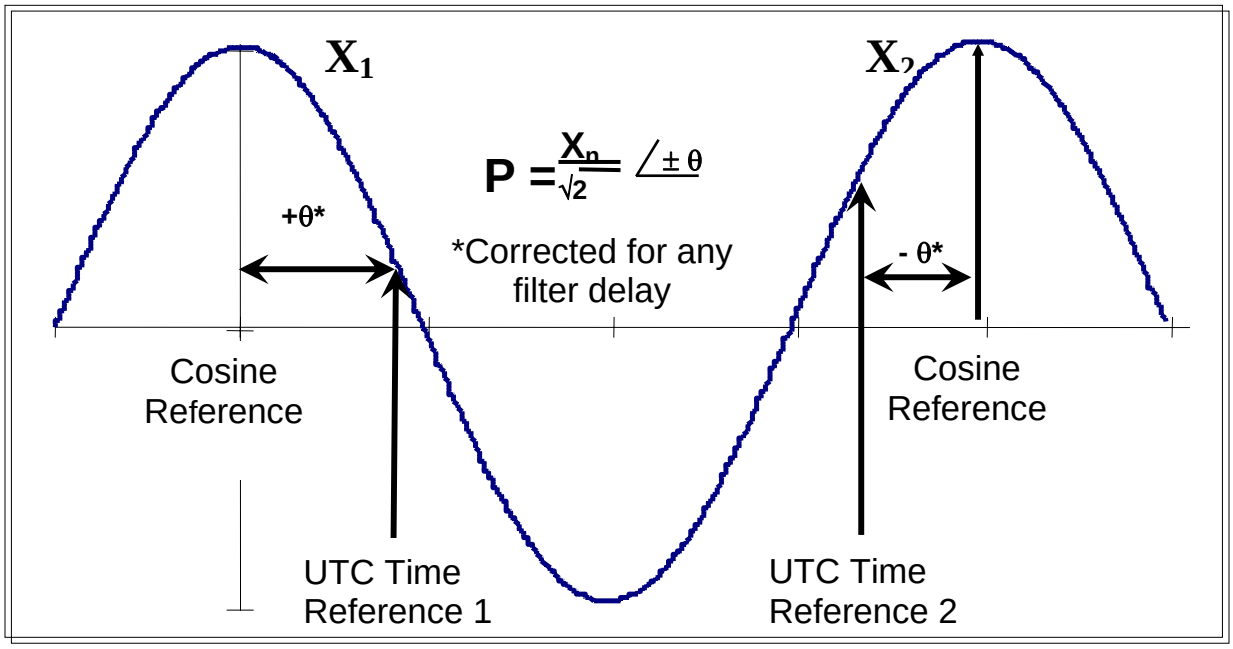

Figure 1
Synchrophasor Definition

In figure 1, time strobes are shown as UTC Time Reference 1 and UTC Time Reference 2. At the instant that UTC Time Reference 1 occurs, there is an angle that is shown as "+θ" and, assuming a steady-state sinusoid (i.e. – constant frequency), there is a magnitude of the waveform of X_1. Similarly, at UTC Time Reference 2, an angle, with respect to the cosine wave, of "-θ" is measured along with a magnitude or X_2. The range of the measured angle is required to be reported in the range of $\pm \pi$. It should be emphasized that the synchrophasor standard focuses on steady-state signals, that is, a signal where the frequency of the waveform is constant over the period of measurement.

In the real world, the power system *seldom* operates at exactly the nominal frequency. As such, the calculation of the phase angle, θ, needs to take into account the frequency of the system at the time of measurement. For example, if the nominal frequency of operating at 59.5Hz on a 60Hz system, the period of the waveform is 16.694ms instead of 16.666ms – a difference of 0.167%.

The captured phasors are to be time tagged based on the time of the UTC Time Reference. The Time Stamp is an 8-byte message consisting a 4 byte "Second Of Century – SOC", a 3-byte Fraction of Second and a 1-byte Time Quality indicator. The SOC time tag counts the number of seconds that have occurred since January 1, 1970 as an unsigned 32-bit Integer. With 32 bits, the SOC counter is good for 136 years or until the year 2106. With 3-bytes for the Fraction Of Second, one second can be broken down into 16, 777,216 counts or about 59.6 nsec/count. If such resolution is not desired, the proposed standard (C37.118) allows for a user-definable base over which the count will wrap (e.g. – a base of 1,000,000 would tag a phasor to the nearest microsecond). Finally, the Time Quality byte contains information about the status and relative accuracy of the source clock as well as indication of pending leap seconds and the direction (plus or minus). Note that leap seconds (plus or minus) are not included in the 4-byte Second Of Century count.

Synchronized Phasor Reporting

The IEEE C37.118 pending revision of the IEEE 1344 Synchrophasor standard proposes to standardize several reporting rates and reporting intervals of synchrophasor reporting. Specifically, the proposed required reporting rates are shown in Table 1 below.

Table 1
Synchrophasor Reporting Rates

System Frequency:	50 Hz		60 Hz				
Reporting Rates:	10	25	10	12	15	20	30

A given reporting rate must evenly divide a one second interval into the specified number of sub-intervals. This is illustrated in figure 2 where the reporting rate is selected at 60 phasors per second (beyond the maximum required value, which is allowed by the proposed new standard). The first reporting interval is to be at the Top of Second that is noted as reporting interval "0" in the figure. The Fraction of Second for this reporting interval must be equal to zero. The next reporting interval in the figure, labeled T0, must be reported1/60 of a second after Top of Second – with the Fraction of Second reporting 279,620 counts on a base of 16,777,216.

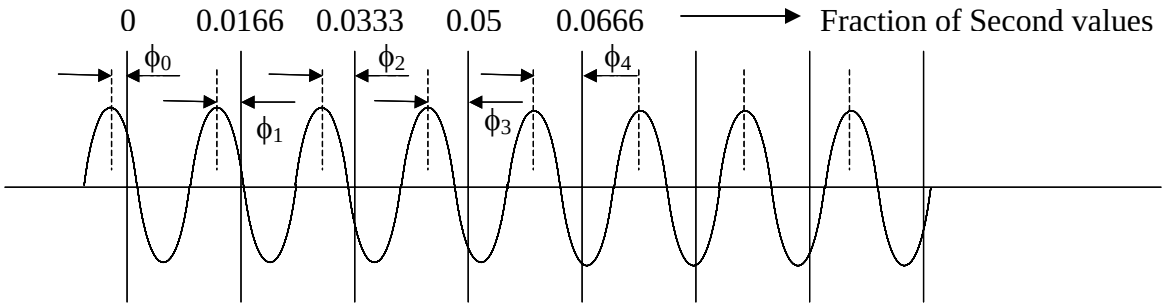

Figure 2
Synchronized Reporting Intervals

Performance Criteria

The measurement of a synchrophasor must maintain phase and magnitude accuracy over a range of operating conditions. Accuracy for the synchrophasor is measured by a value termed the Total Vector Error or TVE. TVE is defined as the square root of the difference squared between the real and imaginary parts of the theoretical actual phasor and the estimated phasor – ratioed to the magnitude of the theoretical phasor and presented in percent (equation 2).

$$\varepsilon = (\sqrt{[((X_r(n) - X_r)^2 + (X_i(n) - X_i)^2) / (X_r^2 + X_i^2)]}) * 100 \qquad \text{Eqn. 2}$$

where: X_r and X_i represent the theoretical exact synchrophasor

and: $X_r(n)$ and $X_i(n)$ represent the estimated synchrophasor

In the most demanding level of operation (Level 1), the proposed synchrophasor standard specifies the a Phasor Measurement Unit (PMU) must maintain less that a 1% TVE under conditions of ±5 Hz off-nominal frequency, 10% Total Harmonic Distortion, and 10% out-of-band influence signal distortion. The next section examines some issues that result from implementation of the phasor measurement using the classical Discrete Fourier Transform.

Off-nominal frequency effect in a classical phasor estimator

For one variation of a classical one-cycle, N samples-per-cycle algorithm, an rms phasor is estimated by the following centered computation:

$$\hat{\mathbf{X}} = \frac{\sqrt{2}}{N} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}-1} x\left[\Delta t\left(k+1/2\right)\right] \cdot e^{-j(k+1/2)\frac{2\pi}{N}}$$

$$\hat{\mathbf{X}} = \text{one - cycle phasor estimate} \qquad \text{Eqns. 3}$$

$$\Delta t = \frac{1}{N \cdot f_{nominal}}$$

$$x\left[\Delta t\left(k+1/2\right)\right] = \text{current or voltage sample taken at t} = \Delta t\left(k+1/2\right)$$

It is assumed that N is even. A 1/2 sample offset is used in both the sampling and the complex exponential to achieve exact centering around the on-time mark.

Suppose that the samples are from a single frequency component, not necessarily at the nominal frequency, with a phase angle measured with respect to t=0:

$$x\left[\Delta t\left(k+1/2\right)\right]=\sqrt{2}Real\left[\overline{\mathbf{X}}\cdot e^{j(k+1/2)\frac{2\pi}{N}\cdot\frac{f}{f_{nominal}}}\right]$$

$\overline{\mathbf{X}}$ = actual, "true", phasor value of the sequence of samples

$f_{nominal}$ = nominal frequency base for fixed rate sampling

f = actual frequency of the sequence of samples

Eqns. 4

By substituting equations 4 into equations 1, and simplifying, it can be shown that the one-cycle phasor estimate is related to the true value as follows:

$$\hat{\mathbf{X}}=A\cdot\overline{\mathbf{X}}+B\cdot\overline{\mathbf{X}}^{*}$$

$\overline{\mathbf{X}}^{*}$ = complex conjugate of $\overline{\mathbf{X}}$

$$A=\frac{\sin\left[\pi\cdot\left(\frac{f}{f_{nominal}}-1\right)\right]}{N\cdot\sin\left[\frac{\pi}{N}\cdot\left(\frac{f}{f_{nominal}}-1\right)\right]}$$

$$B=\frac{\sin\left[\pi\cdot\left(\frac{f}{f_{nominal}}-1\right)\right]}{N\cdot\sin\left[\frac{2\pi}{N}+\frac{\pi}{N}\cdot\left(\frac{f}{f_{nominal}}-1\right)\right]}$$

Eqns. 5

The expressions for A and B may seem daunting, but it is possible to draw some conclusions from them. First, it can be seen that as the actual frequency approaches the nominal frequency, A approaches 1 and B approaches zero, so that the phasor estimate is exactly equal to the true phasor value:

when $f = f_{nominal}$ then $A=1, B=0$

and $\hat{\mathbf{X}}=\overline{\mathbf{X}}$

Eqns. 6

In other words, when the actual frequency is equal to the nominal, the centered window used in equations 3 produces a phasor estimate that is free from any phase or gain error.

For off-nominal frequency, equations 5 indicate there is both phase and magnitude error. As the actual frequency moves away from the nominal, A drops away from 1, and B moves away from zero, with a positive value for a frequency increase, and a negative value for a frequency decrease, introducing a distortion.

To get a better idea of what the nature of the distortion is, it is useful to recast equations 5 in terms of separate real and imaginary components:

$$\hat{\mathbf{X}} = A \cdot \overline{\mathbf{X}} + B \cdot \overline{\mathbf{X}}^{*}$$
$$Real\left[\hat{\mathbf{X}}\right] = \left[A + B\right] \cdot Real\left[\overline{\mathbf{X}}\right] \qquad \text{Eqns. 7}$$
$$Imag\left[\hat{\mathbf{X}}\right] = \left[A - B\right] \cdot Imag\left[\overline{\mathbf{X}}\right]$$

Equations 7 represent an ellipse. One way to see it is to recast the equations into a more recognizable form:

$$\frac{Real\left[\hat{\mathbf{X}}\right]}{\left[A + B\right]} = Real\left[\overline{\mathbf{X}}\right]$$
$$\frac{Imag\left[\hat{\mathbf{X}}\right]}{\left[A - B\right]} = Imag\left[\overline{\mathbf{X}}\right] \qquad \text{Eqns. 8}$$
$$\left[\frac{Real\left[\hat{\mathbf{X}}\right]}{\left[A + B\right]}\right]^2 + \left[\frac{Imag\left[\hat{\mathbf{X}}\right]}{\left[A - B\right]}\right]^2 = \left[Real\left[\overline{\mathbf{X}}\right]\right]^2 + \left[Imag\left[\overline{\mathbf{X}}\right]\right]^2 = \left|\overline{\mathbf{X}}\right|^2$$

Thus it can be seen that the locus of all phasor estimates, for a given phasor amplitude and variable phase angle, is an ellipse with the major and minor axes aligned with the axes of the complex plain. The real and imaginary intercepts of the ellipse are given by:

$$RealIntercept = \left[A + B\right] \cdot \left|\overline{\mathbf{X}}\right| \qquad \text{Eqns. 9}$$
$$ImagIntercept = \left[A - B\right] \cdot \left|\overline{\mathbf{X}}\right|$$

As can be seen from equations 3 and 7, the eccentricity of the ellipse worsens as the frequency deviation grows. It can also be seen for small positive frequency deviations that the major axis of the ellipse is aligned with real axis. For small negative frequency deviations the major axis of the ellipse is aligned with the imaginary axis.

Further examination of equations 5 and 9 also reveals that the magnitude of the phasor estimate "shrinks", because A is always less than 1 for off-nominal operation. Figure 3 shows the outline of the rotating phasor for a 55Hz input signal.

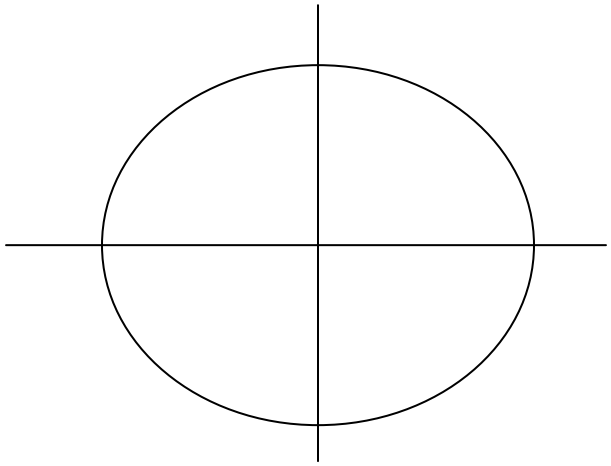

Figure 3
Classic Fourier Response for 55Hz Input

Out-of-Band Interfering Signals

Out-of-band signals are those signals occurring on the power system that typically fall in the 0 to 60 Hz range but specifically, those signals that will be aliased if the reporting phasor data rate is too slow for the phenomenon being observed. For example, a typical power system swing will operate in the 1 to 3 Hz range. In order to "observe" a 3 Hz signal, the phasor reporting rate must be greater than twice the 3 Hz swing frequency or 10 phasors per second (the lowest proposed standard rate). More specifically, if there is an interfering signal of 10 Hz with 10% magnitude modulation on the AC waveform (see figures 4A and 4B for examples) and the reporting rate on the PMU is still set for 10 phasors/second, the proposed standard specifies that influence from the interfering signal shall not raise the TVE above the 1% level.

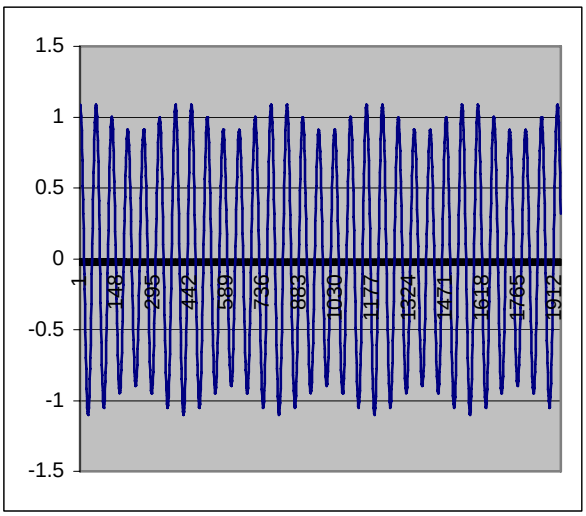

Figure 4A
10 Hz Multiplicative Interfering Signal

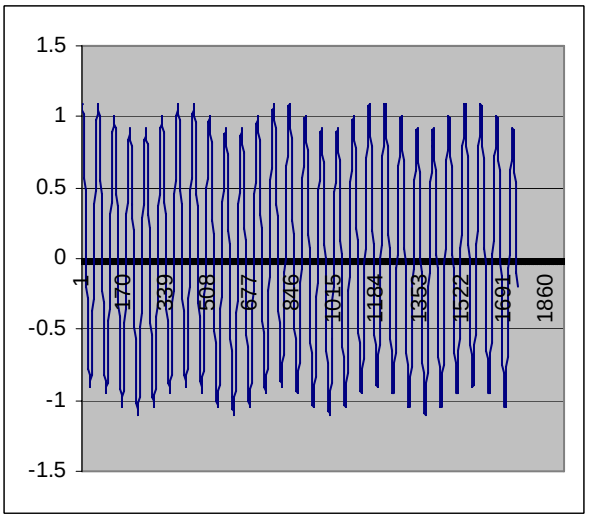

Figure 4B
10 Hz Additive Interfering Signal

System Architecture

As the implementation of phasor measurement proliferates around the world, there are a number of architectural considerations that need to be addressed. First is physical location. It should be noted that, given PMUs with synchronized current measurement capability, complete observability could be obtained by locating PMUs at alternate nodes in the power system grid. Current flows from a substation could be used to estimate the voltage at remote stations by calculating the I_1*Z_1 voltage drop along the line. In general, it is expected that these values will be correlated through a process equivalent to existing state estimators – only 20 times faster.

The next architectural issue to address is that of communications channels and bandwidth. Bandwidth is driven by the user's appetite for data. For example, choosing a phasor reporting rate of 60 phasors/sec for a voltage, 5 currents, 5 Watt measurements, 5 Var measurements, frequency, and rate of change of frequency – all reporting as floating point values – will require a bandwidth of 64,000 bps. On the other hand, a data reporting rate of 12 phasors/second for 1 voltage, 5 currents, and frequency – reported in 16 bit integer format – can be accommodated over a 4800 bps channel.

In making the choice of channel bandwidth, both present and future requirements should be considered. In particular, the possibility of future closed loop control should be considered in as much as the speed of the control is a function of the available bandwidth.

The next architectural choice is that of a physical communication channel. This choice is driven by several functional requirements, namely:

- Bandwidth required
- System availability requirements
- Data availability (i.e. – how many lost packets are tolerable)
- End-user data distribution

These requirements drive a topological architecture as shown in figure 5.

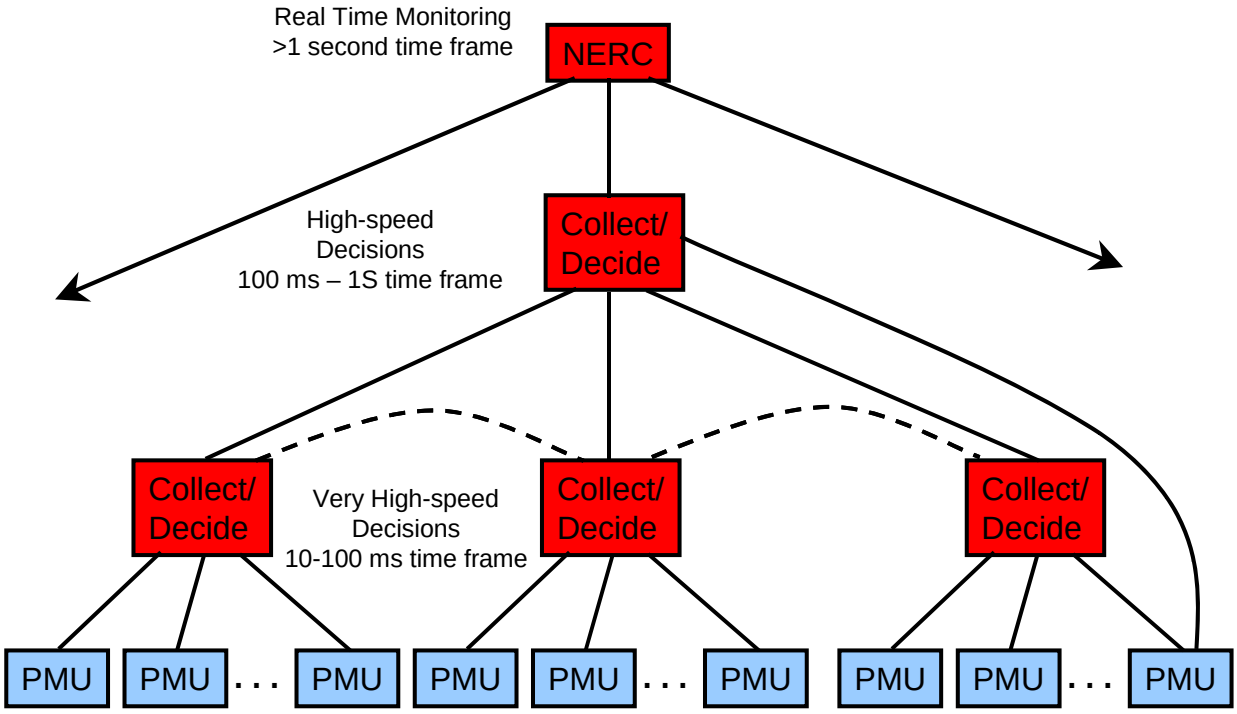

Figure 5
Synchrophasor Data Collection Topology

In this architecture, there are several data paths shown each of which will require different size data pipes and characteristics and there are multiple collection and decision levels that address different operational constraints – primarily that of speed of response in the case where closed-loop control is involved.

The first line data path is the one from the PMU to a first level Phasor Data Concentrator (PDC) where the data is received and sorted by time tag from multiple PMUs. Choices for this link include serial data operating with data rates from 9600 bps to 57,600 bps and Ethernet operating at either 10 or 100 MB. Note that the Synchrophasor standard specifies the data format for the PMU to PDC data link. In many cases, communication redundancy may be required or multiple consumers of data may exist. If serial data links are used, either multiple output ports from the

PMU must be supported or a multi-drop serial link must be employed. When supporting multiple consumers through Ethernet, either multiple connections must be supported by the PMU or the PMU can support multicast data transmission. A particularly useful Ethernet construct that facilitates point to multi-point communications is that of the Virtual LAN or VLAN. The VLAN construct adds a 12 bit VLAN identifier to every Ethernet data packet. Ethernet switches that support VLAN can read the VLAN tag and switch the data packet to all ports that are connected on the same VLAN. Since the switching is done at the data link layer, there is a minimum time delay in switching this data through a network.

Data sharing between PDCs at the same hierarchical level as well as aggregation PDCs at higher levels will be required. It is expected, however, that data exchange between PDCs will take place at lower data rates of about 10 synchrophasors/second. Although the data rate is 6 times slower (60 vs. 10 phasors per second), aggregated data streams may contain data from 16 to 32 PMUs. For these aggregated data streams, communication transports such as T1, SONET, and Ethernet should be considered.

One other area to address architecturally is that of data exchange between the PDC and the application software. In as much as the application SW will most likely be multi-vendor, architectural guidelines suggest that a standard generic interface would best serve the industry. The recently released IntelliGrid Architecture[4] addresses this issue and recommends the Generic Interface Definition (GID) High Speed Data Access interface for this application. In a practical implementation, this is implemented via the OLE for Process Control standard (OPC). An implementation of this PDC architecture is shown in figure 6.

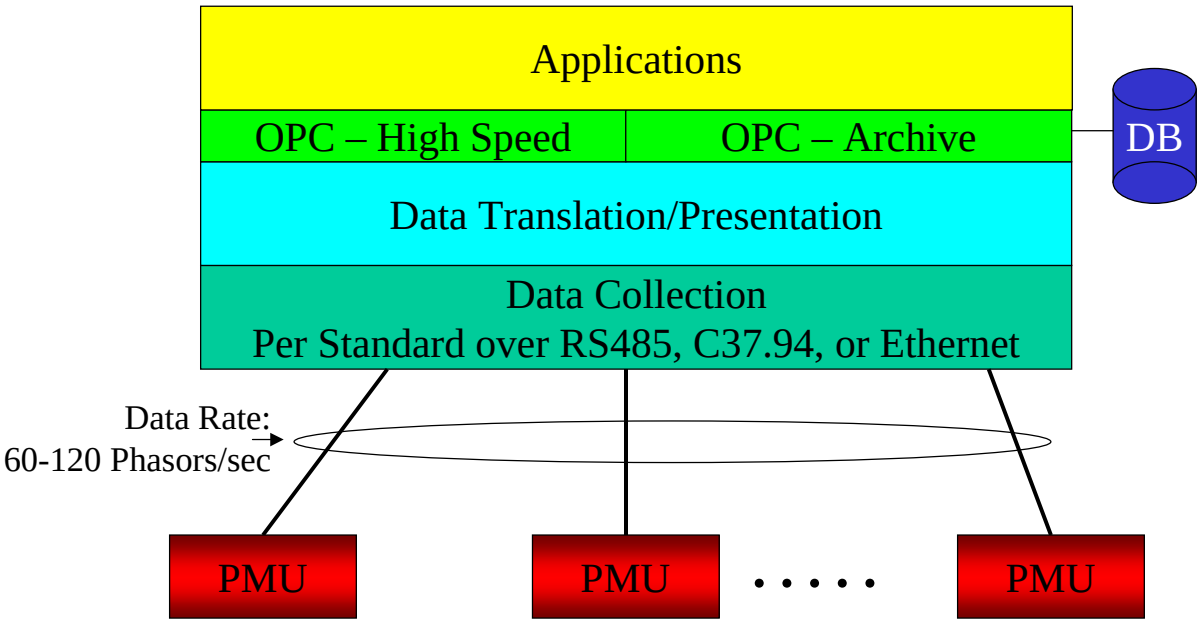

Figure 6
Phasor Data Concentrator Architecture

Applications

The utility industry has taken a 2-phase approach to the development of applications in the synchrophasor domain. Phase 1 (where most of the world is presently operating) is a data visualization stage / problem identification phase. Visualization tools have been developed that look at dynamic power flow, dynamic phase angle separation, and real-time frequency and rate of change of frequency displays. Figure 7 is an example of a real-time plot of the voltage phasor. The contour of the surface indicates instantaneous voltage magnitude and the color indicates phase angle with respect to a user-chosen reference angle. At a glance, any depression indicates a Var sync and the color variation (blue to red) indicated instantaneous power flow. In a control room, this graphic could be animated to show undulations in real time due to power swings.

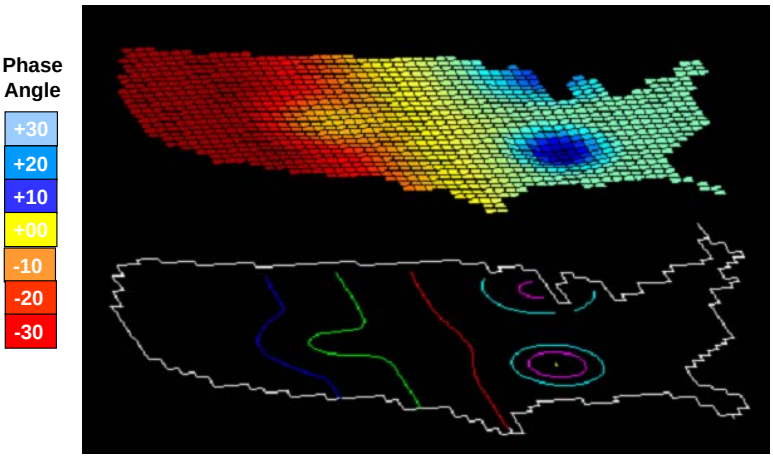

Figure 7
Wide Area Voltage View Example

Other visualization tools that have been developed include a synchroscope view of all the phase angles, frequency and rate of change of frequency plots, oscillation frequency and damping coefficient plots, and general power flow plots.

Phase 2 involves development of a phasor based closed loop control system (figure 8). In such a system, aggregated measurements from one or more PDCs is passed to a "decision algorithm" that computes, in real time, a control strategy and issues the appropriate outputs to the controllable devices located around the system. Control speeds will need to vary – based on the severity of the disturbance. If a potentially unstable power swing was detected, the controller has between ¼ and ½ second to compute and initiate a control action. On the other hand, if the function being implemented is a system-wide automatic Voltage control algorithm, then a control

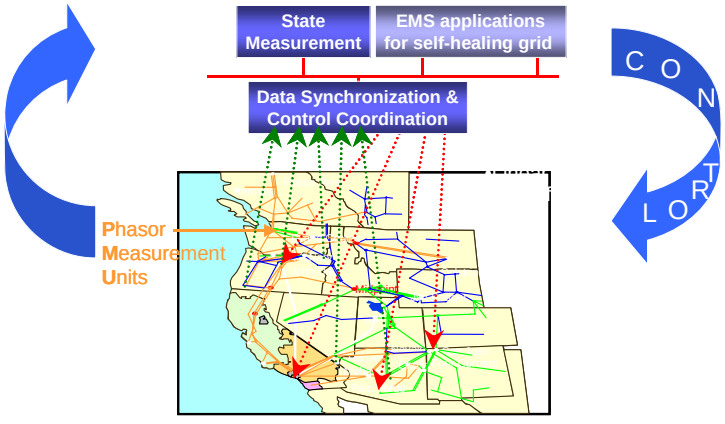

Figure 8
Closed Loop Power System Control

in the multiple second range is quite adequate. Other potential control algorithms include inter-area oscillation damping, enhanced power system stabilization, automatic voltage regulation, out of step tripping and blocking, and Voltage collapse detection and mitigation.

Conclusions

The technology and necessary standards for the measurement and communication of synchronized phasor measurements are becoming available across a range of operating platforms. The need and potential applications for this technology is evolving in parallel will be needed in order to maintain stable operation of the electric power grid of the future.

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Biographies

Dr. William Premerlani is employed at GE's Global Research Center in Schenectady, New York and a holder of over 35 patents. His current research interest is in phasor measurement, advanced algorithms for diagnostics and protection, with applications to motor diagnostics and power system relaying. Other recent work included object - oriented technology, with application to achieving interoperability among communicating intelligent devices in power systems. He is a co-author of the popular textbooks: "**Object Oriented Modeling and Design"** and **"Object-Oriented Modeling and Design for Database Applications".**

Dr. Bogdan Kasztenny received his M.Sc. and Ph.D. degrees from the Wroclaw University of Technology (WUT), Poland. He joined the Department of Electrical Engineering of WUT after his graduation. Later he was with the Southern Illinois and Texas A&M Universities. Currently, Dr. Kasztenny works for GE Power Management as the Chief Application Engineer and a Project Leader for the Universal Relay family of protective relays. Bogdan is a Senior Member of IEEE, has published more than 100 papers and holds several patents on protection and control.

Mark Adamiak received his Bachelor of Science and Master of Engineering degrees from Cornell University in Electrical Engineering and an MS-EE degree from the Polytechnic Institute of New York. Mark started his career with American Electric Power (AEP) in the System Protection and Control section where his assignments included R&D in Digital Protection, relay and fault analysis, Power Line Carrier and Fault Recorders. In 1990, Mark joined General Electric where his activities have ranged from development, product planning, and system integration. In addition, Mr. Adamiak has been actively involved in developing the framework

for next generation relay communications and was the Principle Investigator on the Integrated Energy and Communication System Architecture (IECSA) project. Mark is a Senior Member of IEEE, past Chairman of the IEEE Relay Communications Sub Committee, and a member of the US team on IEC TC57 - Working Group 10 on Substation Communication.