

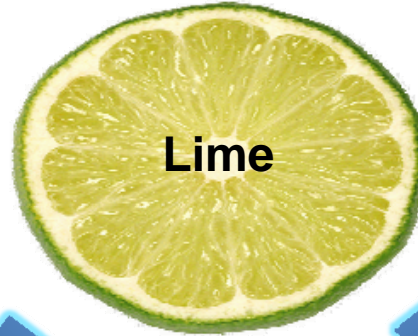
A Stall-Free Real-Time Garbage Collector for FPGAs

David F. Bacon, Perry Cheng, **Sunil Shukla**

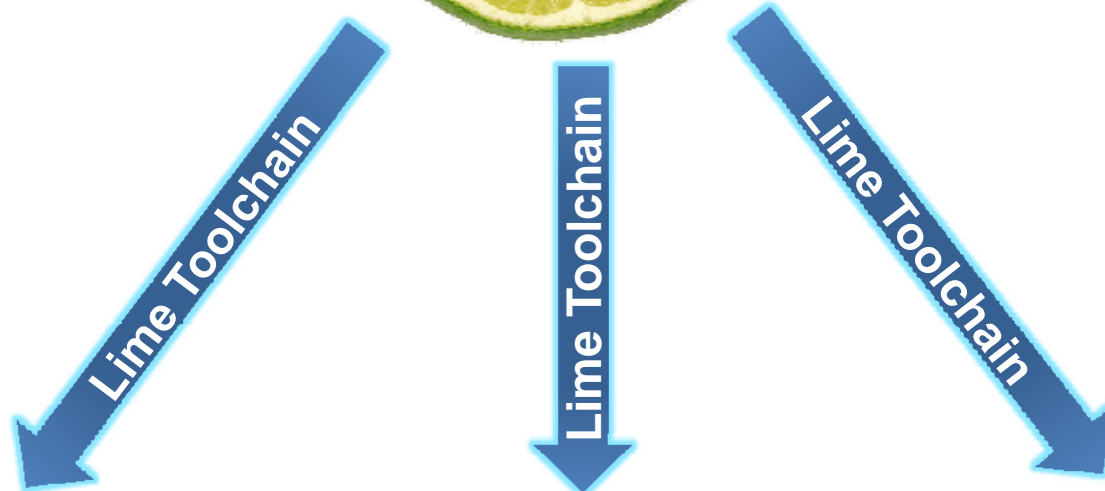
<http://www.research.ibm.com/liquidmetal/>

Motivation: Liquid Metal

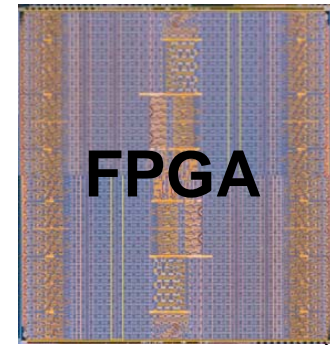
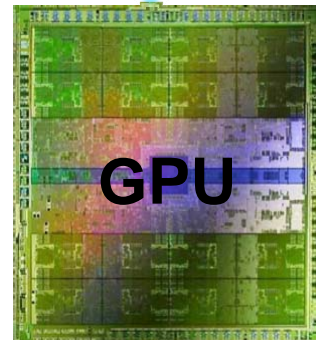
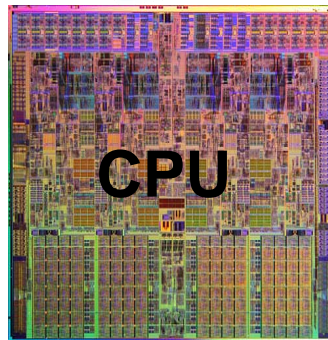
Language



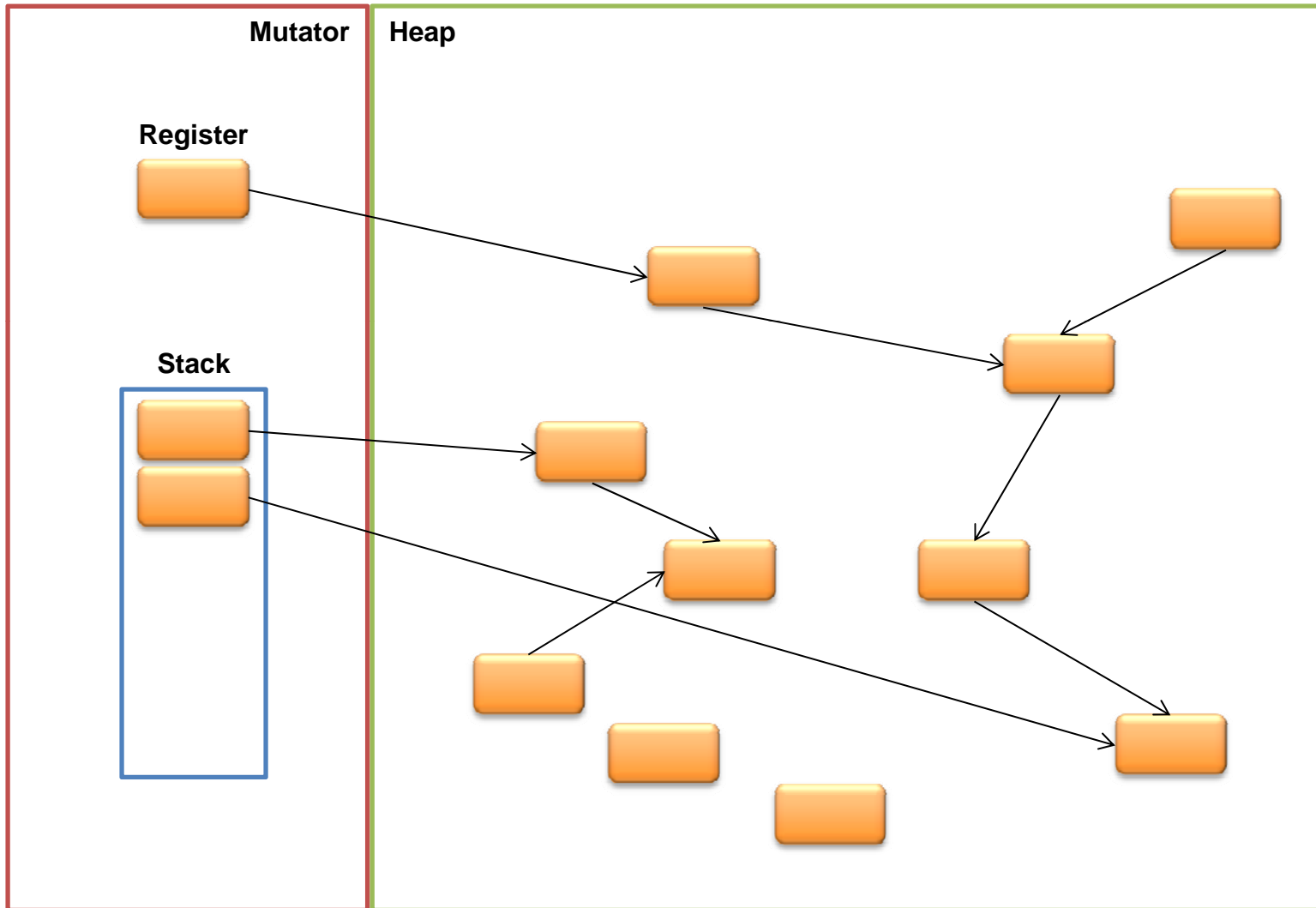
Toolchain =
IDE +
Compiler +
Debugger



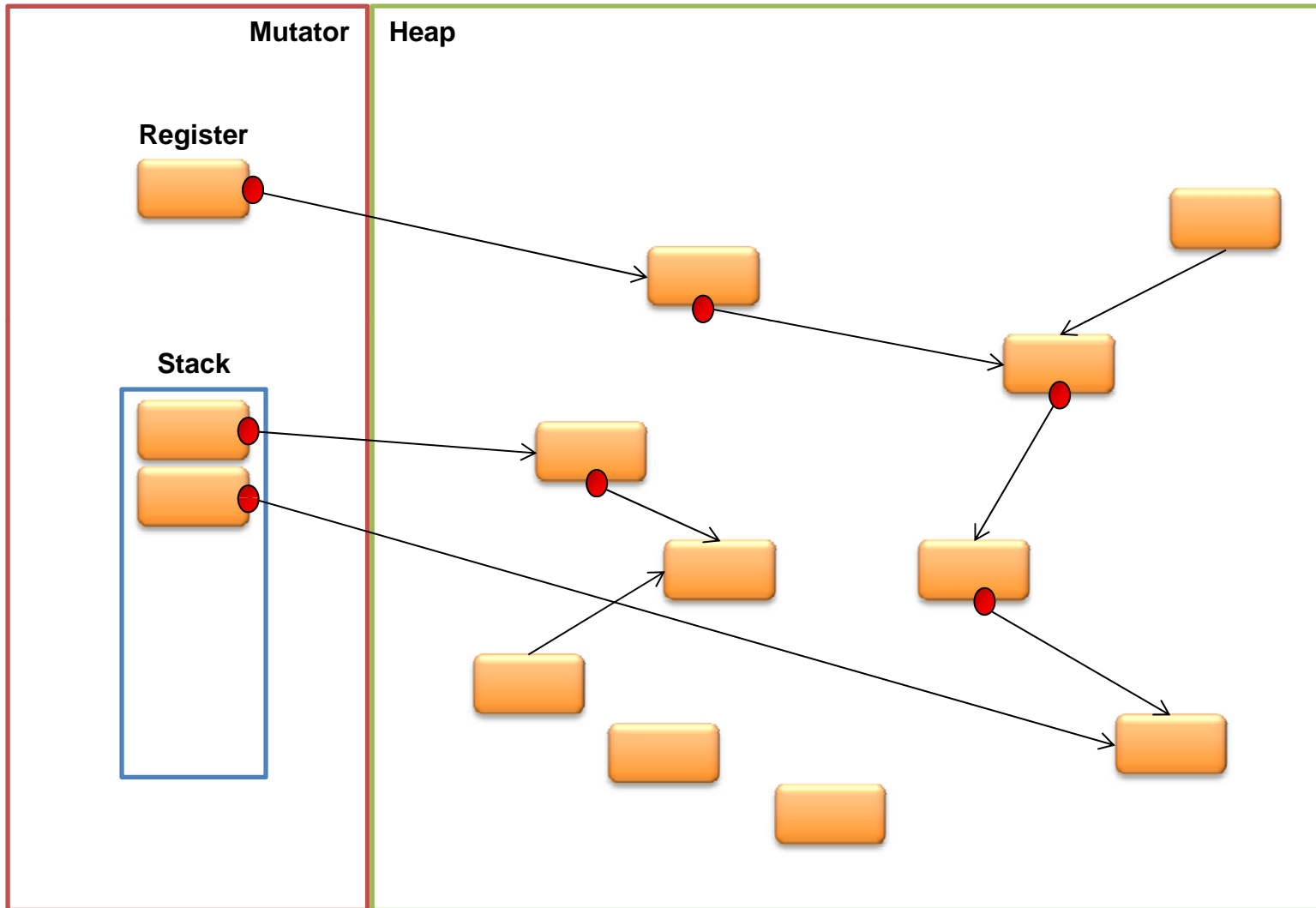
Platform =
Hardware +
Runtime



What is Garbage Collection?

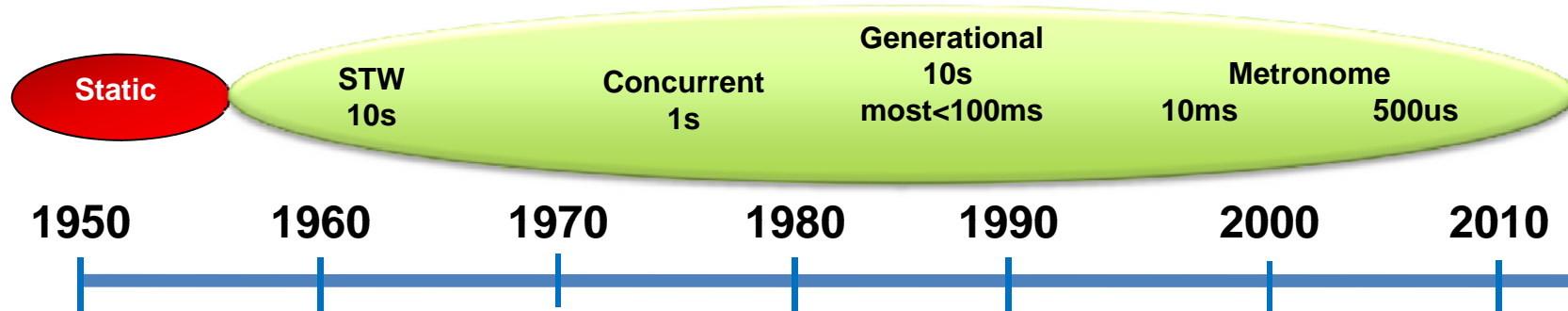


What is Garbage Collection?

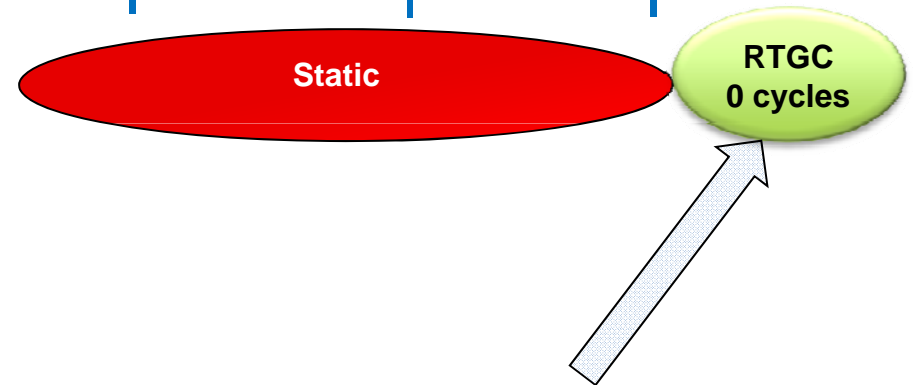


Memory Management: CPU vs. FPGA

CPU



FPGA

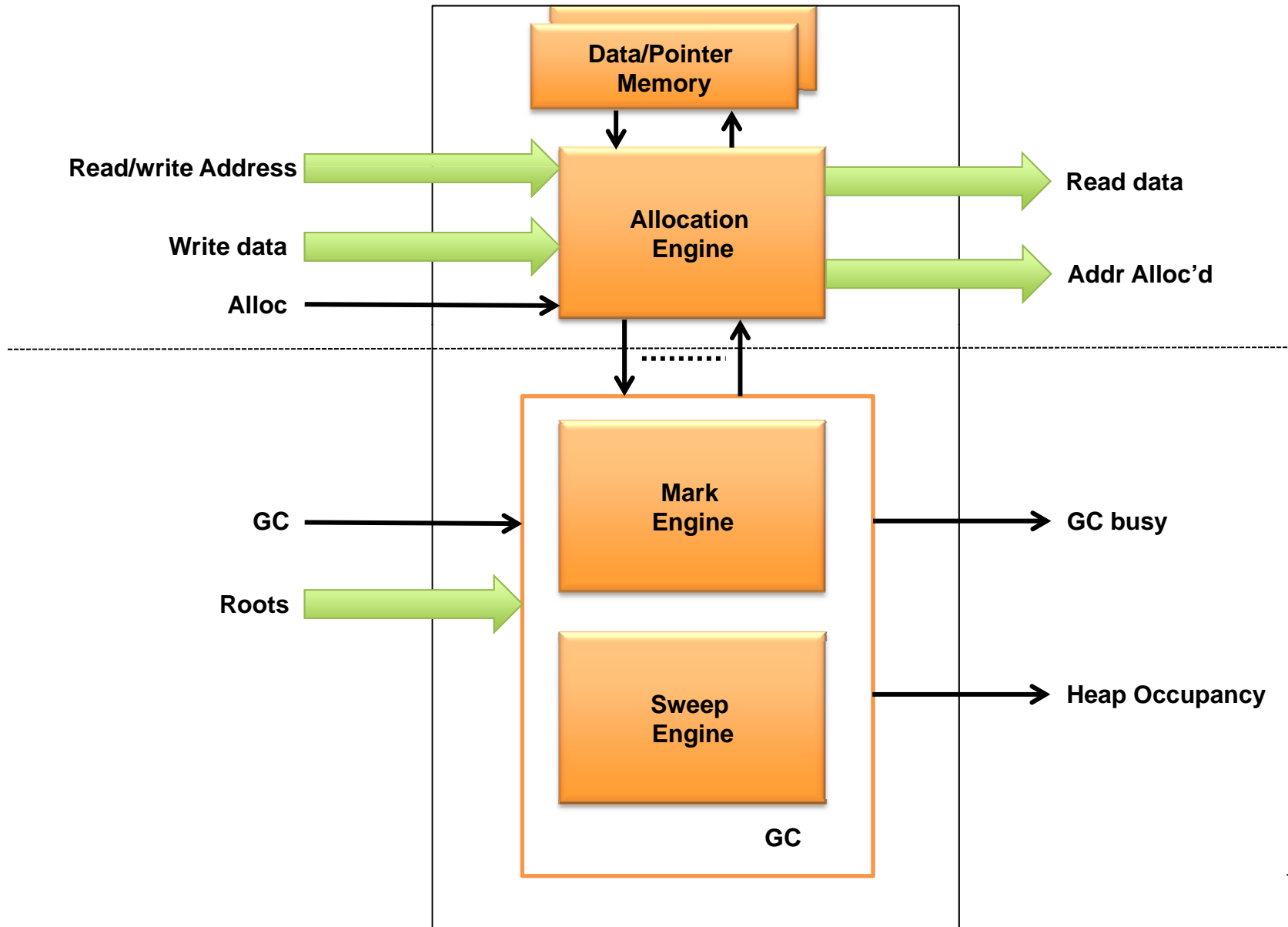


PLDI'12: "And Then There Were None: A Stall-Free Real-Time Garbage Collector for Reconfigurable Hardware"
- D. Bacon, P. Cheng, S. Shukla

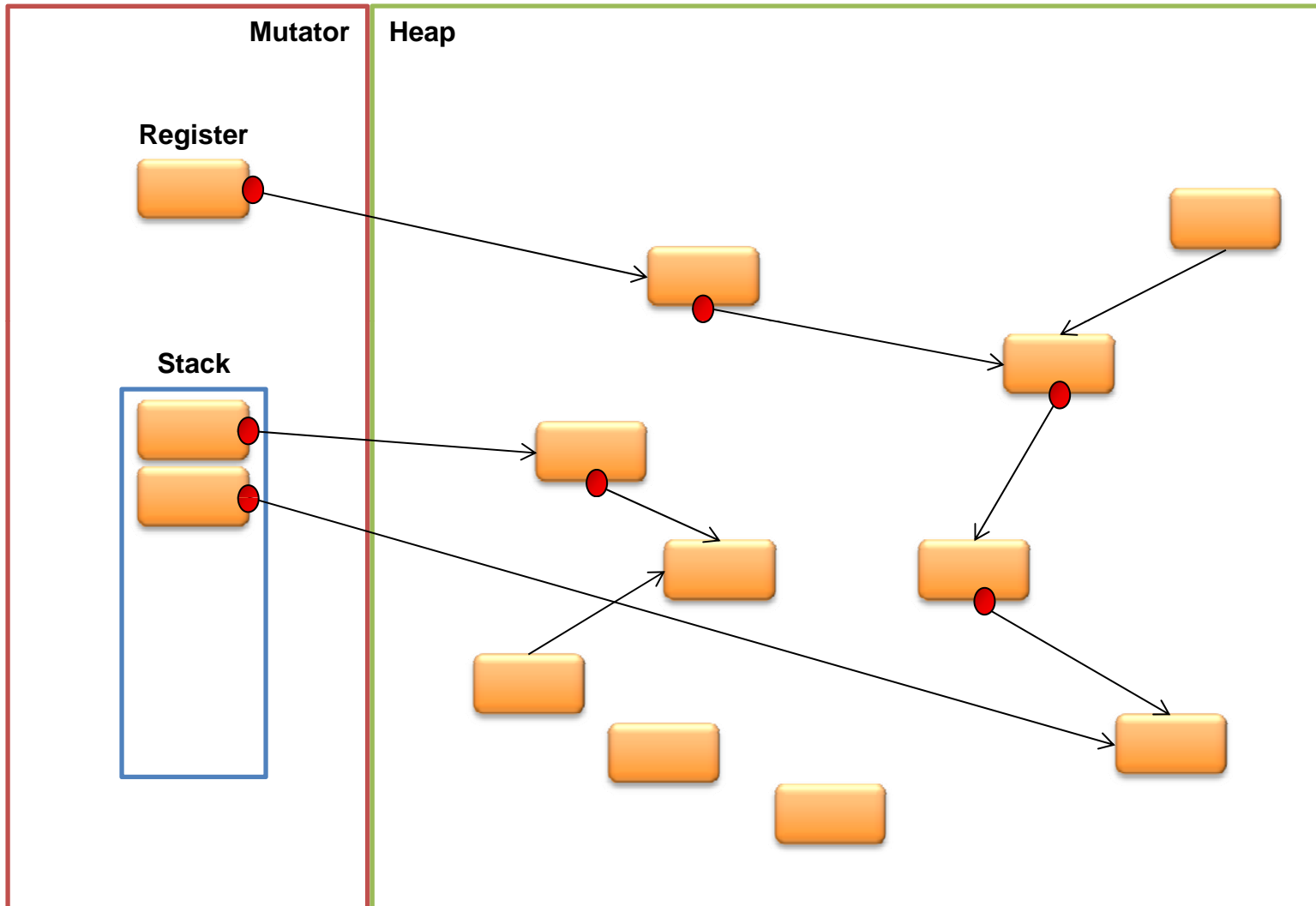
Heap - features

- Homogeneous objects
 - 2 pointer fields
 - Programmable number of data fields
- Minimum mutator utilization (MMU) of 100%
- Validated analytical bounds on the WCET
- Implemented in Verilog

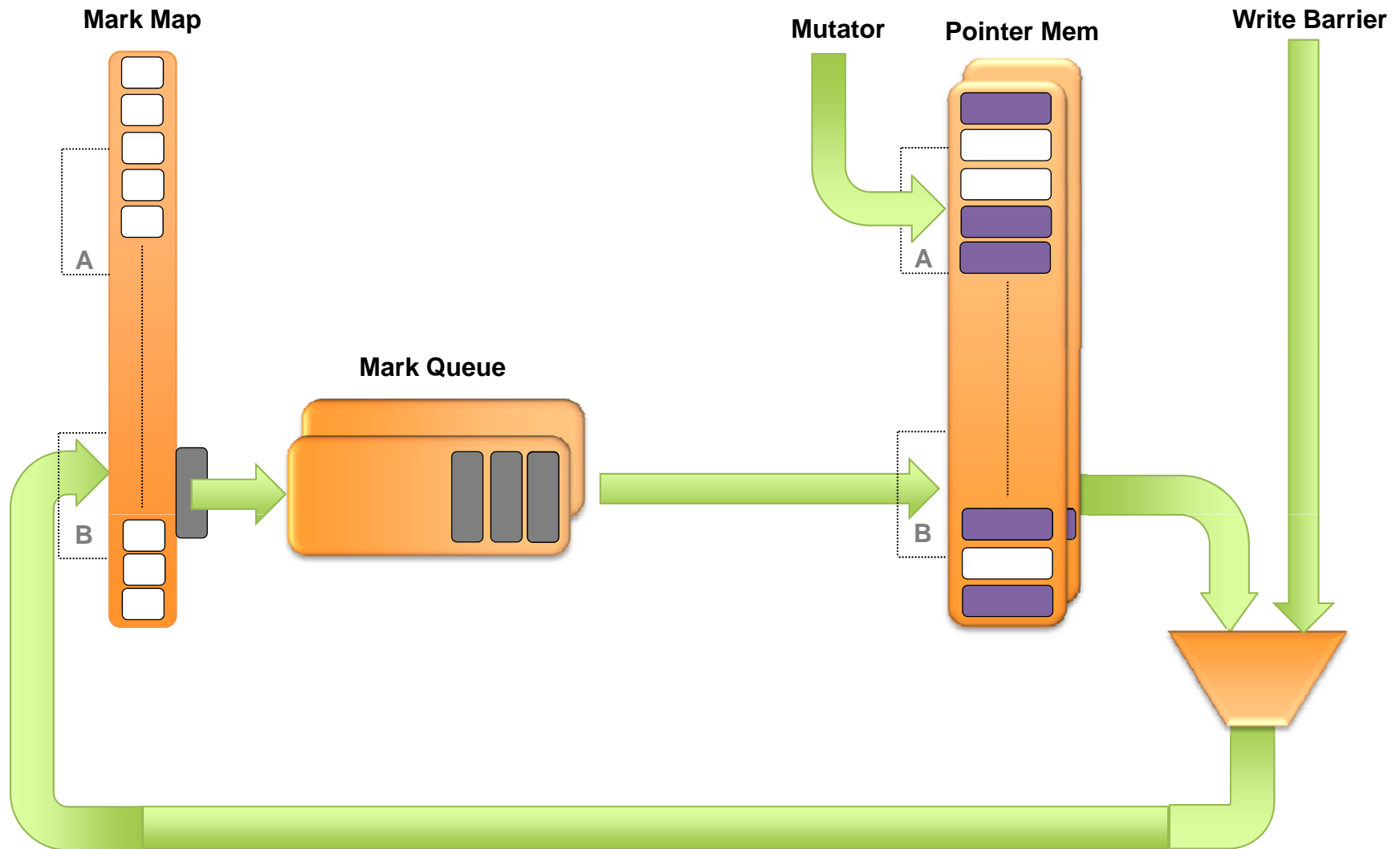
Heap - Block Diagram



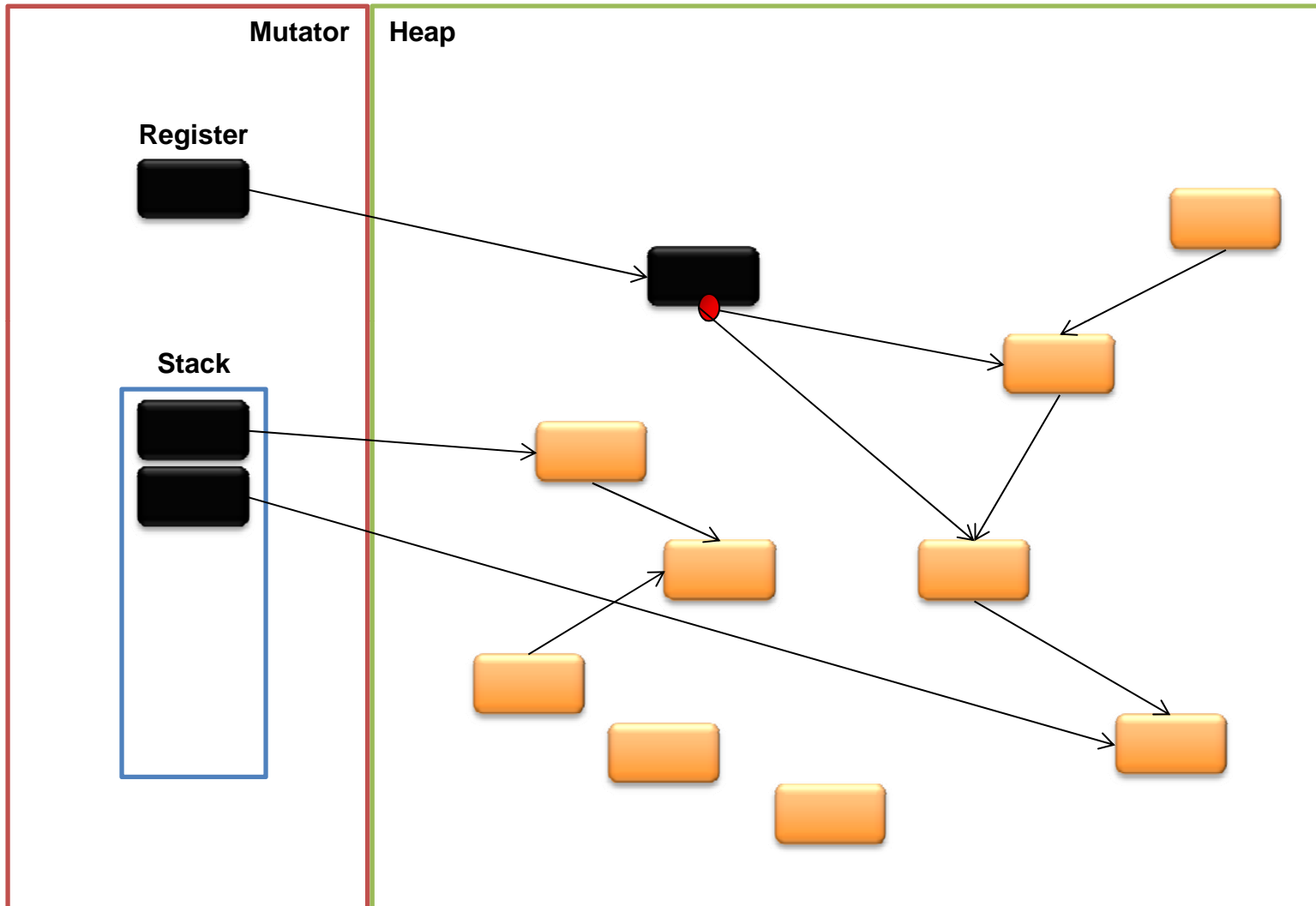
Marking



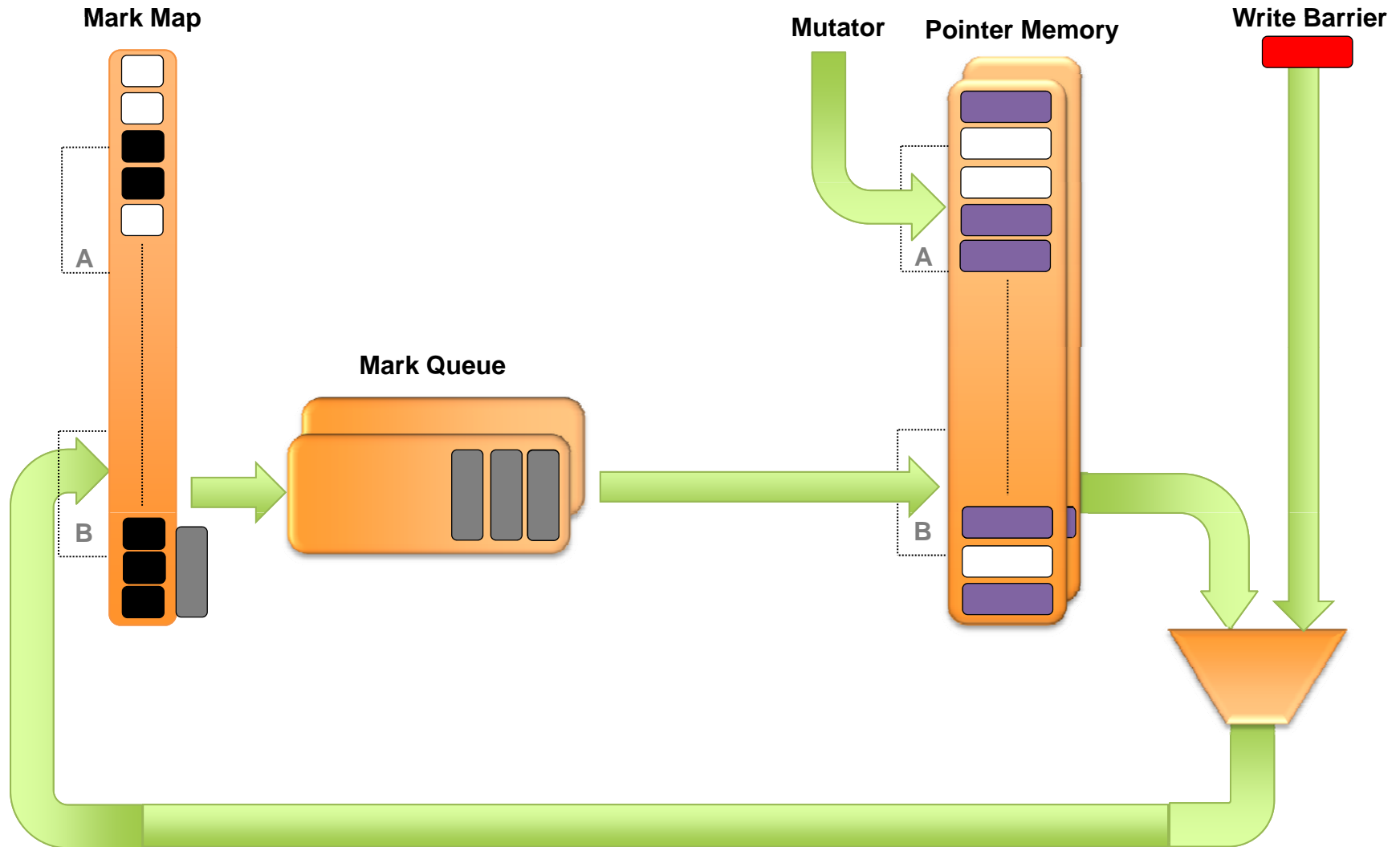
Mark Engine



Mark Engine: Write Barriers

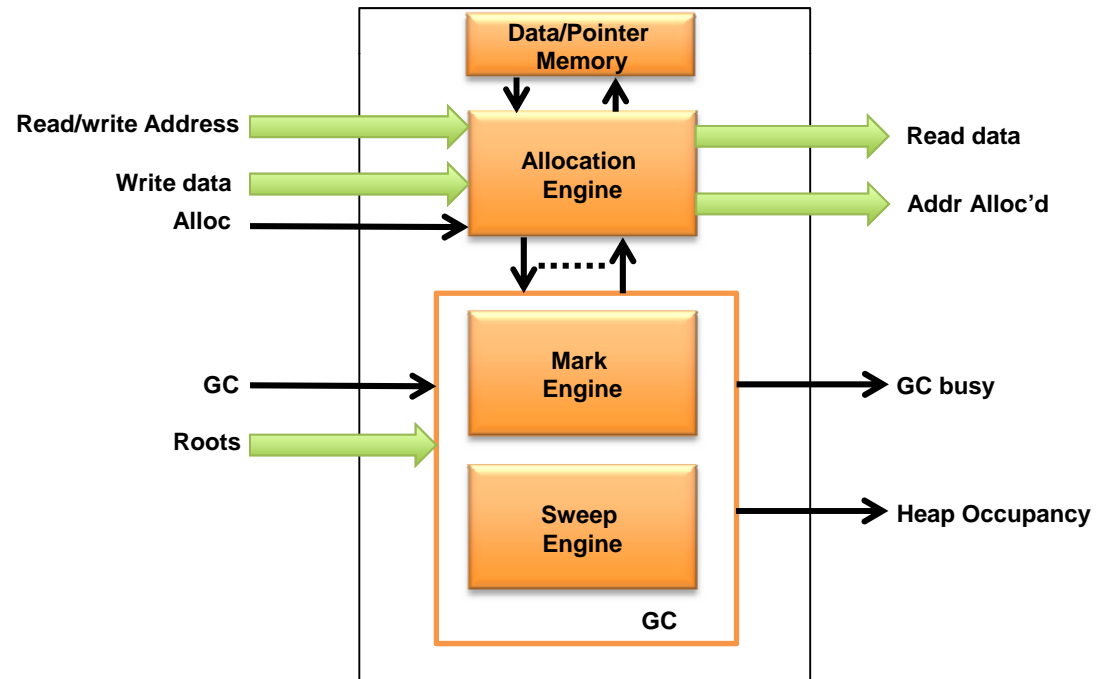


Mark Engine: Write Barriers



Evaluation

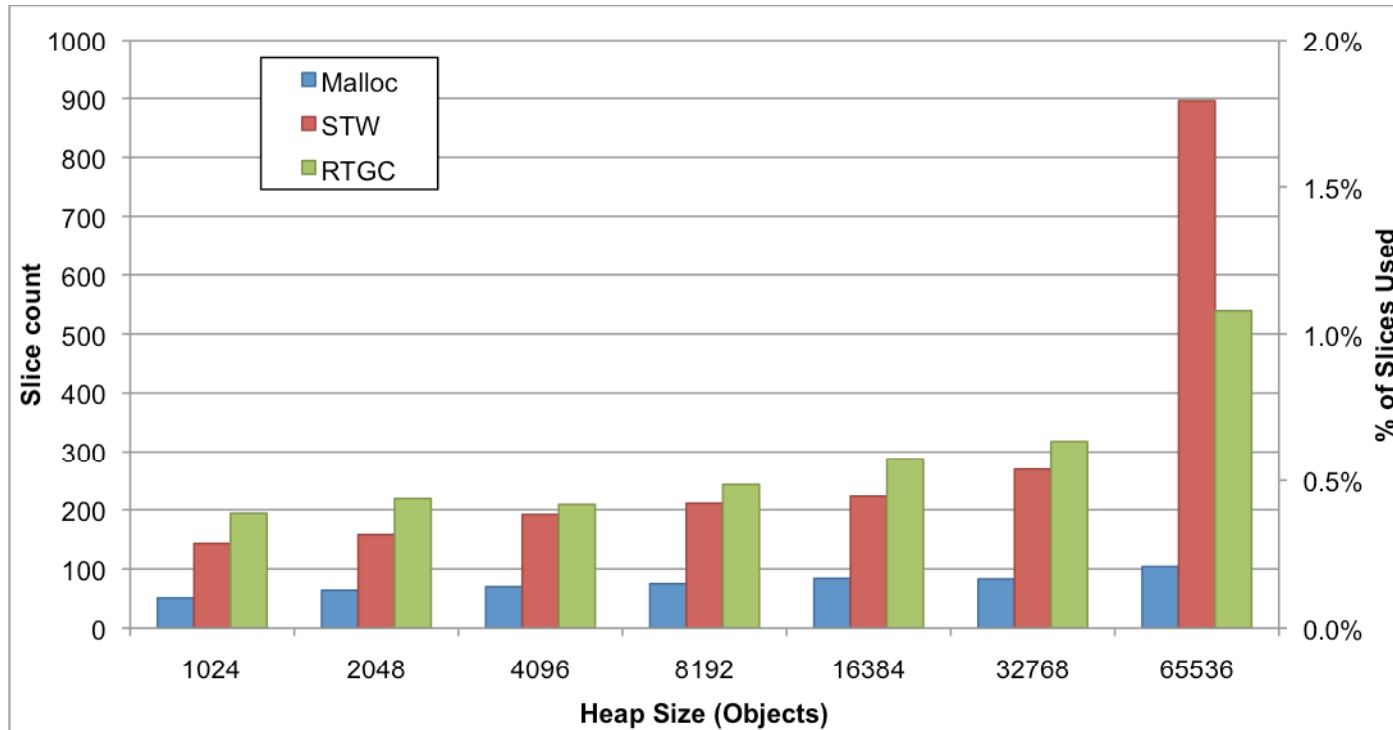
1. Static memory manager (“Malloc”)
2. Stop-the-world collector (“STW”)
3. Concurrent collector (“RTGC”)



Evaluation roadmap

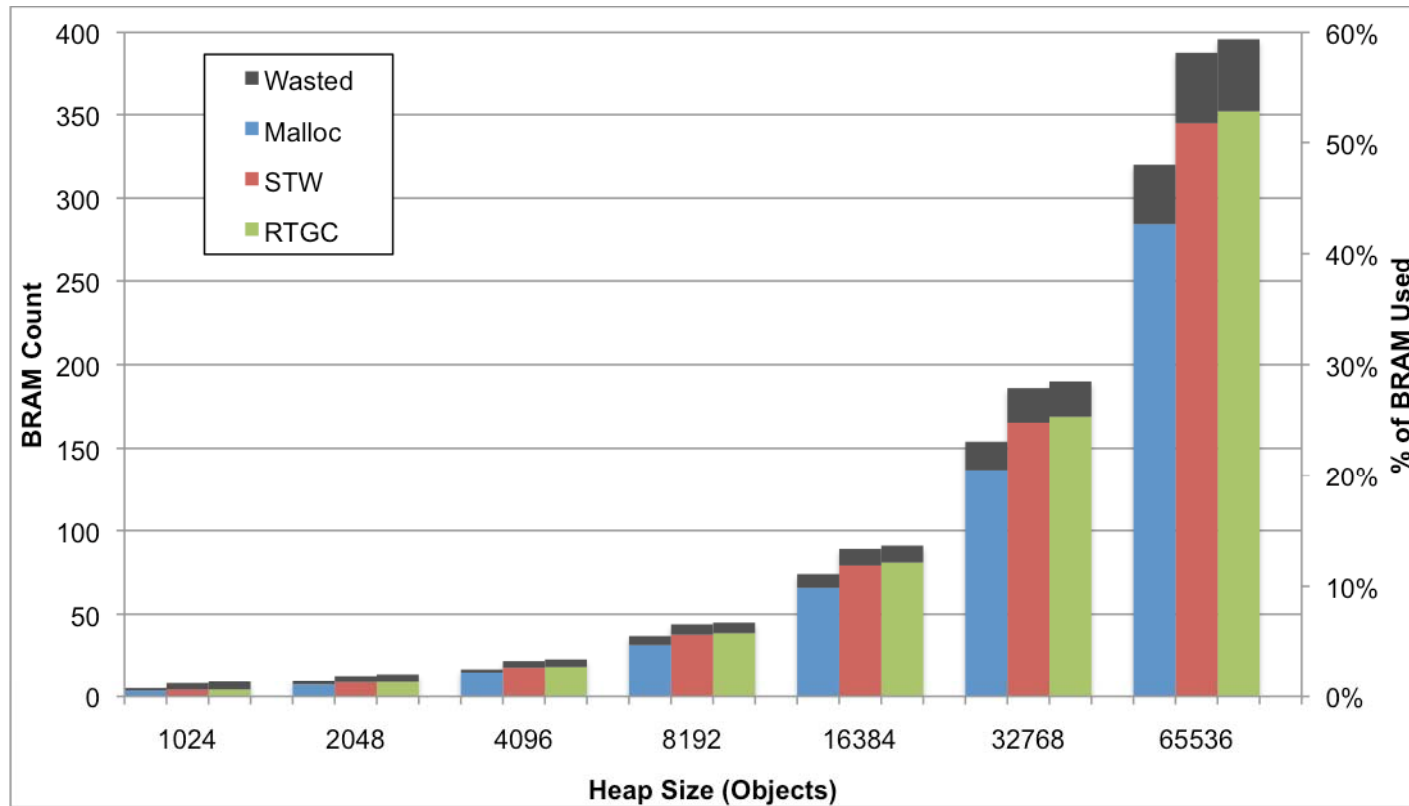
- GC (Space, Frequency)
- Application + GC (Time, Energy)

GC: Area



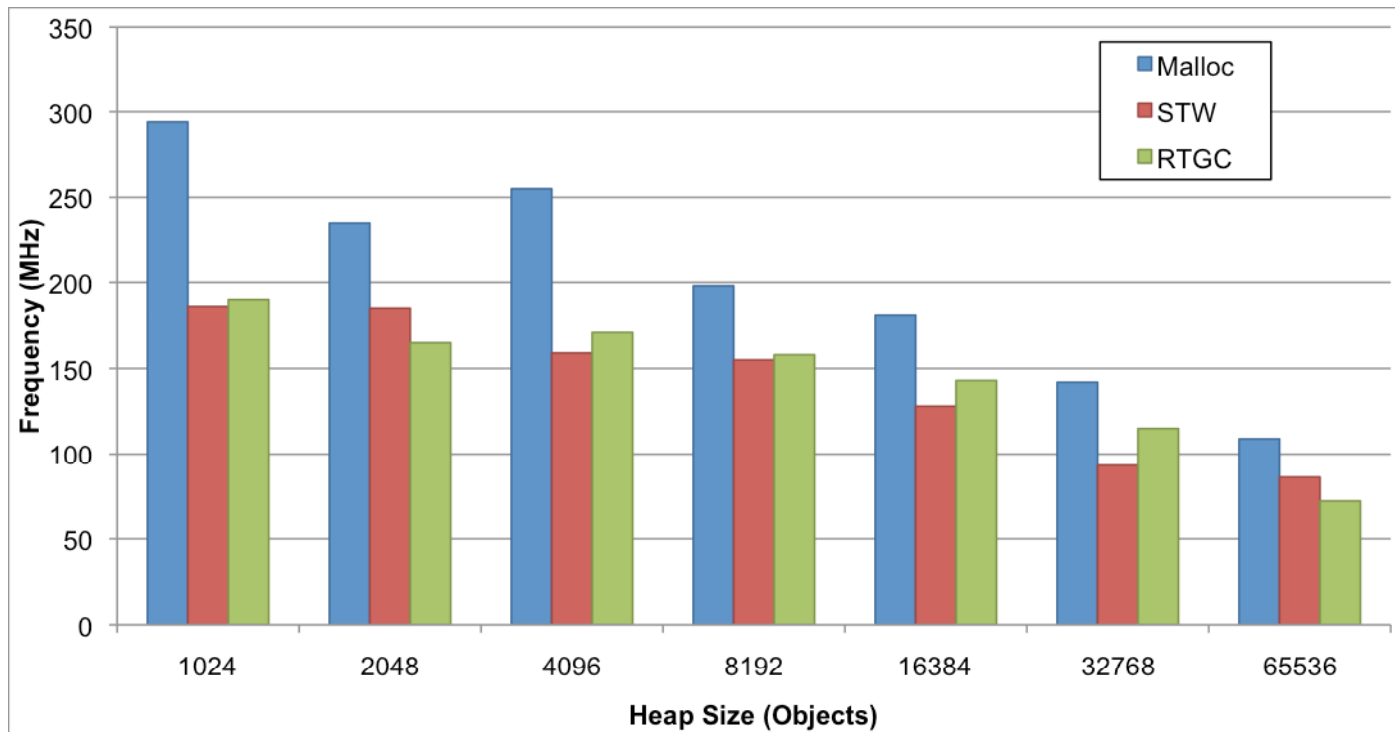
Available slices: 51,840

GC: Memory (BRAM)



Available BRAM: 648 (1.45 MB)

GC: Frequency



Evaluation Roadmap

- GC (Space, Time, Frequency)
- Application + GC (Time, Energy)

Applications

Binary Tree

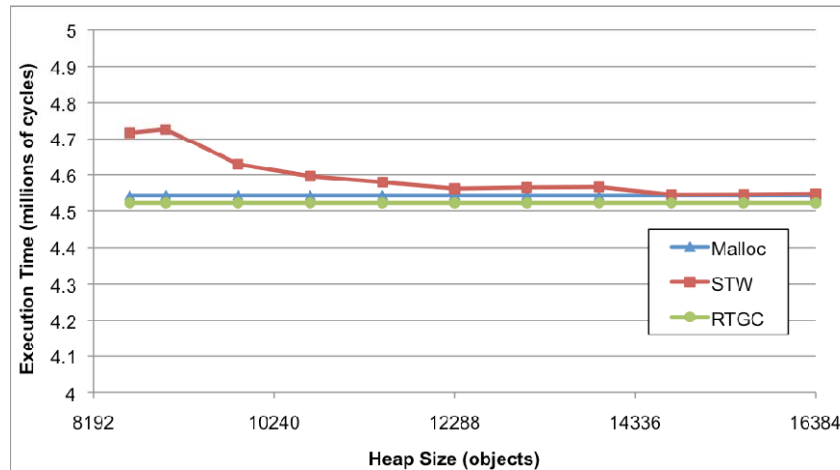
- Operation: insert, delete, traverse
- Bursty operation
- Avg. mutation rate = 0.02
pointer writes/cycle
- Avg. allocation rate (α) =
0.009 objects/cycle

Doubly ended queue (deque)

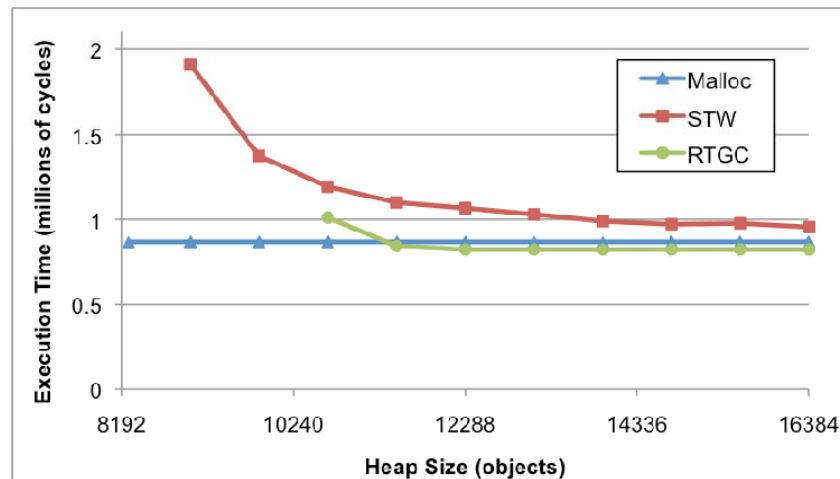
- Two link lists growing from
opposite ends
- mutation rate = 0.13
pointer writes/cycle
- Avg. allocation rate (α) =
0.07 objects/cycles

App+GC: Time (cycles)

Binary Tree

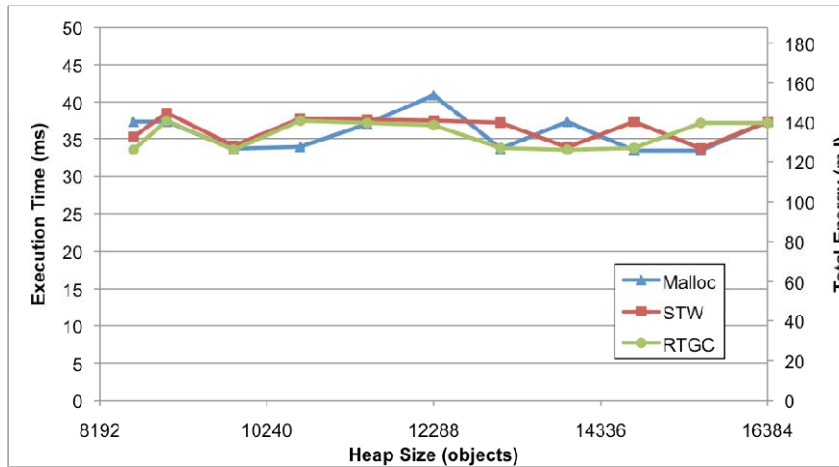


Deque



App+GC: Time (ms), Energy (mJ)

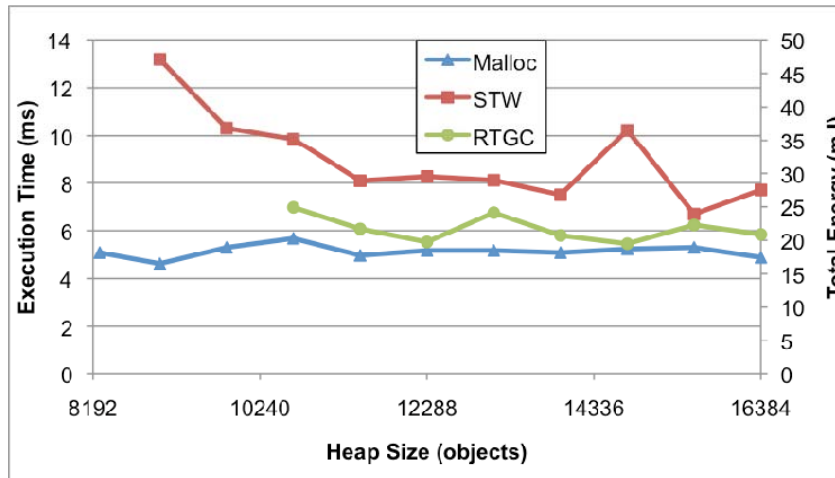
Binary Tree



$$\text{Time (s)} = \text{Time (M cycles)} / \text{Clock_Frequency (MHz)}$$

$$\text{Energy (J)} = \text{Power (W)} * \text{Time (s)}$$

Deque



Conclusion

- First design & implementation of a GC on FPGA
- First GC to entirely eliminate mutator interference by the collector
- Big leap in the field of HLS

THANK YOU

<http://www.research.ibm.com/liquidmetal/>