Digital Sandbox Workshop

Summer 2003

PITTSBURGH DIGITAL GREENHOUSE: growing smart products

PENNSTATE

Electrical & Computer ENGINEERING

Welcome!

- We had a good year…
  - We'll tell you about it
  - Discuss how to best use what we have done
  - Discuss how to make it better
- We are expanding our goals…
  - Full-custom VLSI design (layout)
  - New Design Kits, consolidating existing ones
  - Organized way to capture design flow knowledge
  - We need feedback to increase impact

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Sandbox Mission

- Developing, sharing, supporting CAD tool flow
  - Graduate design classes (Sandbox Design Experience Class)
  - Advanced Undergraduate Classes
  - PDG Short Courses
  - Research
- Providing Technology for Collaborative Design
  - Sandbox Design Experience Class
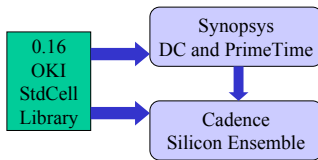
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My New Idols

- CIC in Hsinchu, Taiwan
  - http://tn-www.cic.org.tw/en/
- Activities:
  - Design flow development, support (and testing!)
    - Every tool obtainable from CAD tool vendors
  - Training using tools (7462 students/year!)
  - Multi-chip Wafer Fabrication (300 designs/year!)
  - Chip testing facilities (test chip, or no more fab)
- I wish we could do this all
  - CIC has a budget of $45M and a staff of 40 people

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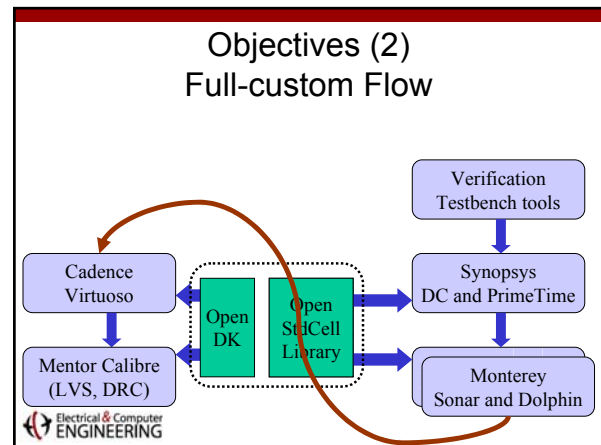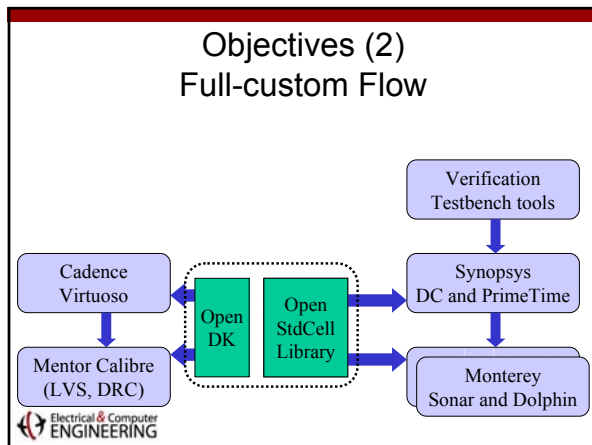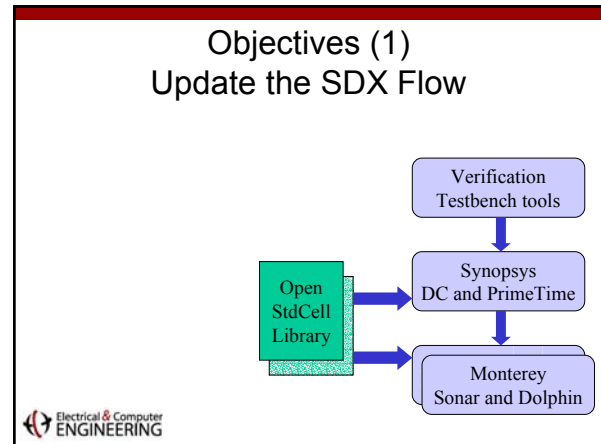

Status Summary (Current)
The SDX Flow

0.16 OKI StdCell Library → Synopsys DC and PrimeTime

0.16 OKI StdCell Library → Cadence Silicon Ensemble

Synopsys DC and PrimeTime → Cadence Silicon Ensemble

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Who's using Sandbox

- Greg Link , PennState ECE
  - Network-on-Chip research
  - ASIC Flow(Synopsis, Cadence); OKI Libraries and memories
- Ricky Radaell-Sanchez, CMU ECE
  - Network-on-Chip LDPC decoder chip
  - ASIC flow (Synopsis, Monterey), STMicro library
- Theo Theocharides, PennState ECE
  - Neural network face detector
  - ASIC flow (Synopsys, Cadence); OKI library and memories

- Others using FPGA tools, Synopsys for area estimates, Cadence generic PDK analog design, NCSU PDK for AMI 1.6u

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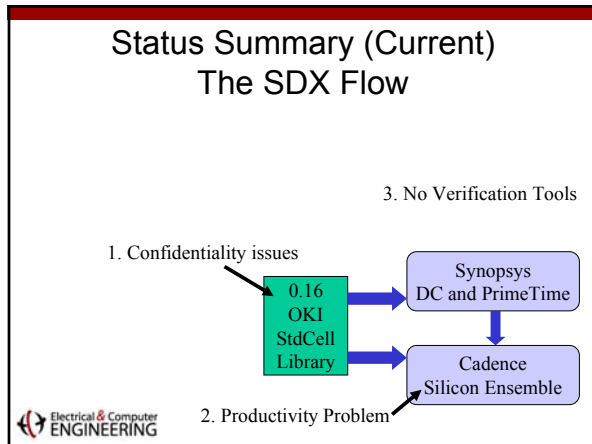
Status Summary (Current)
The SDX Flow

3. No Verification Tools

1. Confidentiality issues

0.16 OKI StdCell Library

Synopsys DC and PrimeTime

Cadence Silicon Ensemble

2. Productivity Problem

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Objectives (1)
Update the SDX Flow

Verification Testbench tools

Open StdCell Library

Synopsys DC and PrimeTime

Monterey Sonar and Dolphin

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Objectives (2)
Full-custom Flow

Cadence Virtuoso

Mentor Calibre (LVS, DRC)

Open DK

Open StdCell Library

Verification Testbench tools

Synopsys DC and PrimeTime

Monterey Sonar and Dolphin

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Objectives (2)
Full-custom Flow

Cadence Virtuoso

Mentor Calibre (LVS, DRC)

Open DK

Open StdCell Library

Verification Testbench tools

Synopsys DC and PrimeTime

Monterey Sonar and Dolphin

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Tech Library Complications

- NDA: No Design Allowed?
- TSMC, ST:
  - No educational use
  - Specific research use
- OKI
  - Abstract views only
- SCMOS based
  - Not very tech specific
  - No memory generators, etc.

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Agenda

- Full-custom design flow (Max Khusid)
- Better semi-custom design flow (Herm and Tom)
- Sandbox Website and CADFAQ (Max)
- Discussion and Wrapup
  - Dave: Synergy between Sandbox flow and short courses
  - Promotion of CADFAQ
  - Other topics?

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Feedback

- We can't do everything
- Big new things
  - Examples: Analog Artist, NeoCell, etc.
  - Realize that these may take some time
- Small adjustments
  - Things that we can do that make what we're doing more useful
  - New class requirements
- Making our job easier
  - Things that we can utilize now
  - Reducing duplicated effort

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