# CMULib18

**Carnegie Mellon 0.18um**
**Standard Cell Library**

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## Motivation

- Supporting Full-custom Design
- Using the Same Design Kit for both:
  - Advanced Undergraduate VLSI
  - Sandbox Design Experience
- Integrate a little Semi-custom into undergraduate VLSI

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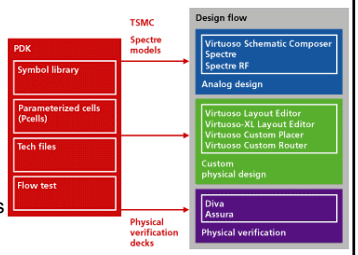
## Process Design Kit

- Targeted at
  - Full-custom IC
  - Analog
  - Mixed-Signal
- Foundry data
  - DRC, LVS
  - Technology files
  - Simulation data
  - Diva rules

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## NCSU PDK

- North Carolina State PDK
  - Free for education and research
  - Targets SCMOS design rules, deep submicron and submicron (available through MOSIS)
  - TSMC 0.25, 0.18
  - Also: AMI 1.6, 0.6, HP 0.6, TSMC 0.4, 0.3
- NCSU CDK adopted for our environment
  - Integrated with Cadence 4.45/5.0 package
  - Support for Deep Submicron rules added
  - Focus: TSMC 0.18
  - Added Diva DRC rules for Metal 5 and 6
  - Using Hspice for simulation and different transistor models (from MOSIS)

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## Additional PDK Goals

- Calibre:
  - Chip scale LVS, DRC
  - Chip scale extraction
- Enable Tape-outs thru MOSIS

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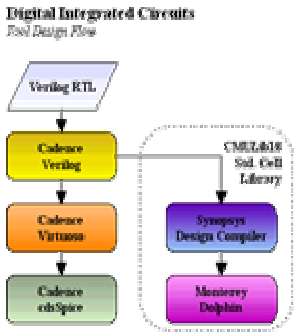
## Custom VLSI Course

**Design Flow for Fall 2003**

- Semi-custom design flow is introduced in parallel with full-custom
- Students implement a design using both full-custom and semi-custom flows
- They observe productivity improvements of semi-custom flow and performance gains of full-custom
- Carnegie Mellon Standard cell library is used in semi-custom design

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## CMULib18 Motivation

- Legal issues with commercial libraries
  - Obtaining std.cell libraries is a lengthy process
  - Commercial libraries require NDA's every semester and by both students and faculty
  - Legal differences in education or research use
- Technical Limitations of commercial libraries
  - Typically, no or limited technical support provided
  - No full views (no layouts, schematic, etc)
  - Can't be extended for easily extended for research purposes

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## CMUlib18, Credits

- CMULib18 completed over the summer
  - First revision, more to come
  - Build on a SCMOS-based "open" design kit
- Project Lead
  - Andrzej Strojwas and Herman Schmit
- Cell Layout and Characterization
  - Zack Menegakis and Steve Beigelmacher
- CAD Support, LEF,Monterey Dolphin
  - Max Khusid and Tom Kroll

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## CMULib18, at a glance

TSMC 0.18um, SCMOS DEEP
- Bsim3v3 SPICE models are taken from MOSIS
- 6-metal process

- Development Process
  - Cell layouts were done in Cadence Virtuoso
  - Built using NCSU PDK (DRC, LVS, ETC, layers defs)
- Current Status
  - Contains 35 most commonly used cells
  - Integrated with synthesis and P&R tools
  - Capable of going through entire RTL-to-GDSII design flow

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## CMULib18, Cell List

- Primitive: INV, BUF, TRIINV, TRIBUF
  - 1, 2, 4, 8x strength for INV and BUF
- Basic gates: AND, OR, NAND, NOR, XOR, XNOR
  - Multi-input (2,3,4)
  - 1x strength
- Complex gates: OAI, AOI, MUX
- Sequential: Latch, DFF
  - Scanned and Regular
  - With and without Clear
- Future Releases
  - more FFs, I/O Pads, Clock buffers, more drive strengths

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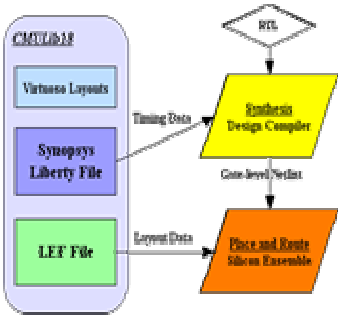
## CMULib18, Where it fits the flow

- Synopsys Liberty file:
  - Delay calculations
  - Load models
  - Behavioral description
- LEF file
  - Abstract cell views
  - Cell geometry
  - Pin placement
  - Layers resistance and capacitance

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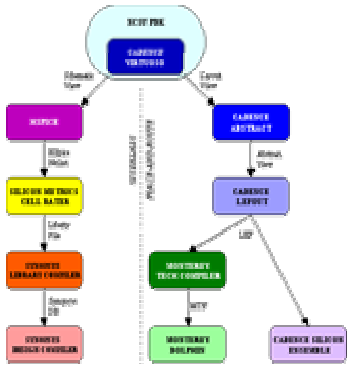
## CMULib18, Design Process

1. Cell Layout
2. Circuit Simulation and Netlist Extraction
3. Abstract and LEF generation
4. Cell Characterization
5. Synthesis tool setup
6. Place-and-Route tool setup



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## Other Public Libraries

- *VirginiaTech Standard Cell library (VTVTLib25)*
  - SCMOS 0.25um (DEEP SUBMICRON rules), NCSU PDK
  - Integrated with Silicon Ensemble and Design Compiler
  - Approx. 40 cells, layouts provided
  - Free for universities and non-profit organizations
- *Cadence Standard Cell library (GSCLib)*
  - Demo library, still work in progress
  - Appears to be based on 0.18um process
  - Works with Cadence Generic PDK
- *Illinois Institute of Technology library*
  - TSMC 0.25/0.18 (SUBMICRON SCMOS rules)

*All Libraries are installed on AFS under Sandbox project tree.*

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## Sandbox, Big Picture

*SEMI-CUSTOM DESIGN*

- CAD Tools
  - ModelSim
  - Design Compiler
  - Silicon Ensemble
  - Monterey Dolphin
  - *Verisity Specman*
- Std. Cell Libraries
  - CMULib18
  - STMicro 0.09,0.18,0.13
  - OKI 0.16
  - Cadence GSCLib
  - VTVTLib25

*FULL CUSTOM DESIGN*

- CAD Tools
  - Cadence Virtuoso
  - Cadence ICFB suite
  - Hspice
  - *Calibre*
- Process Design Kits
  - NCSU CDK (SCMOS for TSMC, AMI, HP)
  - Cadence Generic PDK
  - *STMicro 0.09 – 0.18*
  - *TSMC*

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## Goals and Discussion

- Help with Cadence Virtuoso Installation
  - ECE facilities understands Cadence under AFS
- Consolidate Design Kits
  - Who has NDAs for what libraries?
  - Is it beneficial to keep them all in one place?
- Install the 0.18µ Design Kit and CMU18Lib
- Provide quick start labs for full custom design
- Needs:
  - The contact for PSU and Pitt?
  - Timeframe? When is undergrad VLSI taught?

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