


Digital Sandbox Website

www.ece.cmu.edu/~sandbox

The website is now live and contains information about

- Sandbox courses
- CAD tools used
- Industry participation
- Support available
- Computing facilities
- News and Team info

Thanks to the ECE Multimedia team for the design





The Digital Sandbox website interface includes a top navigation bar with links for 'about', 'courses', 'resources', 'news', 'learn', 'support', 'industry', and 'tools'. The main content area features a 'News & Events' section with three items: 'Digital Sandbox Workshop', 'CMU std. cell library in beta testing', and 'CAD FAQ officially released'. Below this is a 'Welcome' section with a paragraph describing the project's goals and a 'read more' link.

CAD FAQ, Intro

- Purpose:
 - To ease CAD tools learning curve
 - VLSI CAD tools are notoriously "user-hostile", script-based, with thousand pages of documentation
 - Provide a central access point
 - Typically, this help info is scattered on the web, CAD companies restricted sites (SourceLink, SolvNet), academic websites
 - Lessen the burden on ECE Gripe and us
 - FAQ covers actual issues students in 18-725 ran into and accounts for significant portion of software-related issues

Knowledge base for Computer Aided Design Tools used in the Sandbox courses and available at Carnegie Mellon, ECE.




CAD FAQ, Coverage

Primary emphasis put on semi-custom ASIC design flow, but full-custom, FPGA, possibly mixed-signal flows will follow.


- Mentor Graphics ModelSim - HDL simulation
- Open Verification Library – Functional Verification
- Synopsys Design Compiler - Synthesis
- Cadence Silicon Ensemble – Place and Route
- Monterey Dolphin –Place and Route
- Cadence Virtuoso and ICFB – Full-custom layout
- Silicon Metrics Cell Rater – Standard Cell Library design

- On the waiting list: Synplify FPGA, Synplify ASIC, Vera/Specman, Synopsys FPGA Express, First Encounter, Caliber



CAD FAQ, Coverage, cont.


- Support for middleware as well:
- Process Design Kits (Full-custom, Analog, MEMS)
 - North Carolina State (SCMOS, 0.18um and up)
 - Cadence Generic PDK (demo PDK)
- Standard cell libraries – Semi-custom ASIC
 - Carnegie Mellon CMUlib18 – TSMC 0.18
 - VirginiaTech VVTIib25 – TSMC 0.25
 - GSCIib – Cadence Generic



CAD FAQ, Contents

- FAQ for each CAD application typically includes:
 - Unix Environment setup (license, path, libs)
 - Short hands-on tutorials
 - Most common problems running the tools (actual questions from the students)
 - Design tips and tricks
 - Links to Help Documentation

Currently, contains over 50 articles and growing



Search this FAQ this site the web for

CAD F.A.Q Contents


1. [Mentor Graphics ModelSim 5.7a](#)
 1. [Initial environment setup](#)
 2. [Vim error: /vlog:10\) Failed to access library 'work' at "/work"](#)
 3. [Running vim in command-line mode, w/o GUI](#)
 4. [How to pass Verilog macros to Vim on the command-line](#)
 5. [Vim error: /vlog:10\) interleaved gate.v\(102\): Instantiation of 'MUX211'](#)
 6. [Vim loading issues](#)
 7. [Vim doesn't respond to mouse clicks on Sun machines](#)
 8. [ModelSim error: Iteration limit reached](#)
2. [Cadence Silicon Ensemble 5.3](#)
 1. [Cadence error: Pseudo color graphics card not detected](#)
 2. [Cadence warning: Can't read link library file /vsar_library.db](#)
 3. [si fix.pl "Permission denied" error](#)
 4. [To move RAM/ROM in SE interactively](#)
 5. [Precise pin placement](#)
 6. [To find a Cell, Net, etc in SE](#)
3. [Synopsys Design Compiler 2002.05-SP2](#)
 1. [Initial environment setup](#)
 2. [Synthesis with DesignWare fails](#)
 3. [DC Area units](#)
 4. [Synthesis fails with CKEI command cell](#)
 5. [Synthesizing parametrizable designs](#)



CAD FAQ, Website


www.ece.cmu.edu/~sandbox/cadfaq

- Dynamically generated, updated periodically
- Full searchable by keyword or can be browsed by CAD application
- Access is restricted to the following domains because CAD FAQ contains proprietary documentation
 - cmu.edu
 - pitt.edu
 - psu.edu
 - digitalgreenhouse.com



Sandbox Infrastructure

- Sandbox Server Farm
 - 8 Sun Fire 280R, dual-CPU 750/900 MHz with 4 GB RAM
 - Server farm for VLSI CAD applications demanding high-performance processing power and memory bandwidth
 - Synthesis
 - Place-and-route
 - Verilog simulations
 - Spice simulations
 - Looking into adding [Sun Grid Engine](#) load-balancing and job scheduling software as the big players add support for it
 - Currently have scripts that show real-time cluster load



Questions

- Questions
 - Comments
 - » Suggestions
- Any Pitt/PennState resources can be added to CAD FAQ?
- Possible CAD training sessions for Faculty and Staff?
- Should we consider using AFS for file exchange, tools support or CVS was sufficient?

