DIGITAL SANDBOX WORKSHOP

Summer 2004

Sandbox Design Experience Course

Electrical & Computer ENGINEERING

PENNSTATE

Outline

- Introduction
- Overview of SDX 2003
- Sandbox Design Experience 2004
  - What's new
  - Project overview
  - Final Results
- CAD Flow in SDX 2004
- Multimedia CAD demos

Electrical & Computer ENGINEERING

Sandbox Design Experience Course

- Graduate-level VLSI course taught concurrently at three universities in the Spring of each year
  - Carnegie Mellon University
  - University of Pittsburgh
  - Pennsylvania State University
- Professors teaching the course in 2004
  - Rob Rutenbar and Wojciech Maly (CMU)
  - Vijay Narayanan (PSU)
  - Ivan Kourtev (PITT)
- Course contents
  - Project-based, complex SoC design with semi-custom design flow
  - Use Synopsys and Cadence CAD tools and OKI 0.16um technology

Electrical & Computer ENGINEERING

First SDX, 2003

- Project Design:
  - Network-on-Chip architecture
  - Low Density Parity Check error-correction decoder
- ASIC design flow
  - Modelsim, Design Compiler, Silicon Ensemble with OKI 0.16 library
- Web Conferencing with PSU and PITT for lectures and reviews
- Team Organization
  - 4 teams in total (2 CMU, 1 Pitt, 1 PSU) each working on a chip
  - 4 subteams in each team working on a chip component
- All subteams finished layout and RTL verification

Electrical & Computer ENGINEERING

Lessons of the first SDX course

- Overall the class was a major success and popular with students
- Complete chip assembly not finished
  - Previous-generation CAD tools (esp. Place and Route)
  - Not enough time (approx. 2 months for design stage)
- Functional verification is challenging
  - No special tools used and not enough time

Electrical & Computer ENGINEERING

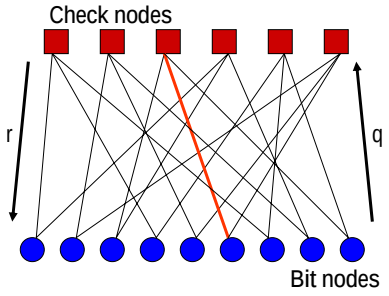
What's new this year, SDX 2004

- Herman Schmit left Carnegie Mellon in December 2003
  - Professors Rob Rutenbar and Wojciech Maly replaced him
- Project
  - Specification is much more relaxed
- Improved CAD flow
  - Added industry-standard verification tool: Verisity
  - Added power estimation
  - Improved coverage of IP integration and clock tree design
- Designed multimedia training demos for CAD tools

Electrical & Computer ENGINEERING

Project Design, LDPC

- Implement LDPC for IEEE Standard 802.11g Spec, June 2003
  - Hot research topic
  - Part of a standard for Digital Satellite, 4G wireless standards; research active for use in Disk Drives, Optical Communication, Ethernet, etc
  - No commercial chips exist to date.. (Intel is working on it)
  - Excellent application for Hardware, exhibits massive parallelism
- Actual spec given to students
  - Data Rate: 54 Mbps
  - Packet Size: 1024 bits
  - LDPC Decoding Accuracy: 10%
  - Area: < 200 mm^2



Electrical & Computer ENGINEERING

Project Design, LDPC

- Last year we gave students
  - Elaborate specification
  - Simulation tools
  - Verilog code for most complex components
  - Communication protocols
  - Suggested architecture
- This year… no fixed architecture and minimalist spec
- Student reaction:
  - Initial: complete disbelief
  - Final: excitement and innovative, diverse architectures

Electrical & Computer ENGINEERING

Project Experience

- Project Flow
  - Teams spent more than a month on architecture alone
  - But… once they got rolling, they had layouts a lot quicker than last year
    - Last year, many people were confused about LDPC till the semester's end
  - Teams reached chip integration and RTL verification for the entire chip
- Team Dynamics
  - Teams were more flexible and came more together than in SDX 2003
  - Few very strong PhD students played a major leadership role
- CAD Design flow
  - More complete: covered power, clock tree, memories

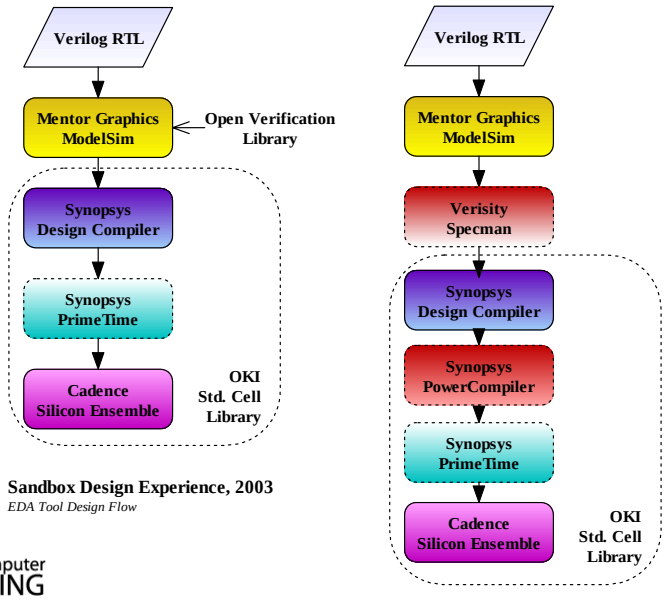
Electrical & Computer ENGINEERING

Final Results

Team	Highlights	Mbps	MHz	W*	mm^2
CMU1	Static schedule	160	275	23	150
CMU2	Dynamic schedule	76	173	N/A	90
PSU	H-matrix topology Supernode	129	200	N/A	100
PITT	Hypercube cluster topology	54	115	N/A	144

Electrical & Computer ENGINEERING

SDX 2004, CAD Design Flow



Sandbox Design Experience, 2003
EDA Tool Design Flow

Electrical & Computer ENGINEERING

CAD lessons

- Verisity Specman for functional verification
  - Many students found the learning curve too steep
  - Previous coursework in verification would be helpful
- Power Estimation
  - All teams obtained power estimation numbers
  - But… bugs in OKI library confused students
  - Better libraries to make power results more predictable
- OKI memories
  - Some teams used memories successfully in their designs
  - Others decided not to b/c area specification didn't force them
- Place and Route
  - Silicon Ensemble can not handle multimillion-gate designs
  - We need a new Place and Route tool

Electrical & Computer ENGINEERING

Multimedia CAD Demos

Problem Definition:

- In SDX class students must learn in a month(!)
  1. ModelSim
  2. Specman
  3. Design Compiler
  4. PrimeTime
  5. Silicon Ensemble
  6. PowerCompiler
- All CAD tools are notoriously counter-intuitive, very complex, come with thousand-page manuals, script-based
- In the industry, engineers attend CAD training for a week, and spend months learning the tools

Electrical & Computer ENGINEERING

Multimedia CAD demos

Solution

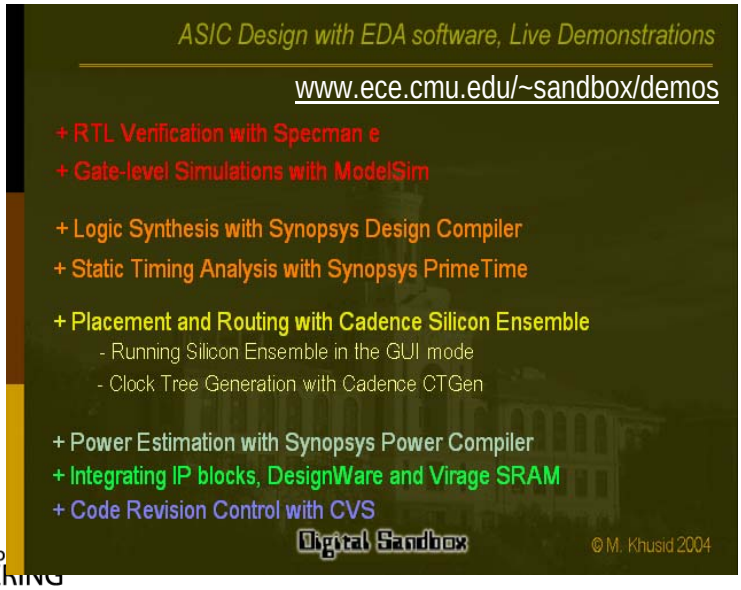
- Prerecorded animated Flash videos
  - Show step-by-step how to setup the tool and run a sample design
  - Contains few essential slides explaining underlying CAD concepts
  - Include on-screen comments highlighting functionality and possible pitfalls
  - Web-based, cross-platform, only needs ubiquitous Flash plug-in
  - Records actual *live* session
- Collection of files for push-button tool use

Results

- I received minimum CAD-related questions from students
- Good reception from students

Electrical & Computer ENGINEERING

Sandbox Multimedia CAD Tutorials



Electrical & Co
ENGINEERING

CAD demos, how to

- Created with Macromedia RoboDemo and RoboPresenter
  - In Flash web-based format; can be voice-annotated as well
  - Demos are easy to compile and annotate (1-2 hours)
  - Requires no programming; software records your mouse movements and keyboard strokes
  - Demos are created on Windows, viewed on Windows/Unix/etc

Electrical & Computer
ENGINEERING

Sandbox Plans for the Demos

- Package for each Jump-Start kit
  - Multimedia Flash, step-by-step demo showing how to run the tools
  - Supplementary design files(RTL), environment setup files(Unix scripts) and all required scripts for the CAD tools
  - PowerPoint presentation explaining basic concept required
  - Web-based, searchable knowledgebase of most common issues
  - SCMOS Design Kit and CMUlib18 Standard cell library
- Develop a rich set of Jump-Start CAD training materials
  - Full-custom: 6 kits
  - Semi-custom: 14 kits
  - FPGA: 3 kits

Electrical & Computer ENGINEERING