DIGITAL SANDBOX WORKSHOP

Summer 2004

Sandbox CAD Support

Electrical & Computer ENGINEERING

PENNSTATE

Digital Sandbox Mission

The virtual SoC design support facility provides "industrial strength" hardware, software, EDA tools, workflows, and technical support staff to all three PDG member universities. This will enable Digital Sandbox student and faculty users to create real-world designs for modern semiconductor process technologies, and thus, enhance university-industry interaction and improve the quality of graduating engineers.

Source: www.digitalgreenhouse.com

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Sandbox Status

We had a productive year…

- Sandbox CAD support greatly expanded
- We obtained latest fabrication technology
- Our projects are increasing in scope and reaching other universities
- Our work supports more research projects and classes

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Presentation Outline

- Sandbox CAD support
  - Improvements over last year
- Fabrication Processes
  - Available processes
- Sanbox Initiatives
  - CMUlib18
  - SCMOS 0.18um
  - CMUram
  - Infrastructure
- Sandbox's impact
- Next year's goals

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Sandbox "Support" Defined

- Sandbox CAD support includes
  1. Obtaining and installation
  2. Integration with existing tools
  3. Tutorials
  4. Jump-start kits and sample scripts
  5. Database of common issues
  6. E-mail support

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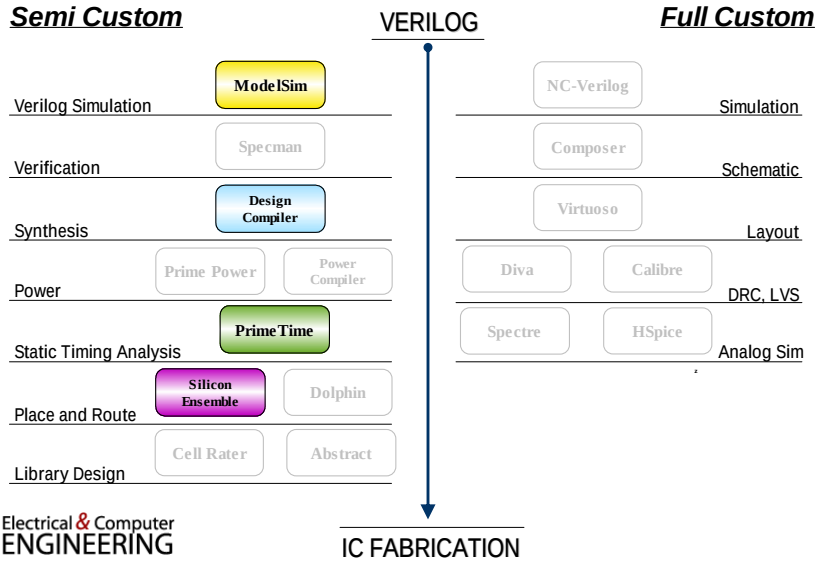
Sandbox CAD Support, 1st year



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2nd year CAD goals

- Full-custom design flow
  - To support undergraduate curriculum
- Functional Verification
  - Add to Sandbox Design Experience course
- Power Estimation
  - Add to Sandbox Design Experience course
- Sign-off tools
  - To enable fabrication
- Standard cell library development
  - For semi-custom <-> full-custom bridge

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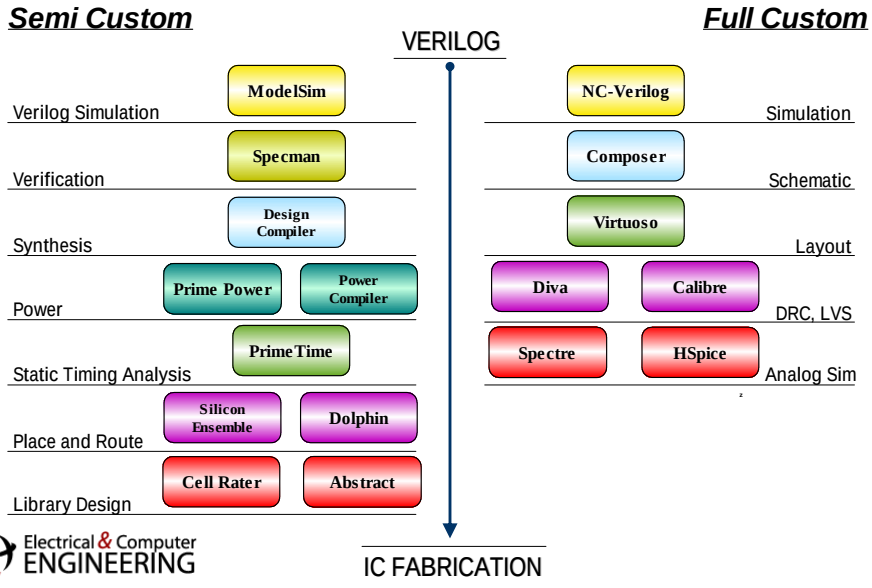
Sandbox CAD Support, 2nd year



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3rd CAD year goals

- To enable multi-million gate SoC design
  - Latest Place-and-Route tools, First Encounter
- To add support for Design-for-Manufacturing
  - Technology CAD tools
- To add support for Design-for-Testing
  - DFT tools from Cadence and Synopsys
- To add support for FPGA tools
  - Synplicity software
- To improve Functional Verification flow
  - Cadence software

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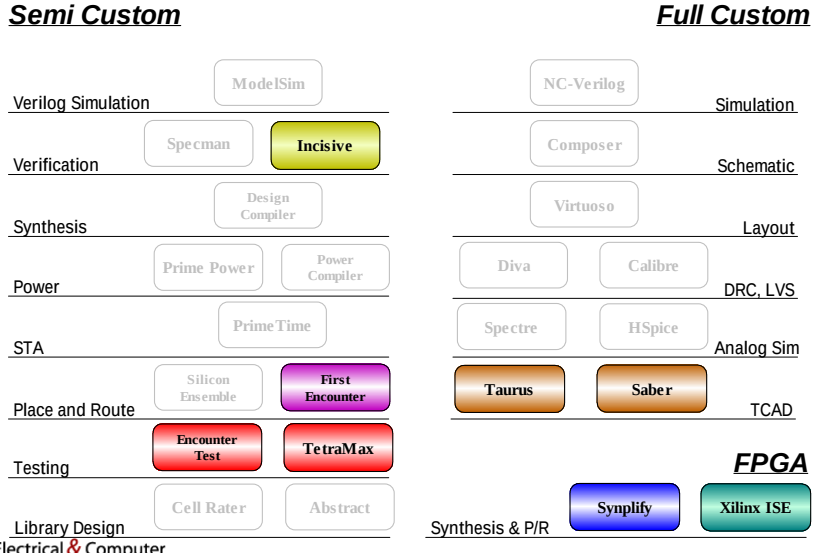
Sandbox CAD, 3rd year projections



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Fabrication Process support, 1st year

Standard Cell Libraries

Semi Custom design flow

- Faraday 0.13um
- ST Micro 0.18, 0.13um, 90nm
- Hewlett Packard 0.35um
- OKI 0.16um
- TSMC 0.13um, 90nm
- Generic Cadence
- CMUlib18 0.18um

Process Design Kits

Full Custom design flow

- IBM SiGe 0.18um
- TSMC 0.25, 0.18um
- UMC 0.13um
- ST Micro 0.18, 0.13um, 90nm
- Hewlett Packard 0.35um
- Generic Cadence
- Scalable CMOS 0.18um

Public, No restrictions | Restricted to School | Restricted to Project

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Fabrication Processes supported, 2nd year

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Process and Libraries Highlights

- Nanometer processes available
  - TSMC 0.13um, 90nm
- Completely open-source processes and cell libraries available
  - SCMOS 0.18um and Generic Cadence
- First open-source manufacturable deep-submicron library
  - CMUlib18 0.18um
  - Developed in-house by the Digital Sandbox

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CMUlib18, Sandbox cell library

- No legal constraints
  - No NDA's to sign
  - Open for both research and education
  - We intend to release it to other universities
- Open-source
  - Complete layouts, analog sims
- Integration with custom and analog
  - Easily extend the library with custom cells
  - Approach complex mixed-signal SoC
- Fabrication with MOSIS

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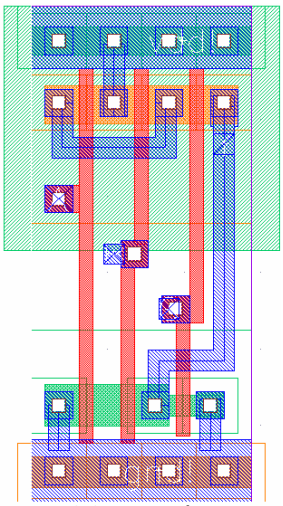
CMUlib18, Specification

- Process
  - Scalable 0.18um CMOS, 6-metal deep submicron
  - Fabrication with MOSIS and TSMC
- Cells
  - 35 most commonly used cells
  - Various strengths, plus cells with scan
- Design Flow
  - Verified with Synopsys and Cadence tools
  - Can be imported to Virtuoso for DRC/LVS and analog simulations



AOI2_1x gate layout

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How good is CMUlib18

Standard Cell Library Comparison

Reported: Girish Venkataramani | Answered: Max Khusid | Date: 03/11/04

Sample design: LDPC decoder for 6x9 H-matrix, approx 100,000 gates, 15ns clock period.

Std. Cell Library	Area, sq. um	Slack, ns	Power, mW	Equivalent Gate area, um
Commercial 0.16um	1,245,281	2.17	288 + 0.005	1.56 x 5.2 = 8.112
CMUlib18 2003, SCMOS 0.18um	966,488	4.84	220 + 0.0	1.44 x 6.48 = 9.3312
CMUlib18 2004, SCMOS 0.18um	746,113	8.40	227 + 0.0	1.44 x 6.48 = 9.3312
GSClib	N/A	7.46	721 + 0.0	2.64 x 7.92 = 20.99
Commercial 0.18um	549,797	7.71	268 + 0.0	1.28 x 6.40 = 8.192
Commercial 0.13um	279,297	6.70	105 + 6.8	0.82 x 4.92 = 4.0344
Commercial 0.09um	165,718	6.30	71 + 0.15	0.56 x 3.92 = 2.1952

- Not bad for a first try
  - It's better than one commercial library, worse than the other
- Speed and Area can be improved
  - Can optimize W/L ratios and optimize layout

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SCMOS 0.18um process

- Originally from North Carolina State
  - Adapted for CMU and enhanced for deep-submicron process
- Successfully used in undergraduate custom VLSI course
  - The most modern deep submicron, 0.18um
  - Students learn nanometer challenges
- Open-source
  - Open for education and research
- Fabrication available through MOSIS

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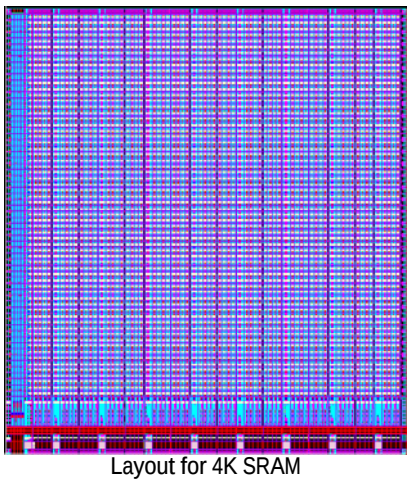
CMUram, SRAM Memory Compiler



Layout for 4K SRAM

- First open-source 0.18um SRAM compiler
- Based on GPDK compiler
- Generates SRAM of any size
  - Layout
  - Schematic
  - Verilog
  - LIB and LEF
- Complements CMUlib18 and SCMOS18 process
- To be released later this year

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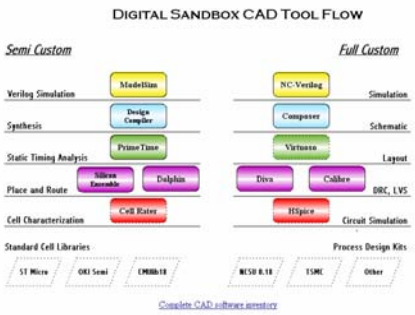
CADFAQ Website

- Knowledge base for Sandbox CAD tools
  - Tutorials, Demos, Sample scripts, Common issues and solutions



www.ece.cmu.edu/~sandbox/cadfaq

  - Website is growing, *150* articles to date
  - Access restricted to PDG universities

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Sandbox Infrastructure

- Sandbox Server Farm
  - 8 Sun Fire 280R, dual-CPU with 4Mb RAM
- Major upgrade to Linux platform
  - Most Synopsys and Cadence tools supported
  - Experienced major speed-ups

- Intel 30 donated powerful Xeon servers to the ECE dept

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Videoconferencing, the need

- Students acknowledge the need for video
  - In the SDX, students and faculty were frustrated with remote connectivity
  - Very hard to communicate, “talking to a wall” experience
- Virtually no interaction with audio alone
  - Video would promote interactive
  - It breaks psychological barriers
- Long-term investment for all three schools
  - Video setup can be reused for other Sandbox, or other classes

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Video Conferencing, Options

- Inexpensive
  - Pros: NetMeeting plus Webcam, cheap $100-500 webcams
  - Cons: very poor quality, can’t see students, and hard to interact
- Outsourcing
  - CMU’s IT group, $200 for 1st hour, $50 for additional
  - SDX course: 6 design reviews + 6 lectures = $2000
  - Pros: no hassle
  - Cons: temporary solution, fixed locations (UC)
- Professional, in-house
  - DV camcoder($1500), cameraman (we can do)
  - Real-time codec server, price? 3-way video? Separate ISDN?
  - Might need professional assistance with setup
  - Pros: state-of-the-art, promote interaction, shared with other classes
  - Cons: price, $5000 – $20,000

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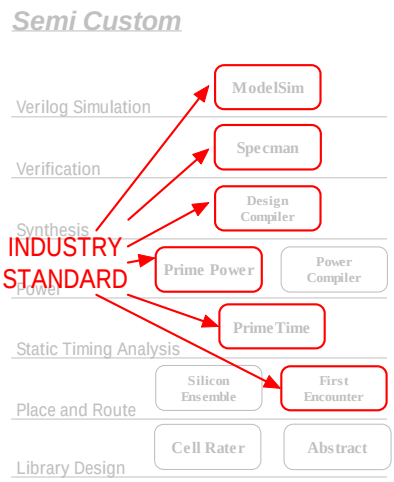
Modern tools – Modern challenges



- State-of-the-art CAD tools allow to stay in touch with modern semiconductor trends
- Challenges addressed:
  - Code coverage
  - Assertions
  - P/R of millions of gates
  - Signal integrity

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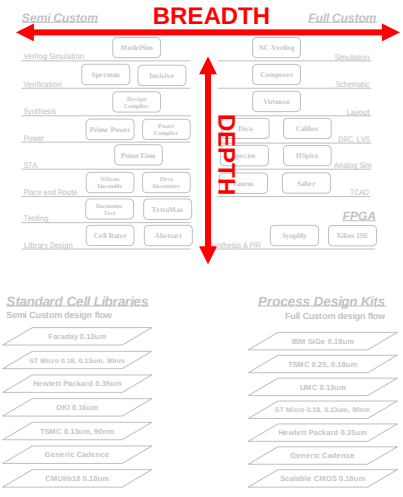
Research quality



- Elaborate design flows improve design *quality* and *credibility*
- Examples:
  - Sign-off quality timing
  - Transient power
  - Custom libraries

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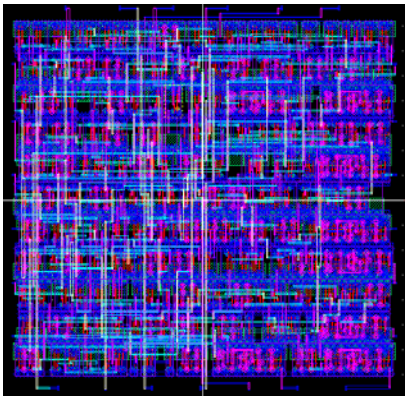
Open-source process and library



Layout with CMUlib18

- CMUlib18 & SCMOS18 open new research opportunities
  - CAD algorithms
  - Leakage
  - Design for Manufacturing
- Allow fabrication of complex multi-million gate designs in academia
  - 10M vs. 10K transistors

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Who is using Sandbox, Research

Student and Advisor	Research project	Sandbox support
S. Rovner & Prof. Pileggi	Via-Patterned Gate Array	Design Kit, Cadence
Y. Takegawa & Prof. Strojwas	Design for Yield	Software installs and support
Z.Menegakis & Prof. Strojwas	Design for Manufacturing lib	Cell library development
C.Hao & Prof. D. Marculescu	Low-power design	ASIC CAD support
J. Hu & Prof. R. Marculescu	Low-power, leakage	Power Compiler, ASIC, libs
Prof. J.C. Hoe and Pueschel	Hardware DSP Automation	ASIC CAD support, libs
Prof. Mukherjee	Classwork and MEMS	Design Kits
T. Zanon & Prof. Maly	Design for Yield	TCAD tools, memory layout
T. Theocharides & Prof. Narayanan	Neural Networks	OKI libs, ASIC CAD
A. Hermawan & Prof. R. Marculescu	Interconnect & parasitics	Cadence, Diva
G. Venkataramani & Prof. Goldstein	Asynchronous HW	ASIC CAD, Encounter, libs
J. Park & Prof. Yue	High-speed analog design	Design kit and libs

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Sandbox support for Education

- Past year Sandbox supported three courses
  - Undergraduate custom VLSI course (18-322), CMU
  - Graduate semi-custom VLSI courses, SDX, CMU/PSU/PIT
  - Graduate custom VLSI course (18-525), CMU
- In 2004, updated undergraduate custom VLSI course
  - Introduce semi-custom design in a junior-level course
- Next year, possible candidates include
  - Undergraduate Functional Verification course, CMU
  - Undergraduate Hardware design methodologies course, PIT
  - Undergraduate Verification course, PITT/PSU
  - Graduate testing course, CMU

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