Managing Pipeline-Reconfigurable FPGAs

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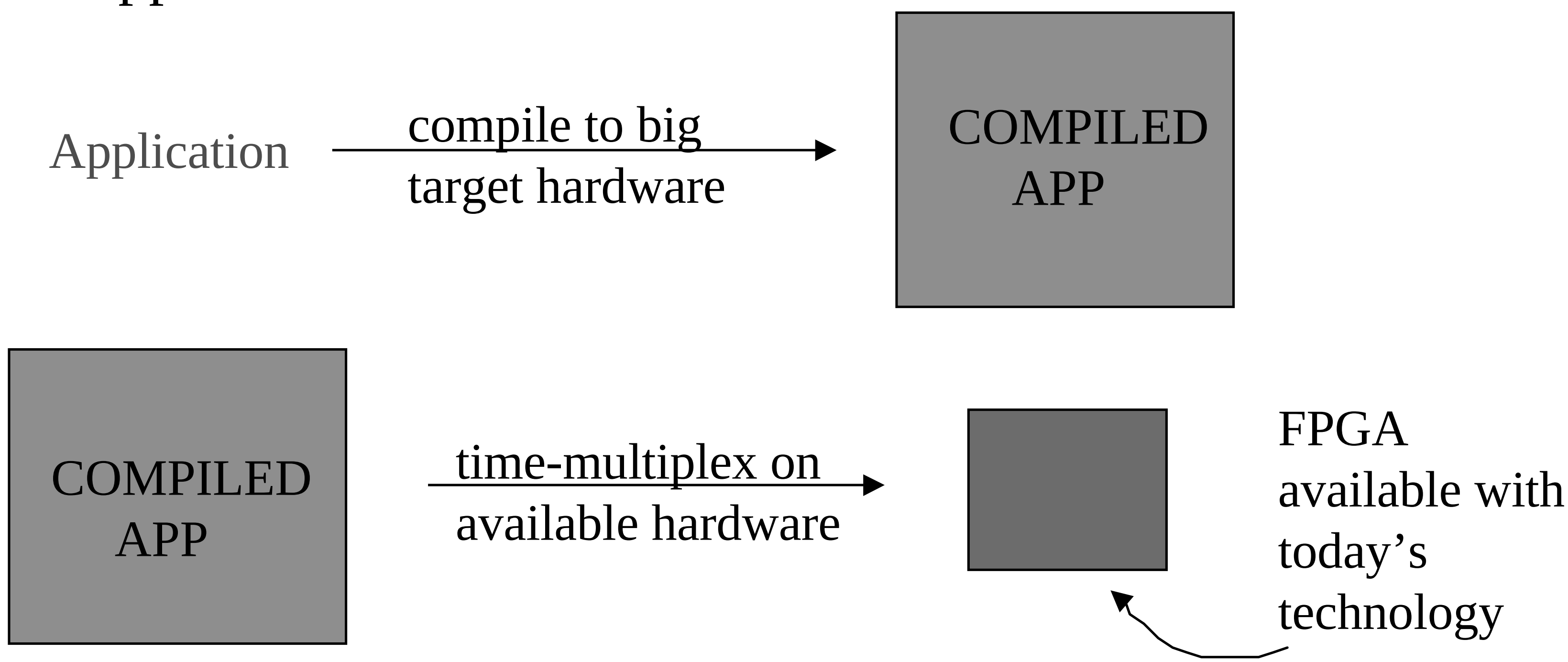
Reconfigurable Computing

- Problems
  - No forward compatibility
    - performance does not scale with technology
    - recompilation required for newer generations
  - Not compiler-friendly
    - applications have to fit in hardware!

Our solution

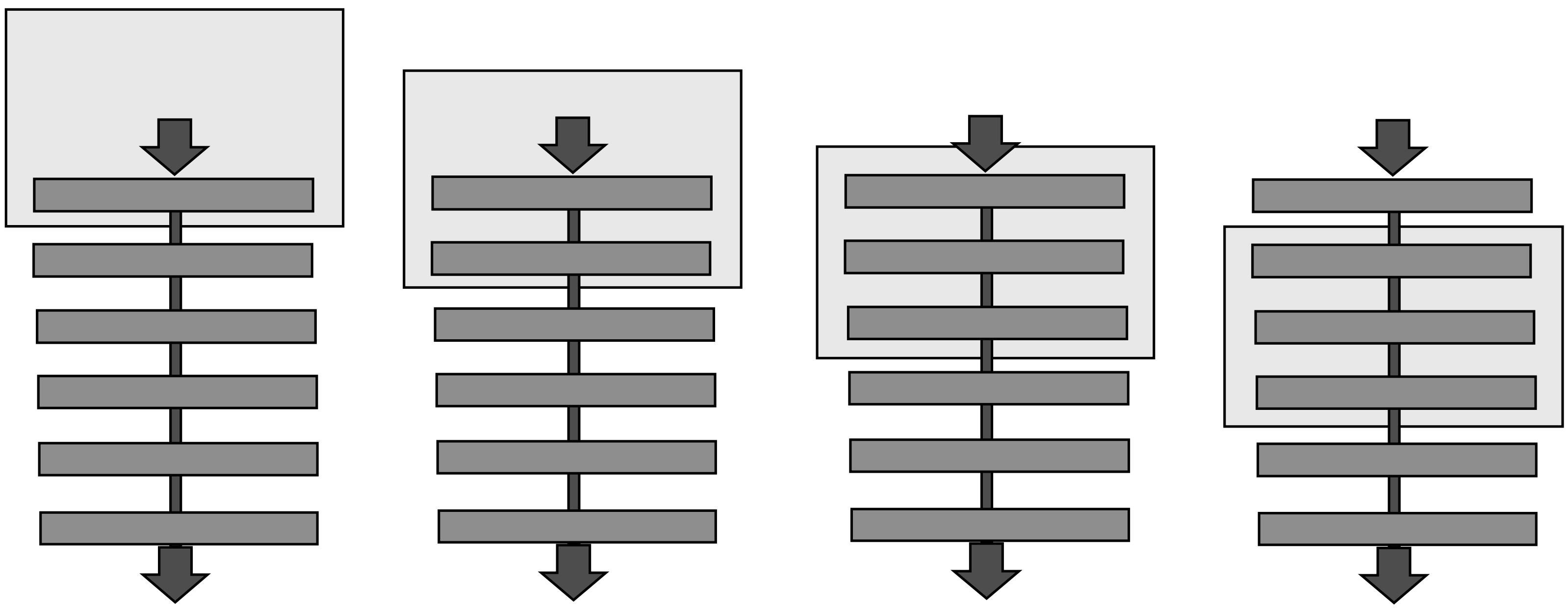
Hardware Virtualization

- assume you have a target hardware that fits the entire application at once



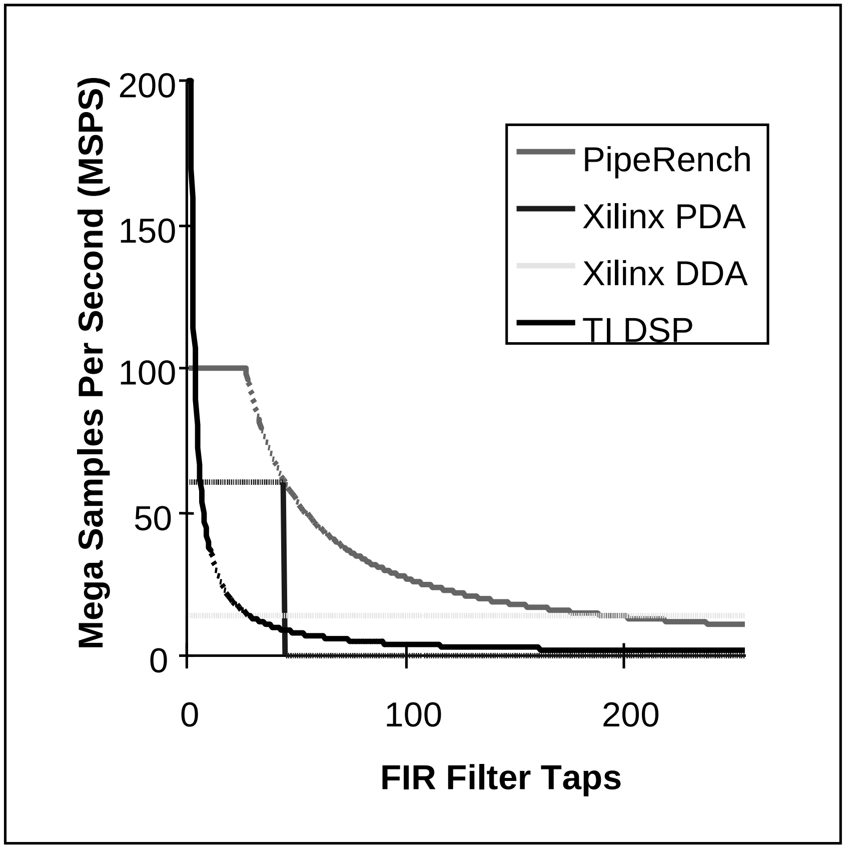
Making it happen

Incremental Reconfiguration: “scrolling” FPGA fabric



How good is this concept?

- CMU PipeRench
  - 100 sq. mm die area
  - 128-bit datapath
  - 100 MHz clock
  - 0.35 um technology



What’s coming your way

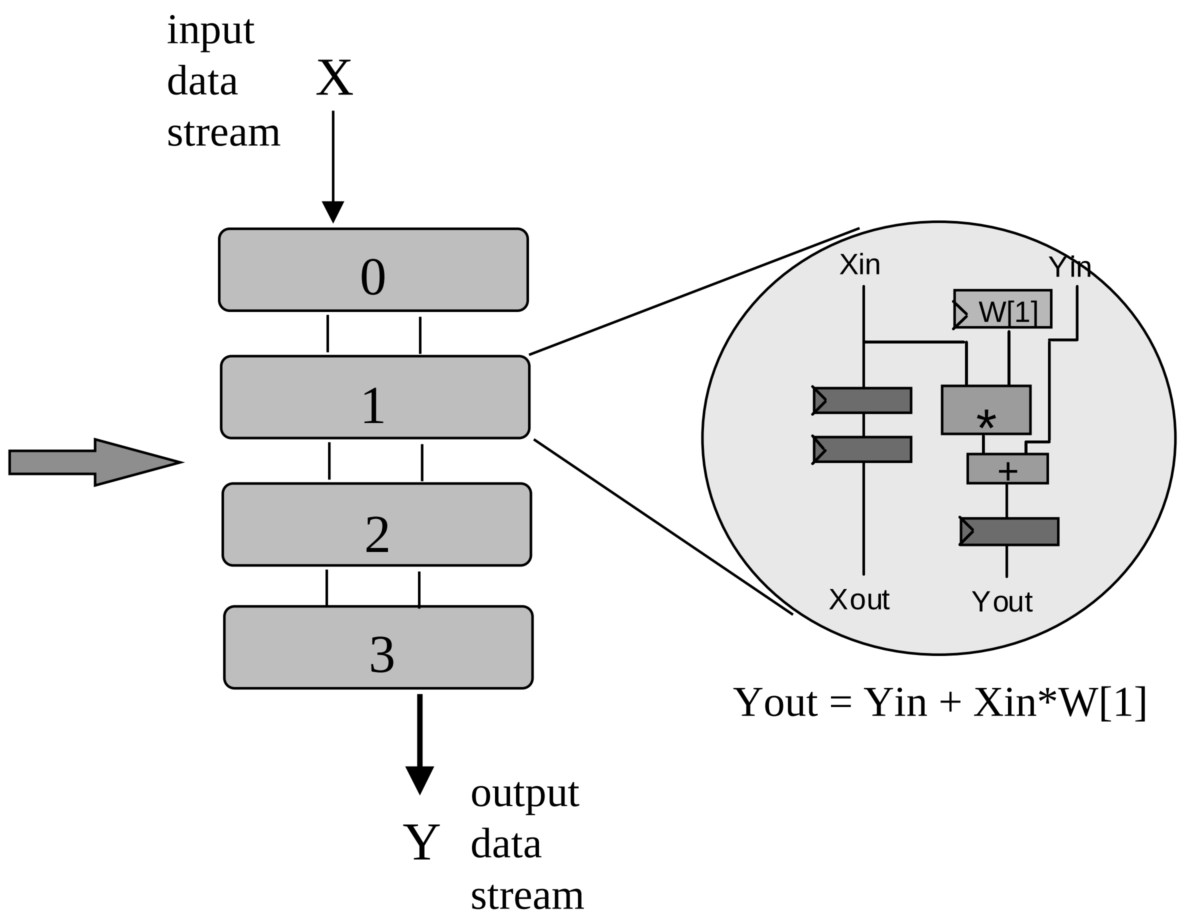
- What’s required to make hardware virtualization work?
- This talk will use an example to illustrate
  - breaks in the input data stream
  - saving and restoring lost state

Example: Convolution Algorithm

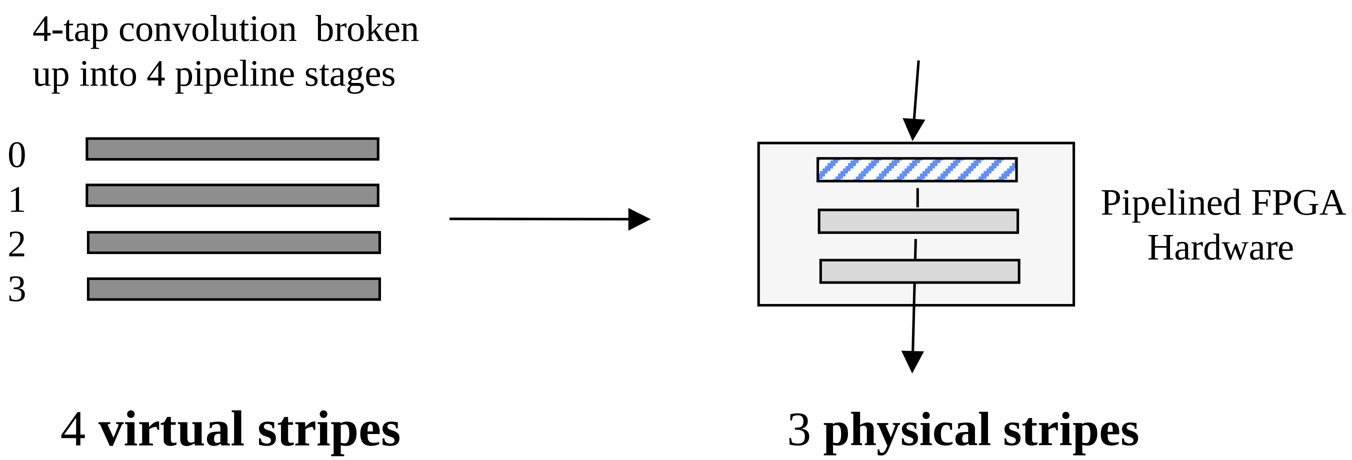
```
// 4-tap FIR filter
// 7 input data elements X[0] - X[6]
// 4 output data elements Y[0] - Y[3]
// 4 constant weights W[0] - W[3]

for i = 0 to 3   {
    Y[i] = 0;
    for j = 0 to 3   {
         Y[i] += X[i+j] * W[j];
    }
}
```

A Systolic Implementation

```
for i = 0 to 3  {
    Y[i] = 0;
    for j = 0 to 3  {
          Y[i] += X[i+j] * W[j];  }
}
```



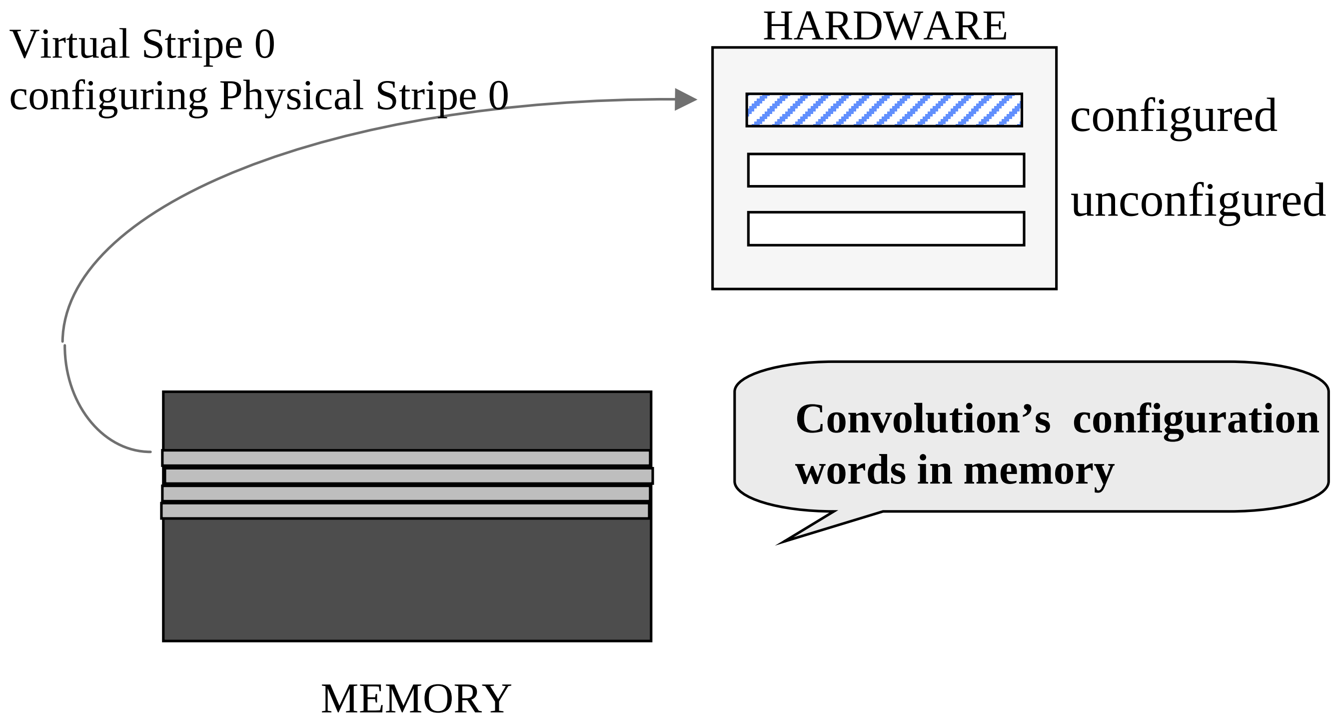
Target hardware



- Pipelined
- Concurrent reconfiguration and execution
  - One pipestage reconfigured each cycle
  - Other stages may execute

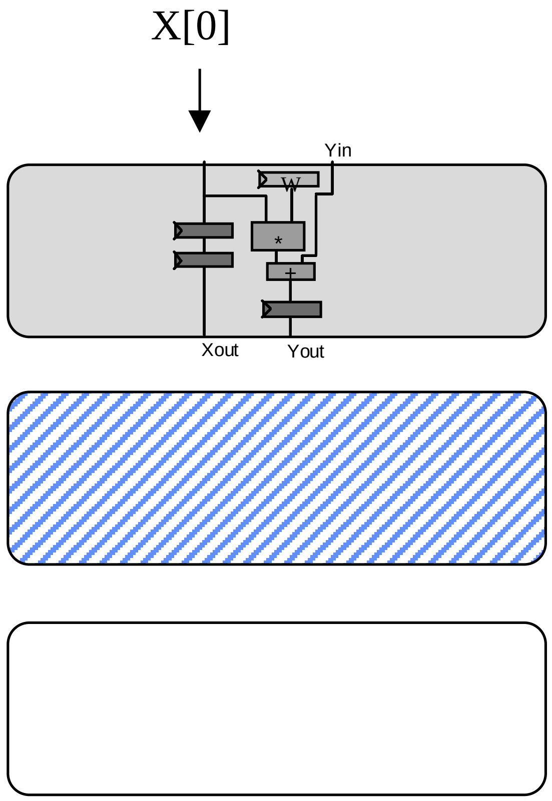
Clock Cycle 0

- Configure next available physical stripe

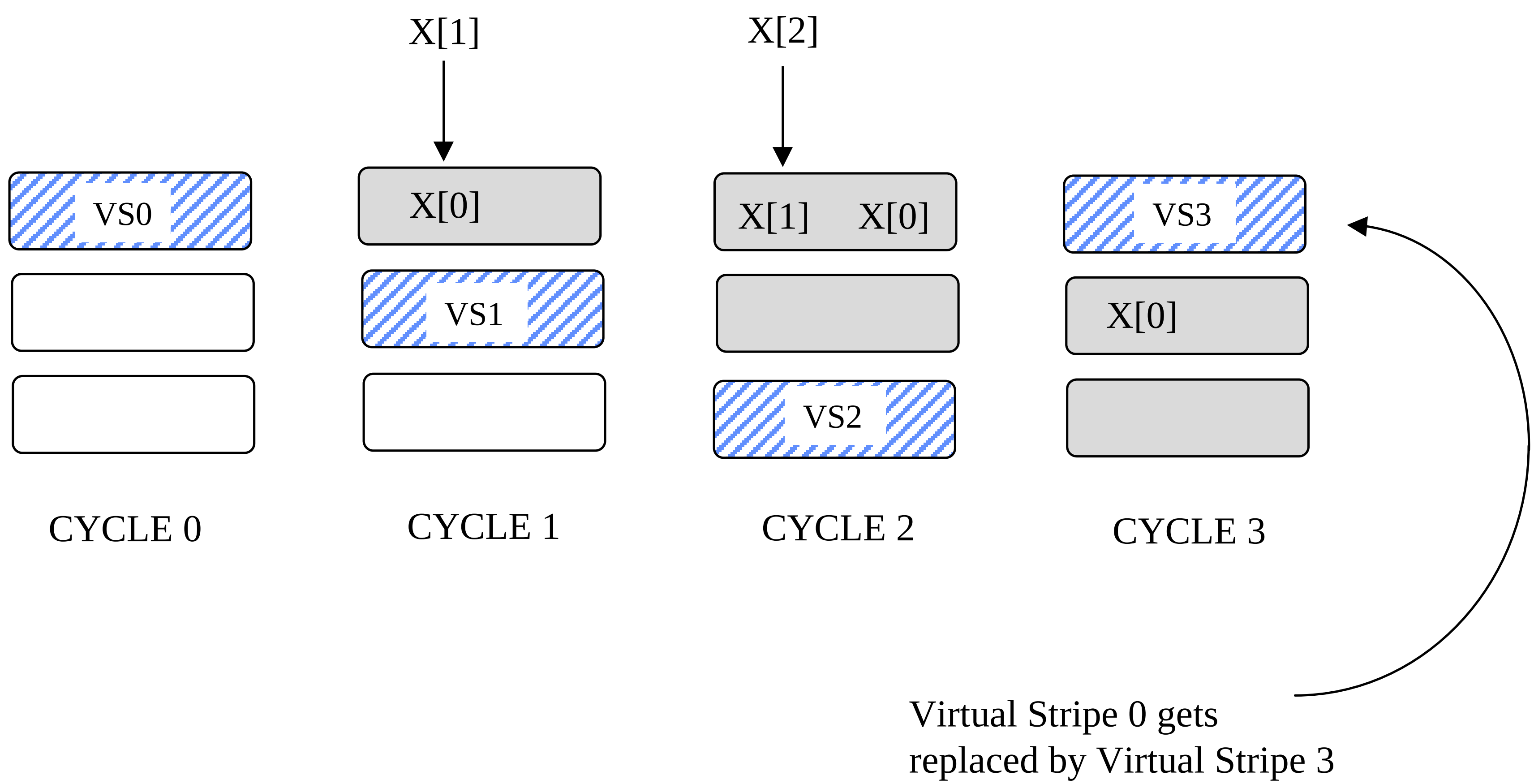


Clock Cycle1

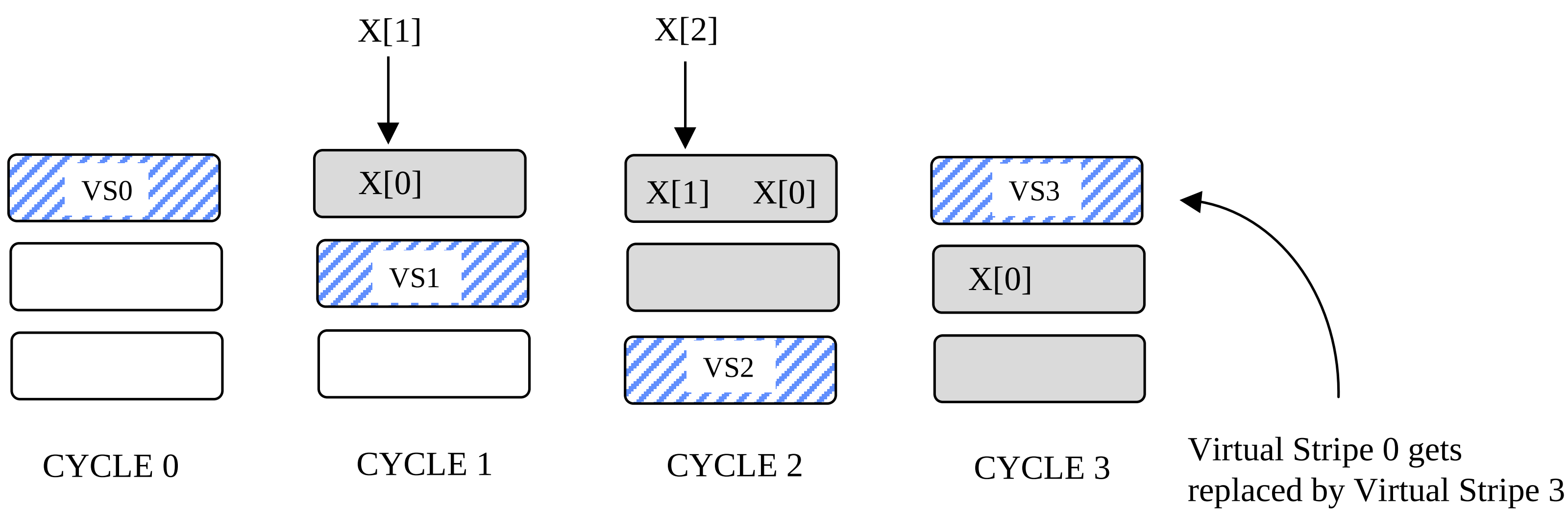
- Physical Stripe 0
  - configured to behave like Virtual Stripe 0
  - now executing
  - needs data X[0]
- Physical Stripe 1 being configured...



The first four cycles

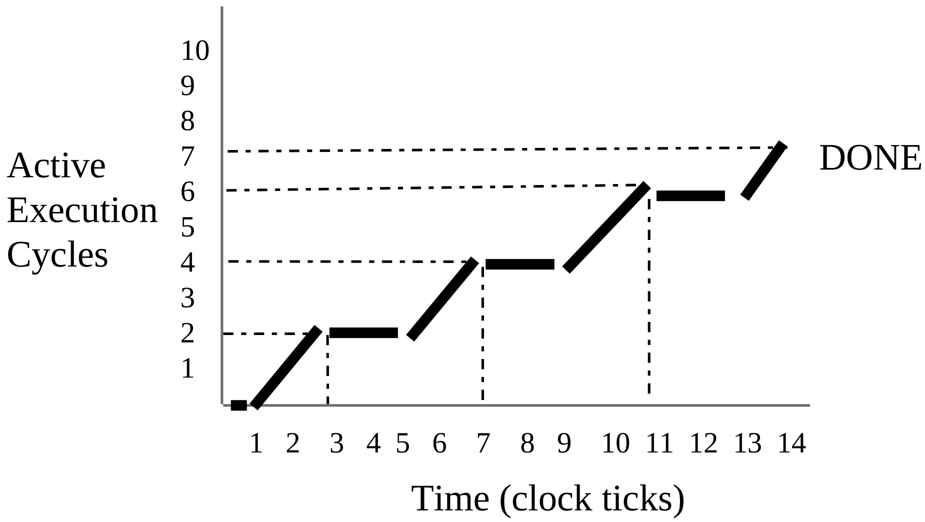


Pipeline Disruption



- break in data stream: input has to stop
- only done with X[1] and X[0].
  - needs to process X[2]-X[6]
  - 5 more execution cycles to go

The life of Virtual Stripe 0

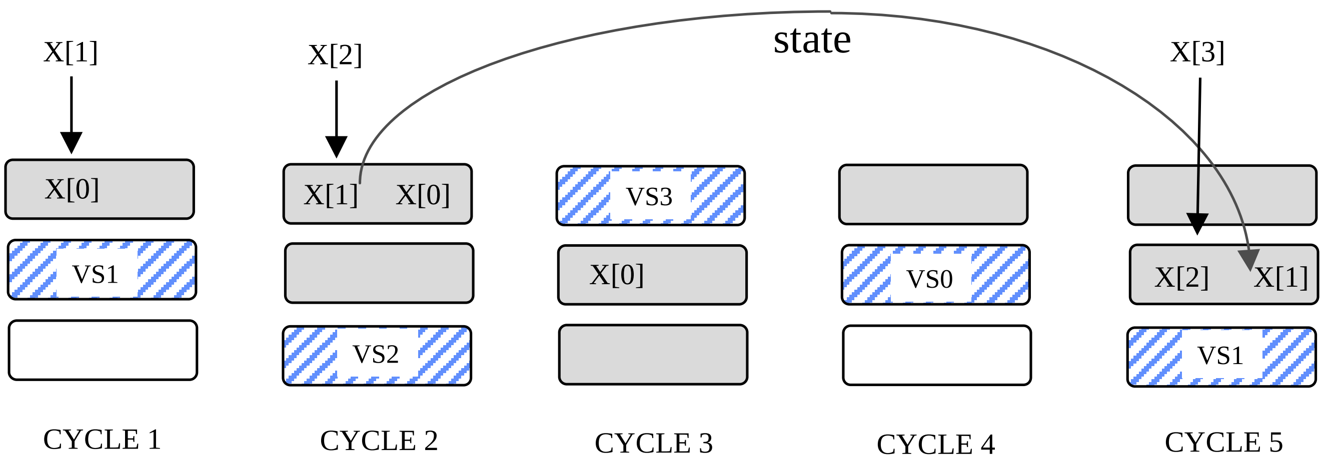


Behavior a function of application and architecture

With V virtual and P physical stripes

- execution cycles at a stretch = P - 1
- swap-out duration = V - P + 1

Further complications!

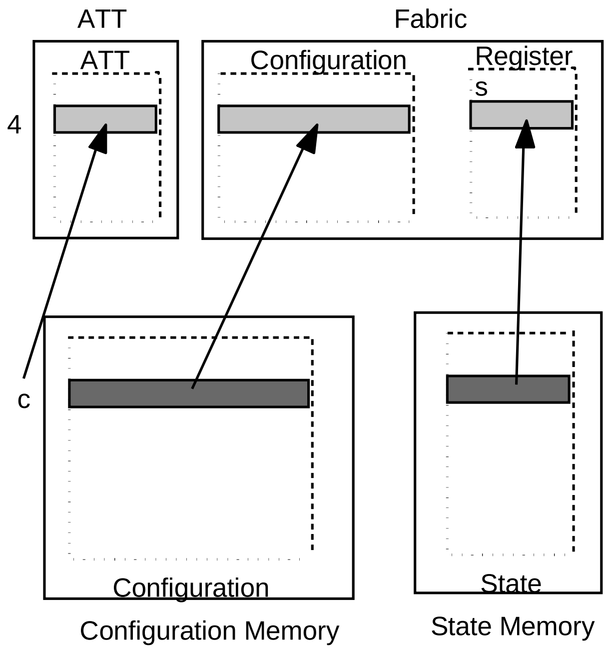


Virtual Stripe 0 has state

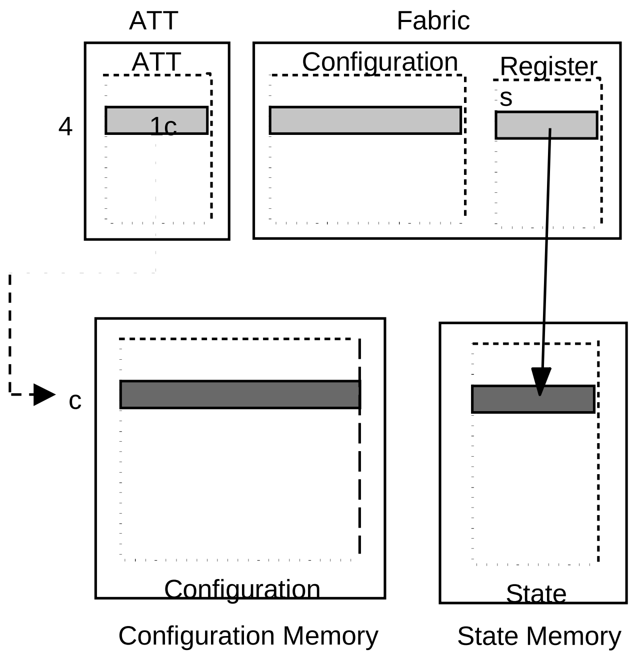
- required when it resumes executing
- need to save and restore it when stripe is configured back in

Implementing Save/Restore

SWAPPING INTO FPGA
(RESTORE)

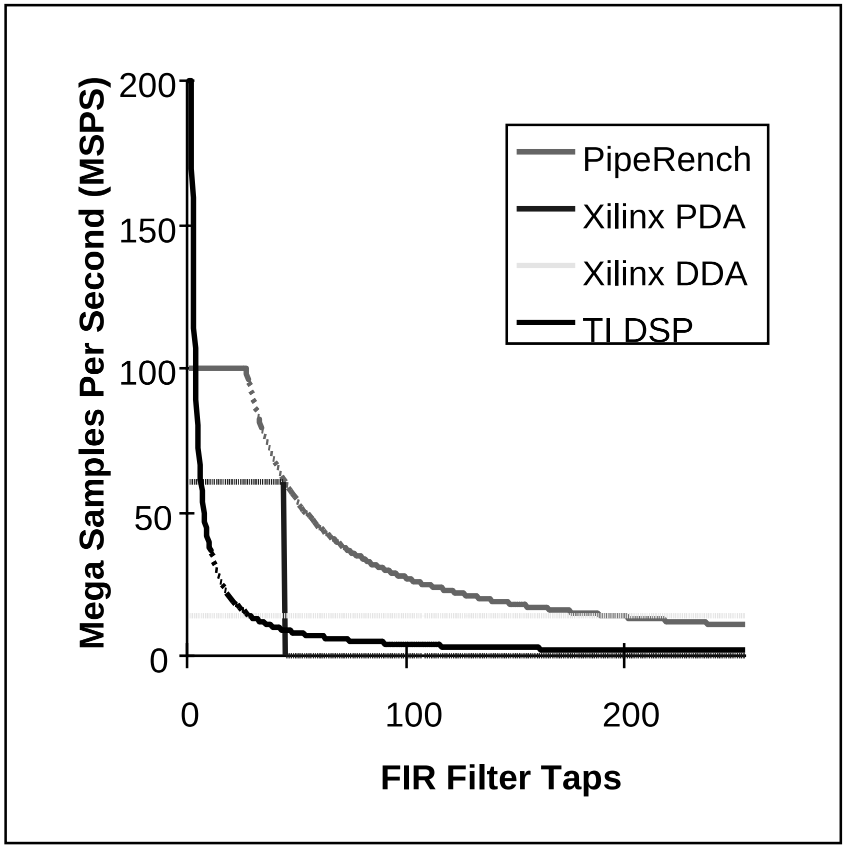


SWAPPING OUT OF FPGA
(SAVE)

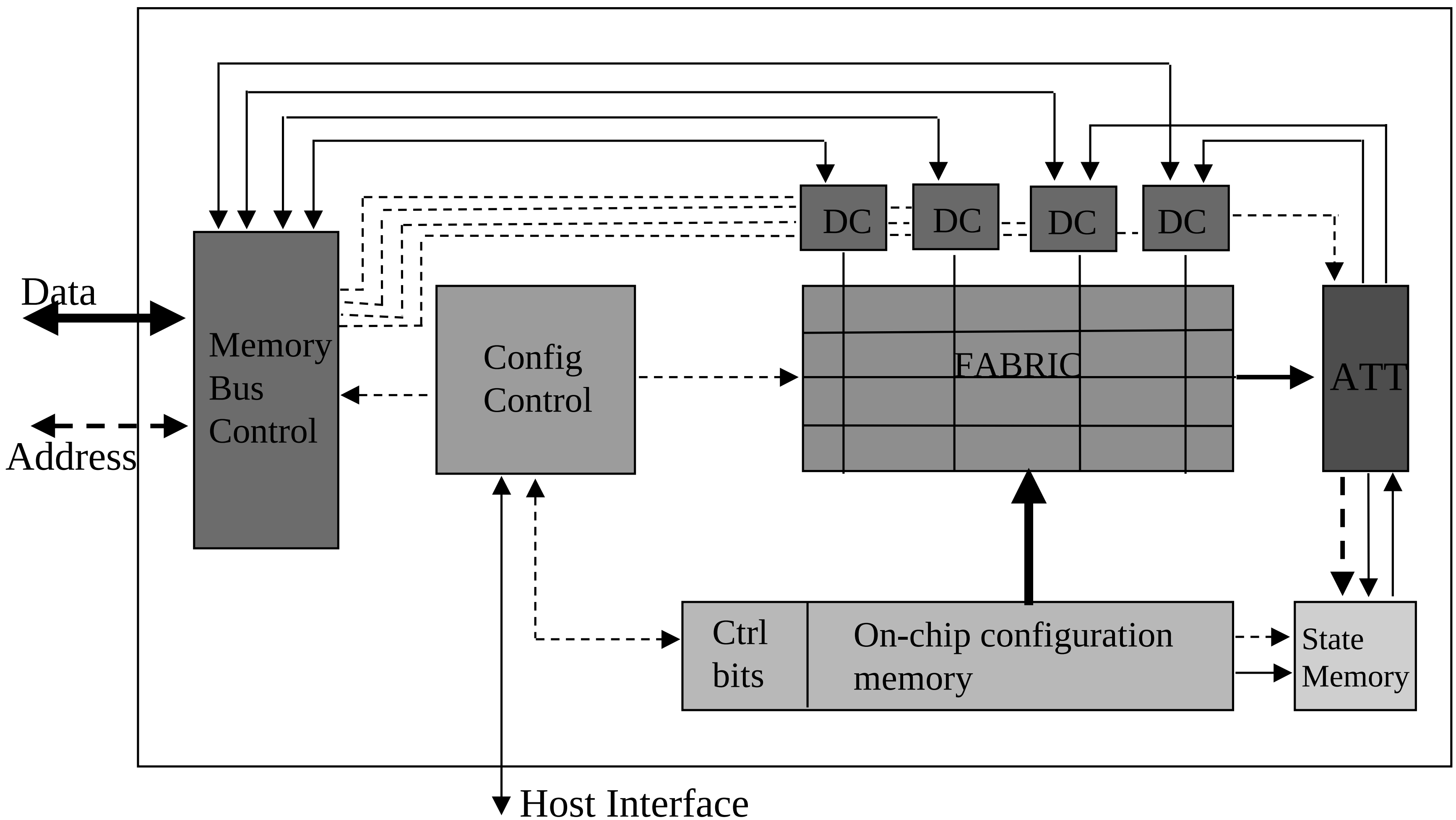


Conclusions

- Pipeline-reconfigurable FPGAs provide
  - forward compatibility
  - robust compilation



PipeRench-1



Data
Address
Memory Bus Control
Config Control
DC
DC
DC
DC
FABRIC
ATT
Ctrl bits
On-chip configuration memory
State Memory
Host Interface

Implementing hardware virtualization

Reconfigure entire FPGA

- need more reconfiguration time
- need intermediate storage