

Millimeter-Wave Power Amplifiers for Wireless Communications



Wei Tai



David Ricketts



Rick Carley

Scaling of silicon-based technologies has substantially increased the cut-off frequency of transistors. Their unprecedented switching speed makes the design of highly integrated millimeter-wave (30-300GHz) ICs increasingly feasible. However, realization of a highly efficient, highly linear Watt-level mm-wave power amplifier (PA) in silicon is still an open problem. The reasons behind this are three-fold: First, reduced breakdown voltage minimizes available voltage swing at the device output; as a result, efficient power combining strategies have to be deployed to achieve high output power. Second, device gain is greatly reduced at mm-wave frequencies. The benefit of a high efficiency switch-mode output stage is diminished since its low power gain requires substantial driving power, resulting in little improvement in system efficiency. Finally, the conductive silicon substrate reduces the quality factor of on-chip passive devices. This makes it particularly difficult to perform matching and power combining in an efficient manner. In addition to these technology-related challenges, the complex modulation schemes used in modern communication standards require highly linear PAs. Efficiency at power back-off, which is important due to the high peak-to-average power ratio (PAPR) in OFDM systems, is hard to achieve with traditional linear PAs. To attack these difficulties, we propose a PA architecture which incorporates an outphasing transmitter with a multi-way power combining structure. The outphasing action enables the use of more efficient switch-type output stages without sacrificing linearity. Through supply voltage switching, efficiency at low output power is boosted, which greatly enhances average efficiency in high PAPR PAs. Multi-way power combining through a zero-degree combiner minimizes loss and area consumption with acceptable isolation, and it also performs the required impedance transformation. Experimental PA chips that aim to validate these design concepts at 45GHz and 94GHz have been fabricated in 130nm SiGe BiCMOS and 45nm SOI CMOS processes, respectively.

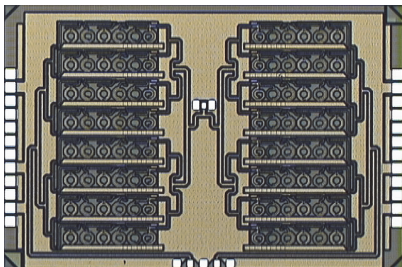


Fig. 1: Chip micrograph of a 45GHz 16-way outphasing power amplifier in 130nm SiGe BiCMOS that achieved 0.69W peak output power.

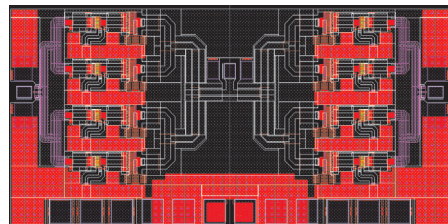


Fig 2: Chip layout of a 94GHz 8-way outphasing power amplifier in 45nm SOI CMOS with simulated peak output power of 0.6W and power-added efficiency of 19%.