Efficient Analog Performance Modeling by Bayesian Model Fusion



Fa Wang **Wangyang Zhang** **Xin Li**

With the continuous scaling of IC technology, analog and mixed-signal (AMS) circuits have become increasingly vulnerable to process variations. Performance modeling is an important technique to facilitate efficient parametric yield estimation for AMS circuits with consideration of large-scale process variations. In this project, we develop a novel statistical method, referred to as Bayesian Model Fusion (BMF), for efficient performance modeling of large-scale, complex AMS systems. The key idea of BMF is to borrow the data generated from an early stage (e.g., schematic level) to create accurate performance models at a late stage (e.g., post layout) with low computational cost. This goal is achieved by carefully modeling the correlation between two different design stages through Bayesian inference.

As a demonstration example, we consider a simplified SRAM read path implemented with a 32nm CMOS SOI process. In this example, there are 61572 independent random variables that model the device-level variations, including both inter-die variations and random mismatches. Our objective is to approximate the post-layout read delay as an analytical function of these device-level variations. For testing and comparison purposes, two different performance modeling techniques are implemented: (1) the traditional method based on sparse regression, and (2) the proposed BMF approach that borrows schematic-level simulation data for post-layout performance modeling. Figure 1 and Table 1 show the modeling error and cost for both methods. Note that BMF achieves 4.5× runtime speed-up over the traditional method, while simultaneously offering superior accuracy.

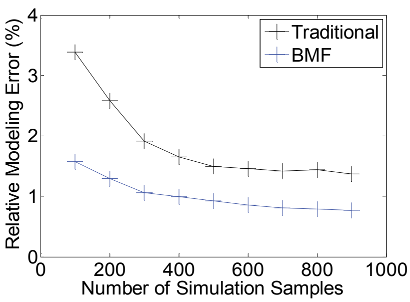

Fig. 1: Modeling error as a function of the number of post-layout simulation samples.

	Trad	BFM
Modeling error	1.38%	1.29%
Number of simulations	900	200
Simulation time (min)	1829	407
Fitting time (sec)	9.23	5.44
Total modeling time (min)	1829	407

TABLE 1: Comparison of performance modeling cost.