

On the Mitigation of NBTI and PBTI Induced Degradation



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Negative Bias Temperature Instability (NBTI), a PMOS aging phenomenon and Positive Bias Temperature Instability (PBTI), its NMOS counterpart, are poised to cause significant degradation to transistor behavior in future technologies. Hence, reducing the impact of these phenomena has become a critical challenge for temporal reliability concerns in nanoscale designs. As smaller transistors are more likely to undergo NBTI and PBTI effects, the trend of technology scaling has made these effects more significant. In addition, higher operating temperatures and longer operating times increase the circuit degradation phenomenon. Experimental data on PMOS aging indicate that NBTI can incur a 50mV increase in the magnitude of PMOS threshold voltage, and in turn slow down the circuit by nearly 10%. If the thickness of gate oxide shrinks down to 4nm, the circuit lifetime will be dominated by increased NBTI effects. We propose the use of *logic restructuring* (LR) and *pin reordering* (PR) to mitigate the effects of NBTI and PBTI. These two methods induce no gate overhead. Instead, both methods involve moving the gates and pins on the circuit in a manner that leaves the output unchanged but accounts for possible delays and tries to reduce them.

We conducted HSPICE simulations on several different sizes of transistor technologies to determine the effects of our proposed degradation mitigation methods. Assuming 65nm technology, we show that the effects of NBTI and PBTI combined are greater than either of their effects alone (Fig. 1). Furthermore, LR and PR reduce the delays caused by NBTI and PBTI to the nominal values. To see the impact of smaller technology nodes, Fig. 2 shows the voltage degradation values due to PBTI for 65-22nm technologies. Smaller transistors have smaller absolute voltage degradation values, but these have more effect because smaller transistors also have lower error margins. Future directions include taking into account more forms of degradation and modeling newer transistor technologies.

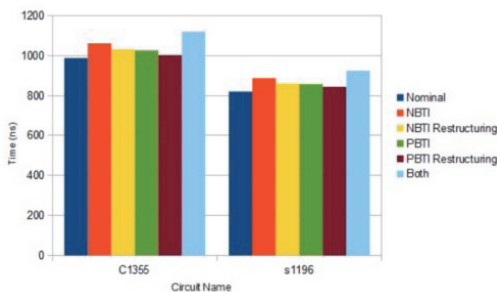


Fig. 1: 65nm restructuring results

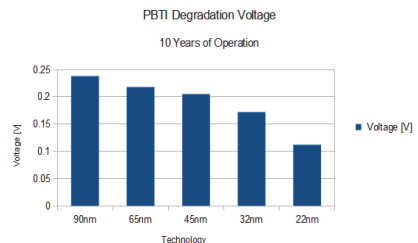


Fig. 2: Voltage degradation for 65-22nm